



CEP20N65SA/CEB20N65SA CEF20N65SA

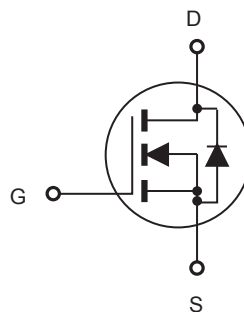
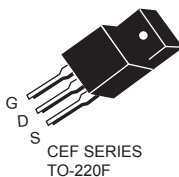
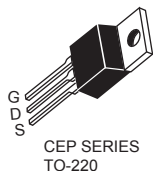
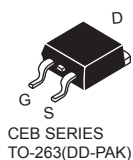
N-Channel Enhancement Mode Field Effect Transistor

PRELIMINARY

FEATURES

Type	V _{DSS}	R _{DS(ON)}	I _D	@V _{GS}
CEP20N65SA	650V	0.18Ω	20A	10V
CEB20N65SA	650V	0.18Ω	20A	10V
CEF20N65SA	650V	0.18Ω	20A ^d	10V

- Super high dense cell design for extremely low R_{DS(ON)}.
- High power and current handling capability.
- RoHS compliant.



ABSOLUTE MAXIMUM RATINGS $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Limit		Units
		TO-220/263	TO-220F	
Drain-Source Voltage	V _{DS}	650		V
Gate-Source Voltage	V _{GS}	±20		V
Drain Current-Continuous @ T _C = 25 °C @ T _C = 100 °C	I _D	20	20 ^d	A
		13	13 ^d	A
Drain Current-Pulsed ^a	I _{DM} ^e	80	80 ^d	A
Maximum Power Dissipation @ T _C = 25 °C - Derate above 25 °C	P _D	205	35	W
		1.64	0.28	W/°C
Single Pulsed Avalanche Energy ^h	E _{AS}	40		mJ
Single Pulsed Avalanche Current ^h	I _{AS}	9		A
Operating and Store Temperature Range	T _J , T _{stg}	-55 to 150		°C

Thermal Characteristics

Parameter	Symbol	Limit		Units
Thermal Resistance, Junction-to-Case	R _{θJC}	0.61	3.6	°C/W
Thermal Resistance, Junction-to-Ambient	R _{θJA}	62.5	65	°C/W

This is preliminary information on a new product in development now .
Details are subject to change without notice.

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<http://www.cet-mos.com>



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Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0V, I_D = 250\mu A$	650			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 650V, V_{GS} = 0V$			1	μA
Gate Body Leakage Current, Forward	I_{GSSF}	$V_{GS} = 20V, V_{DS} = 0V$			100	nA
Gate Body Leakage Current, Reverse	I_{GSSR}	$V_{GS} = -20V, V_{DS} = 0V$			-100	nA
On Characteristics^b						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 250\mu A$	2		4	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 20A$		0.15	0.18	Ω
Dynamic Characteristics^c						
Input Capacitance	C_{iss}	$V_{DS} = 30V, V_{GS} = 0V,$ $f = 1.0\text{ MHz}$		1565		pF
Output Capacitance	C_{oss}			935		pF
Reverse Transfer Capacitance	C_{rss}			13		pF
Switching Characteristics^c						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 520V, I_D = 10A,$ $V_{GS} = 10V, R_{GEN} = 6\Omega$		29		ns
Turn-On Rise Time	t_r			10		ns
Turn-Off Delay Time	$t_{d(off)}$			76		ns
Turn-Off Fall Time	t_f	$V_{DS} = 520V, I_D = 10A,$ $V_{GS} = 10V$		8		ns
Total Gate Charge	Q_g			42		nC
Gate-Source Charge	Q_{gs}			7		nC
Gate-Drain Charge	Q_{gd}		15		nC	
Drain-Source Diode Characteristics and Maximun Ratings						
Drain-Source Diode Forward Current	I_S^f				20	A
Drain-Source Diode Forward Voltage ^b	V_{SD}	$V_{GS} = 0V, I_S = 20A^g$			1.5	V
Notes : a.Repetitive Rating : Pulse width limited by maximum junction temperature . b.Pulse Test : Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$. c.Guaranteed by design, not subject to production testing. d.Limited only by maximum temperature allowed . e.Pulse width limited by safe operating area . f.Full package $I_{S(max)} = 8A$. g.Full package V_{SD} test condition $I_S = 8A$. h.L = 1mH, $I_{AS} = 9A, V_{DD} = 50V, R_C = 25\Omega$, Starting $T_J = 25\text{ C}$.						

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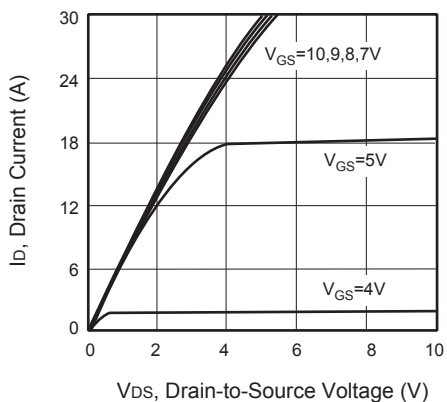


Figure 1. Output Characteristics

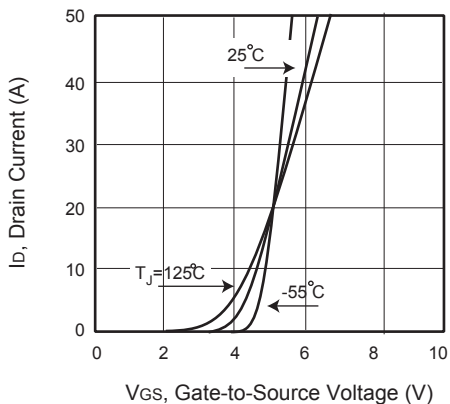


Figure 2. Transfer Characteristics

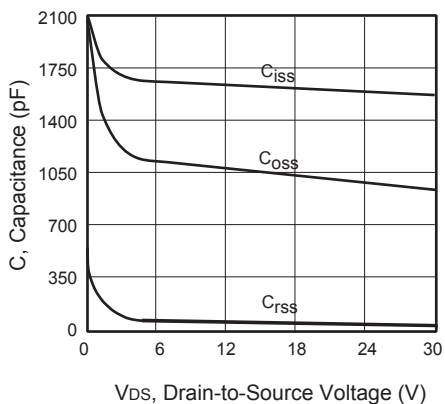


Figure 3. Capacitance

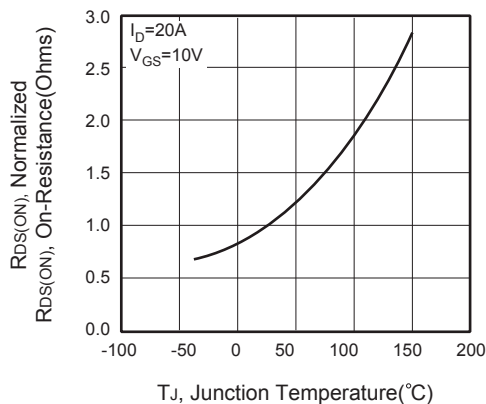


Figure 4. On-Resistance Variation with Temperature

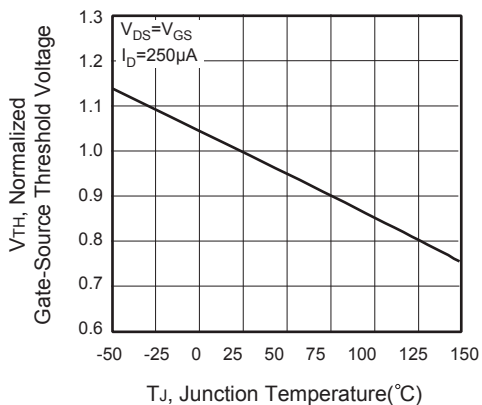


Figure 5. Gate Threshold Variation with Temperature

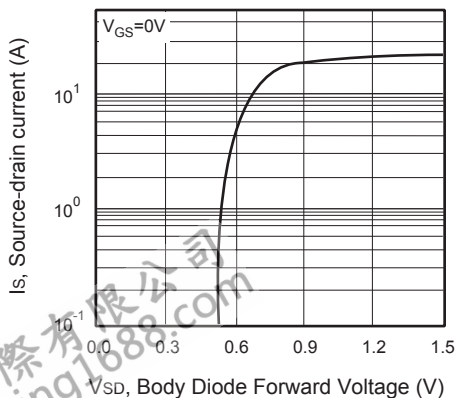
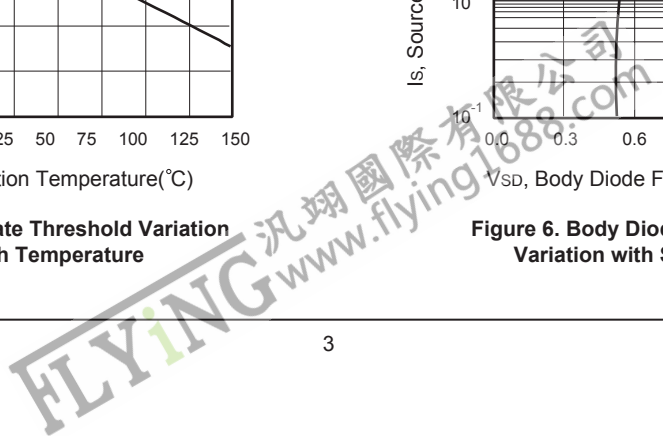


Figure 6. Body Diode Forward Voltage Variation with Source Current





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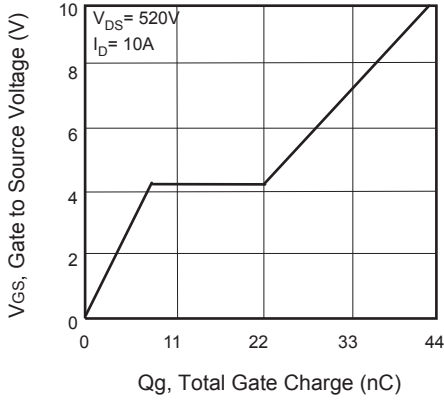


Figure 7. Gate Charge

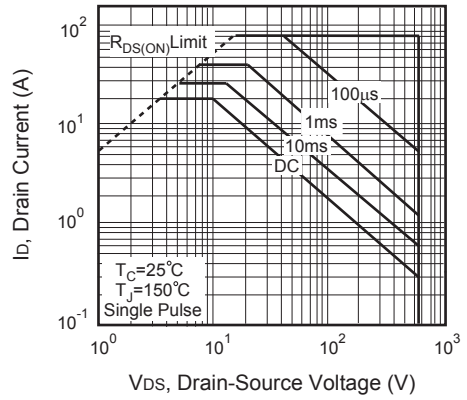


Figure 8. Maximum Safe Operating Area

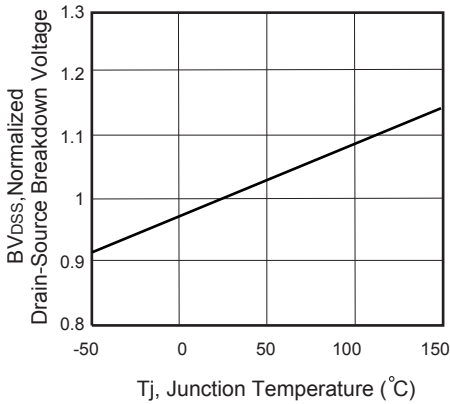


Figure 9. Breakdown Voltage Variation VS Temperature

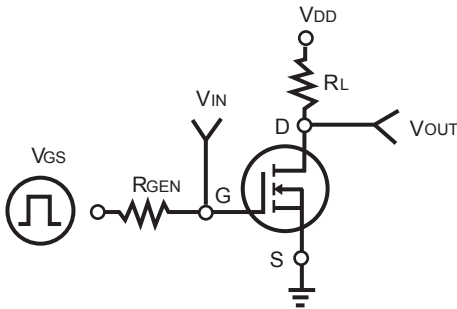


Figure 10. Switching Test Circuit

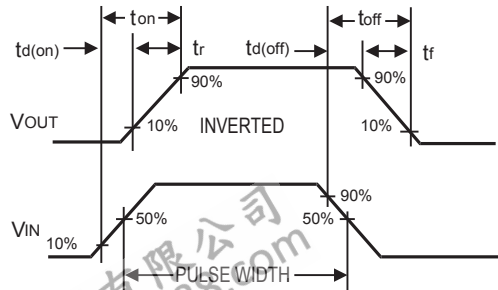


Figure 11. Switching Waveforms

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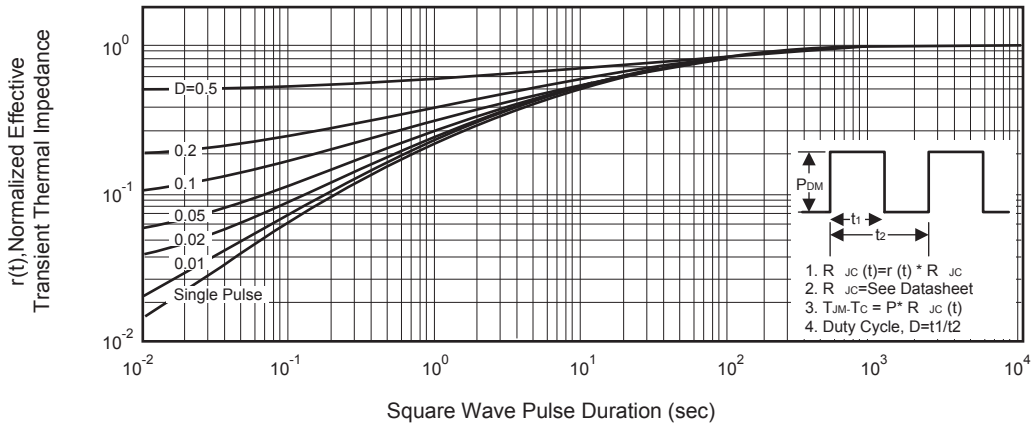


Figure 12. Normalized Thermal Transient Impedance Curve