BOOST/ BUCK-BOOST/ BUCK CONTROLLER IC with FREQUENCY SYNCHRONIZATION FUNCTION

FEATURES

- AEC-Q100 Grade1 Qualified
- 5 - 60V input voltage range
- Single resistor programmable constant current driver
- Excellent constant current accuracy ±3% typically
- 0.1V feedback reference voltage tailor-made for LED application
- Support Boost/Buck/Buck-Boost/SEPIC configuration
- DC and PWM dimming
- On-chip thermal shutdown at 170°C
- Thermal derating by using external NTC
- Programmable soft start
- Programmable switching frequency 80kHz to 1MHz (by default 430kHz)
- Dithering in oscillator frequency to simplify the EMI design
- Cycle-by-cycle current limit
- Over-current protection
- Open LED overvoltage indication and protection
- External Clock Synchronization Capability
- 15μA shutdown current
- TSSOP16 package

Applications

- High Power LED Driver
- LED illuminance
- LCD backlight illumination
- Automotive interior lighting
- Automotive Headlights

PIN ARRANGEMENT

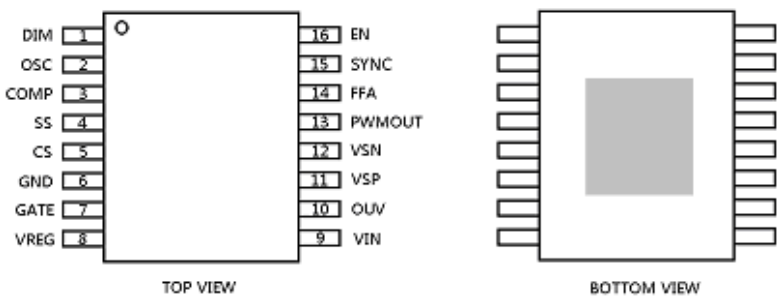
GENERAL DESCRIPTION

The T8333FI is designed to operate as a constant current source for driving high current LEDs. It is a current mode control IC which provides a good line transient response. The device can provide an excellent constant current accuracy of +/-3% typically. A frequency adjustment pin allows the user to program the frequency from 80kHz to 1MHz to optimize efficiency, performance or external components.

Moreover, integrated diagnostics and two fault outputs give indication of VIN and VREG under-voltage, chip over-temperature, output open circuit, LED short circuit and LED undercurrent, and can be configured to provide short to supply and short to ground protection for the LED connections, LED overcurrent and shorted LED string protection.

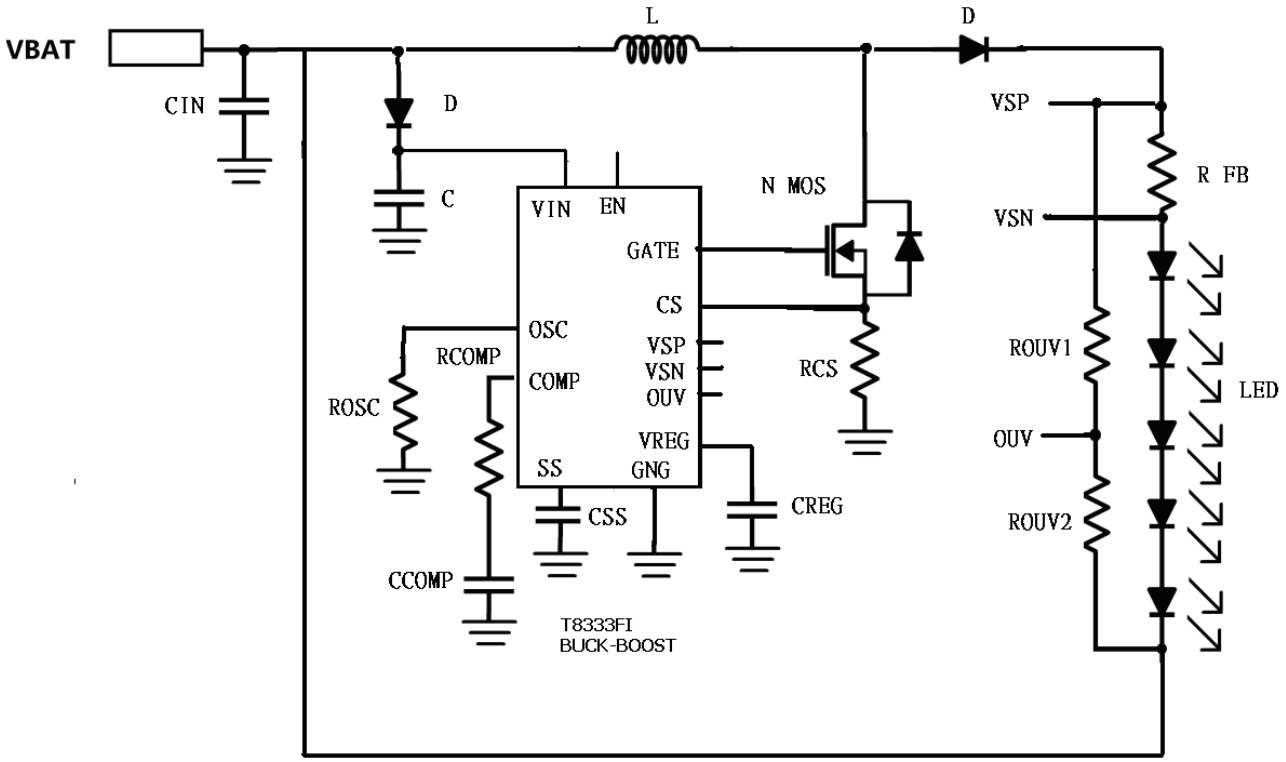
PART NUMBER EXAMPLES

PART NO.	PACKAGE
T8333FI	TSSOP-16



T8333FI, TSSOP16

TYPICAL APPLICATION
(BUCK-OOST)



PIN DESCRIPTION

Pin No.	Pin Name	Pin Description
1	DIM	DC Dimming
2	OSC	Frequency set
3	COMP	Compensation pin.
4	SS	Soft start
5	CS	Connect a resistor for the current mode control
6	GND	Ground Pin. IC ground.
7	GATE	Switch gate drive
8	VREG	Internal regulator
9	VIN	Main supply
10	OUV	Over-voltage and under-voltage protection pin, connect this pin to the output voltage of the LED through a resistor divider to detect the over voltage and under-voltage.
11	VSP	Load current sense +ve input
12	VSN	Load current sense –ve input
13	PWMOUT	PWM gate drive for external p-channel MOSFET (active low)
14	FFA	Fault indication flag
15	SYNC	Clock Synchronization
16	EN	Enable chip
	EP	Connect to GND

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
VIN, VSP and OUV pin voltage relative to GND		-0.3 to +60	V
OUV		VSP - 5 to VSP	
PWMOUT		VSP - 10 to VSP	V
GATE		-0.3 to +10	V
VSN		VSP - 1V to VSP	V
FFA		-0.3 to +60	V
VREG		-0.3 to +8	V
DIM pin voltage relative to GND		-0.3 to +3.3	V
EN, SYNC, SS, COMP, CS and OSC pin voltage relative to GND		-0.3 to +5.5	V
Junction temperature range	T_J	-40 to +150	^oC
Maximum soldering temperature (at leads, 10sec)	T_{LEAD}	300	^oC
Storage temperature range	T_S	-65 to +150	^oC
Junction to case thermal resistance	θ_{JC}	3.5	^oC /W

Electrical Characteristics

◆Denotes the specifications which apply over the full operating temperature range T_J = -40°C to +125°C, V_{IN} = 12V. Otherwise specifications are at T_A = 25°C, V_{IN} = 12V.

Symbol	Description	Conditions		Min.	Typ.	Max.	Unit
Supply and Reference							
V_{OVP}	Fixed Output Over-voltage Protection	Measured at VSP with respect to ground			65.5		V
V_{IN}	Operating voltage range		**	5		60	V
V_{INUV}	V_{IN} under voltage	V_{IN} Decreasing		4.25	4.5		V
ΔV_{INUV}	V_{IN} under-voltage hysteresis				260		mV
I_Q	Operating quiescent current	f_{OSC} = 430kHz; Capacitor load = 1000pF at gate pin			2.5		mA
I_{OFF}	Shutdown current	IC shutdown by $V_{EN} < V_{EN\_OFF}$			20	26	μA
V_{REG}	Regulation pin voltage	V_{IN}=12V, I_{REG} = -10mA	◆	6.5	7.3	8	V
V_{REGUV}	VREG under voltage	V_{REG} Decreasing		3.8	4.2		V
ΔV_{REGUV}	V_{REG} under-voltage hysteresis				350		mV
V_{REGCL}	V_{REG} current limit	V_{REG} short to GND	◆	-25	-52		mA
Oscillator and Soft Start							
f_{osc_dither}	Oscillator frequency (with Dither ON)	Rosc = 3.3kΩ			1000		kHz
		Rosc = 6.8kΩ			500		kHz
		Rosc short to GND			430		kHz
		Rosc = open			80		kHz
f_{osc}	Oscillator frequency (with Dither OFF)	Rosc short to GND			384		kHz
	Oscillator frequency range			80		1000	kHz
I_{SS}	Soft start current	Current out of pin			11		μA
V_{RAMPUP}	The Upper limit of the Soft Start Ramp Up Voltage Active Region				1.8		V

Symbol	Description	Conditions		Min.	Typ.	Max.	Unit
LED Current Sense and Control							
V_{IDL}	Differential input voltage (Active)	EN=High, VSP - VSN		97	100	103	mV
V_{OCLED}	LED Over current threshold	EN=High, VSP - VSN		150	167	182	mV
$V_{DIM,ON}$	DC Dimming ON			0.116	0.156	0.196	V
$V_{DIM,MAX}$	DC Dimming Control for Full Brightness	DC voltage on the DIM pin			2.3		V
$V_{DIM,MIN}$	DC Dimming Control for Gate Driver OFF	DC voltage on the DIM pin		0.07	0.11	0.15	V
Gate Drive Output							
T_R	Turn-On Rise Time	Rosc = open Loading Cap =2.2nF (from 10% to 90%)			30		ns
T_F	Turn-Off Fall Time	Rosc = open Loading Cap =2.2nF (from 10% to 90%)			30		ns
V_{OL}	Output low level		◆			0.2	
V_{OH}	Output high level		◆		VREG		V
D_{MAX}	Maximum duty cycle		◆	88	92	96	%
Switch Current Sense and Amplifier							
V_{SWOCP}	Switch over-current protection threshold voltage			440	500	560	mV
A_{CS}	Voltage Gain				4		V/V
I_{BIASS}	Input Bias Current			-24	-32	-40	μA
Logic Inputs and Outputs							
V_{EN_ON}	EN pin chip enable voltage	V_{EN} rising	◆	2			V
V_{EN_OFF}	EN pin disable voltage		◆			0.8	V
t_{DIS}	Disable time	f_{OSC} = 430kHz			38		ms
FFA	Fault output (Open Drain)	I_{OL}=1.2mA, fault not asserted				0.26	V
$I_{FFA(SINK)}$	Fault output FFA sink current	V_O=0.4V, fault not asserted		0.8	1.7		mA

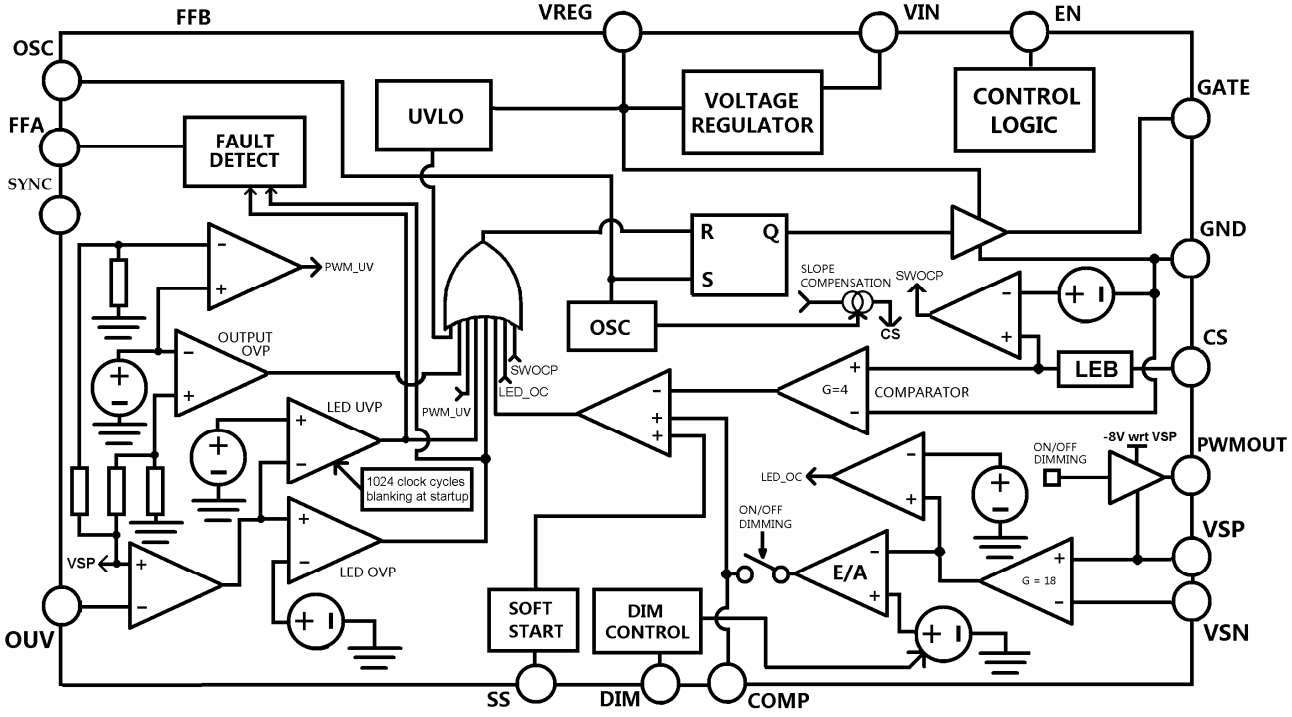
Symbol	Description	Conditions		Min.	Typ.	Max.	Unit
Dither Generator							
f_{SPREAD}	Dither Frequency Range	% of switching frequency			+/-12		%
Clock Synchronization							
$V_{SYNC,ON}$	Clock Synchronization enable voltage threshold	SYNC voltage rising			1.35		V
$V_{SYNC,OFF}$	Clock Synchronization disable voltage threshold	SYNC voltage falling			1.15		V
Slope Compensation							
I_{SLOPE}	Slope Injection Current	Sawtooth current added to current sense (CS) pin			-97		μA
Protection							
t_{FB}	Fault blank timer	At start up, f_{OSC} = 430kHz			2.4		ms
V_{SCL}	LED short protection voltage	V_{SP} - V_{OUV}		260	300	330	mV
V_{OCL}	LED open protection voltage	V_{SP} - V_{OUV}		1.08	1.2	1.34	V
PWM_{UV}	PWMOUT Under-voltage	VSP Decreasing		5	5.5		V
PWM_{HYS}	PWMOUT Hysteresis				0.56		V
T_{SD}	Over-temperature warning threshold*	Measured at junction, temperature increasing	*		170		°C
T_{SDHYS}	Over-temperature hysteresis*	Measured at junction, recovery = T_{SD}-T_{SDHYS}	*		35		°C

◆ Function is correct but parameters are not guaranteed.

** At VIN equals 5-6V and >50V, the part only guarantees GATE pin switching but not guarantee to follow the electrical parameters.

*Parameters are not tested at production and guaranteed by design, characterization and process control.

Block Diagram



FUNCTIONAL DESCRIPTION

T8333FI is a constant current LED driver which can be configured as a Boost, Buck-Boost, Buck or SEPIC converter. It depends on the user's choice of the number of LEDs on the output. Typical converter application circuits of T8333FI are shown in the next section.

VIN

The VIN is the power supply voltage pin for the supply to the control circuit of T8333FI. The pin has an UVLO function, once voltage on the pin reaches 4.52V; the IC is ready to start the operation. When the voltage on this pin falls below 4.52 V, the IC will be shutdown. *(Note: A bypass capacitor must be connected close between this pin and GND.)*

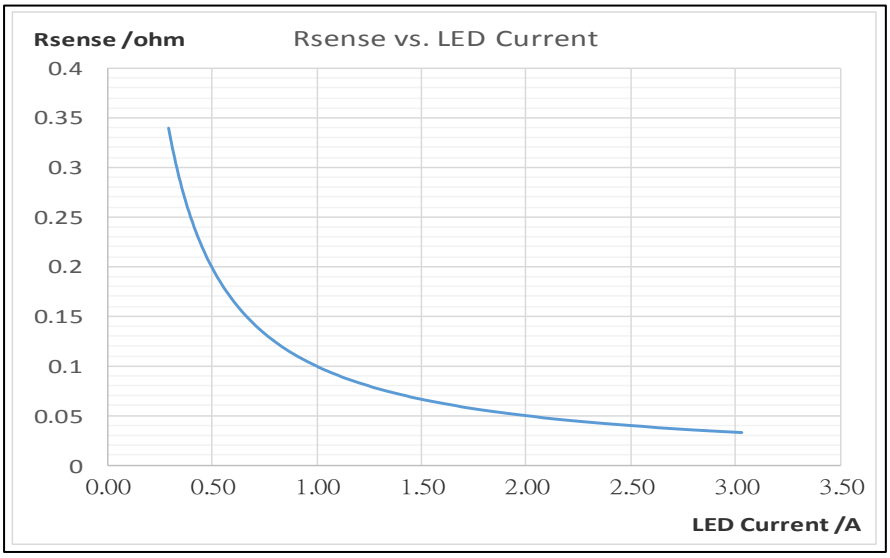
VREG

To provide a filtered output and to ensure the regulator is stable, a 2.2μF or above ceramic capacitor is required to be connected between VREG and GND. The ceramic type should be a quality type such as X5R, X7R, or X8R. The VREG pin voltage is for driving the external switching MOSFET. Normally, at 12V VIN, the VREG voltage is 7.3V typically. The UVLO point of the VREG is around 4.2V. Once the VREG is under 4.2V, the gate driver will be turned off and it will resume back to normal when the VREG voltage rises back to around 4.55V.

Output LED current setting

The output LED current is determined by a combination of the LED sense resistor R_{SENSE}, the LED current threshold voltage, V_{IDL}, (100mV). For example, to program a 1A output current, the sensing resistor will be

$$R_{SENSE} = \frac{100mV}{1A} = 0.1\Omega$$



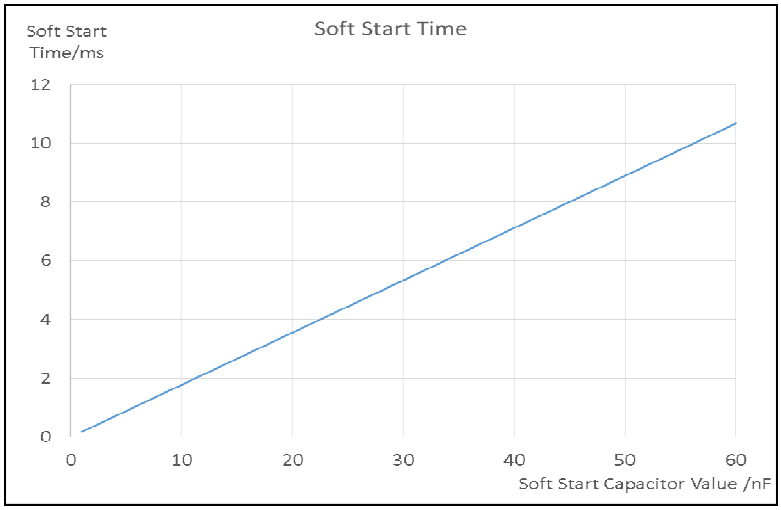
Soft Start

For many applications, it is important to minimize the inrush current at start-up. The built-in soft-start circuit significantly reduces the start-up current spike and output voltage overshoot. The soft-start interval is set by the soft-start capacitor selection according to the equation:

$T_{SS} = C_{SS} \times \frac{1.8V}{11\mu A}$, where T_{SS} is the soft start time and the C_{SS} is the soft start capacitor

For example, to program the soft start time as 2ms, the C_{SS} capacitor will be:

$$C_{SS} = 2ms \times \frac{11\mu A}{1.8V} => C_{SS} = 12nF$$



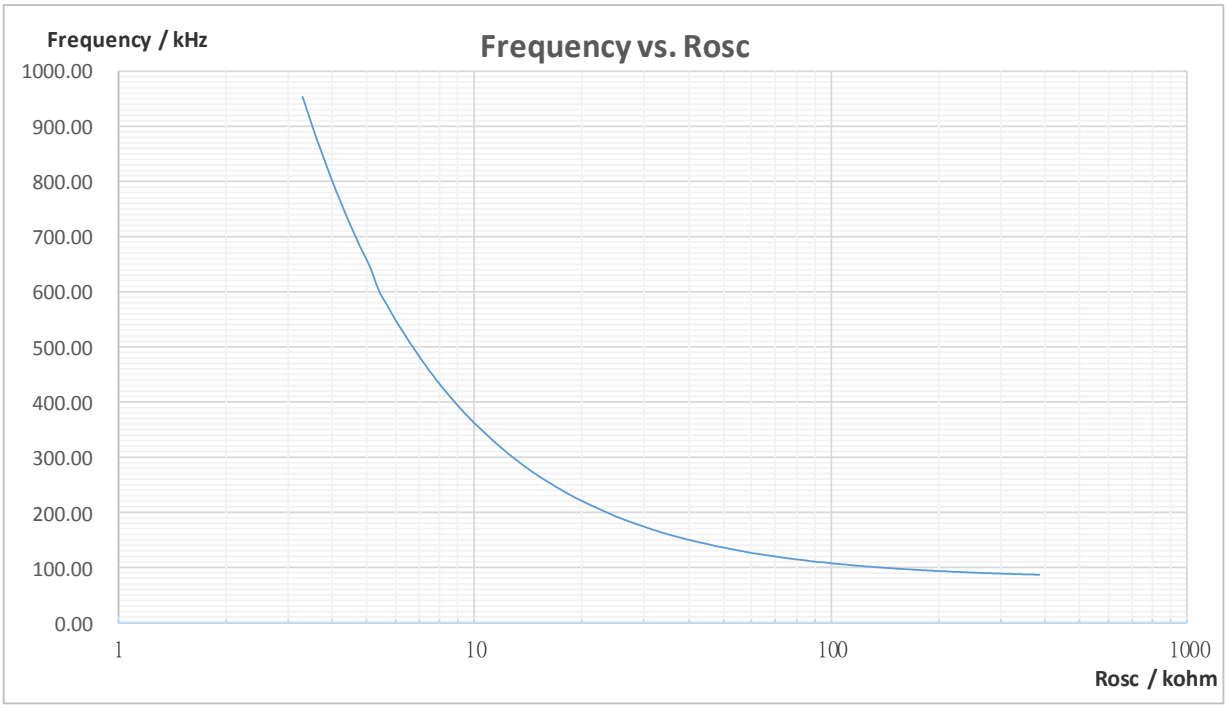
Frequency Dithering

T8333FI has an internal frequency dither function to improve the EMI performance of the system. The internal frequency is hopping in a small frequency range to reduce the radiation at the switching frequency which simplifies the EMI design. The dither frequency range is ~ +/-12% typically.

Oscillator

The oscillator can be programmed by tiding an external resistor R_{OSC} (kΩ). The oscillator is designed to run between 80 and 1000 kHz. The oscillator frequency is approximately:

$$f_{osc} = 80 + \frac{48000}{17 \times R_{osc}} (kHz)$$



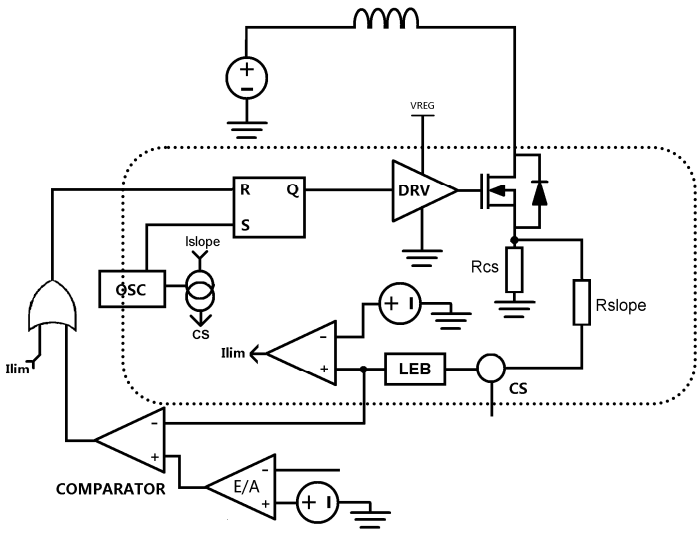
Note: The oscillator frequency will be around 80 KHz when OSC pin open and 430 KHz when short to GND

Enable Pin Function

The enable pin is to control the IC on/off operation. When the enable pin is pulled down over the disable time that stated in the datasheet (~16340 clock cycles which equivalent 38ms at switching frequency 430 kHz), the IC will completely shutdown and enter into the shutdown mode. The IC current consumption reduces to nearly 20μA. This pin can also be used as direct PWM input for LED dimming.

Switch current limit and over-current protection

T8333FI has a switch current limiting function. When the CS pin voltage reaches the current limit threshold (~0.5V), the IC begins to count for the switch over current. Once the switch over current is over 8 clock cycles, the IC will enter into hiccup mode. The hiccup mode turns off the gate driver for 8192 clock cycles. After the hiccup mode, the IC will resume to monitor for the switch over current, if the switch over current stills exist and over 8 switching clock cycles, the IC will go to the hiccup mode again. Of course, if the switch over current condition removed, the IC will resume to normal operation. The switch over current limit equation is shown below.



Slope Compensation

The slope compensation is to prevent subharmonic oscillations at duty cycles greater than 50% in continuous current conduction mode. A current source is provided at the CS pin as a sawtooth from 0 to 97μA. An external resistor, R_{SLOPE}, connected between the CS pin and the source connection of the MOSFET, is used to program the appropriate voltage level to scale the slope compensation for correct use with the appropriate topology and set up conditions that have been adopted.

PWMOUT Under-voltage

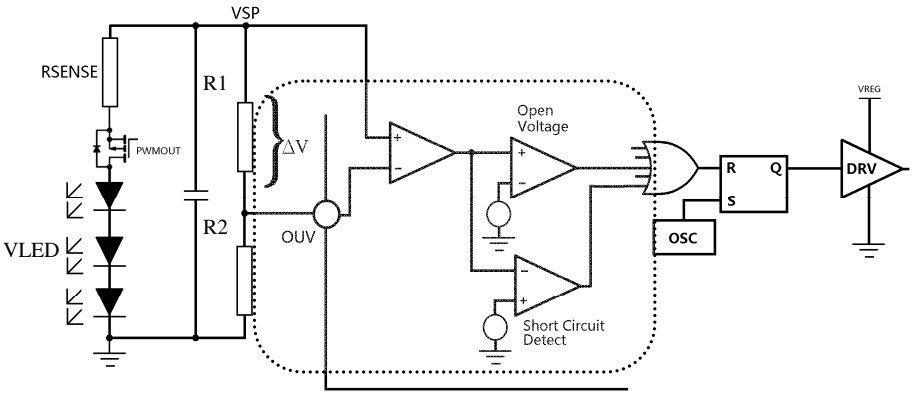
During startup, the VSP pin voltage is going to ramp up. When this voltage is under 6V, the PWMOUT will not provide any gate driving voltage to turn on a high side PMOS. When the VSP pin voltage exceeds 6V, the PWMOUT driver turns on and begin to provide a conduction path for the output LED. The PWMOUT will be disabled when the VSP pin voltage drops down to 5.5V (voltage hysteresis around 0.5V).

Fixed Over Voltage Protection

The T8333FI has a fixed over voltage protection which is implemented on the VSP pin. Once the VSP pin voltage over around 65.5V, the IC will stop the gate driver and the output voltage will drop. The hysteresis for the fixed over voltage protection is around 5V. Once the voltage on the VSP falls below around 60.5V, the IC will resume the switching on the gate driver.

Open and short LED protection

The open and short LED protection are implemented by placing a resistor divider on the output of the converter (VSP) with respect to the LED negative terminal. The divided sensing voltage is compared with the VSP voltage and formed △V which shown in below picture. If the voltage difference is over 1.2V for more than 2 clock cycles, the LED string will be treated as over voltage condition. Then, T8333FI will stop the gate driving voltage to the external MOSFET and entering into a hiccup mode. The hiccup mode will turn off both the gate driver and the PWMOUT for 8192 clock cycles. And the FFA and FFB pins are pulled low and open drain respectively. The IC gate driver will turn on again if the over voltage fault has been removed after the hiccup period. Normal voltage difference of VSP – OUV is within around 0.3V to 1.2V. If the over voltage stills exist after the hiccup period, no gate driver signal will coming out and the IC continues to count 8192 clock cycles for the hiccup mode again..



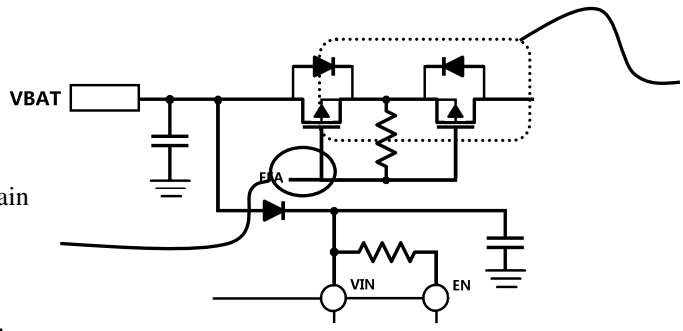
△V=VSP×(R1/(R1+R2))

△V＜0.3V LED short protection

△V＞1.2V LED open protection

(0.3V＜△V＜1.2V)

If the voltage difference is less than around 0.3V for 32 clock cycles (after the fault blanking time at IC startup, the blanking time is typically 1024 clock cycles), the LED will be treated as an output under voltage condition. T8333FI will stop the gate driving voltage to the external MOSFET and the FFA pin goes to open drain to disconnect the closed loop circuit path by back to back P channel MOSFETs of the converter.

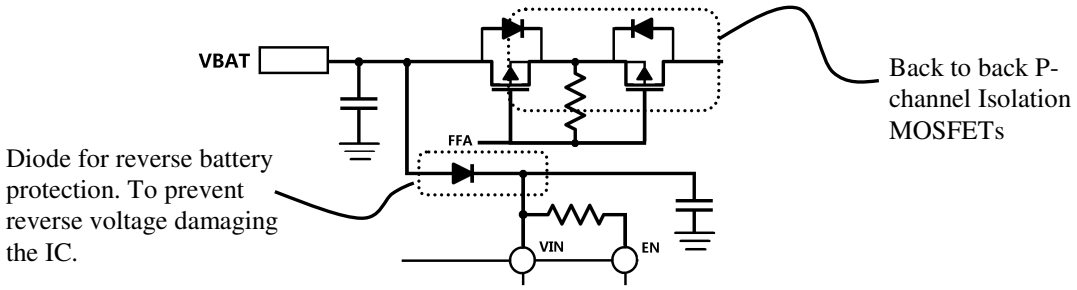


Note:
For 430kHz,

- *1024 clock cycles equivalent to 2.4ms.*
- *8192 clock cycles equivalent to 19ms.*

Reverse Supply Protection

Protection for the T8333FI is provided by an external low current diode between the VBAT and the VIN pin, as shown in the picture below. This can prevent damaging the IC under reverse battery condition. Also, additional of isolation MOSFETs, it is possible to provide reverse battery protection to the switching elements and the LEDs. The additional MOSFETs should be connected, as shown in picture below, with the drain to the supply and the source to the source connection of the original isolation MOSFET.



Over-temperature Protection

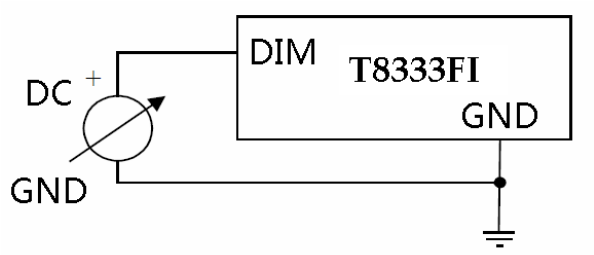
If the chip temperature exceeds the over-temperature threshold T_{SD} (~170°C), the IC will stop the gate driving. When the IC is shutting off, the IC's temperature will begin to drop. Once the temperature drops around 135°C (the temperature hysteresis is 35°C typically).The IC will resume to start switching again.

Clock Synchronization

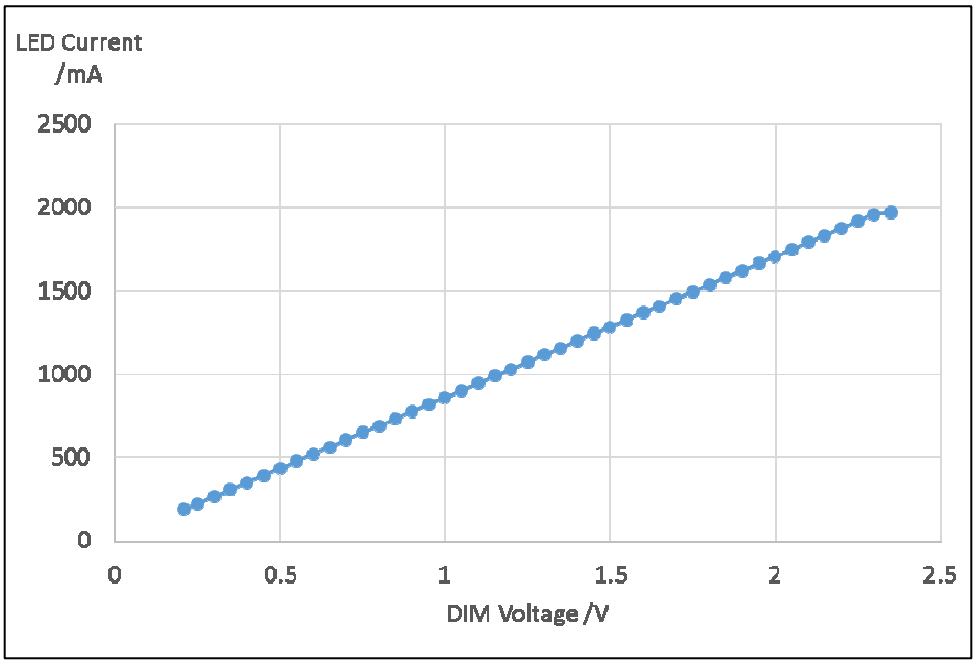
The SYNC pin is used to synchronize the internal oscillator. The frequency setting resistance, connected between OSC pin and GND pin, should be chosen to program an internal switching frequency typically 20% faster than the SYNC pulse frequency. Gate turn-on occurs at a fixed delay after the rising edge of SYNC. If SYNC is pulled to GND, the Gate will stop switching. If SYNC is floating, the controller IC will work at programmed switching frequency.

Output current adjustment by external DC DIM control voltage

The DIM pin can be driven by an external dc voltage, as shown, to adjust the output current to a value below the one programmed by R_{SENSE}.



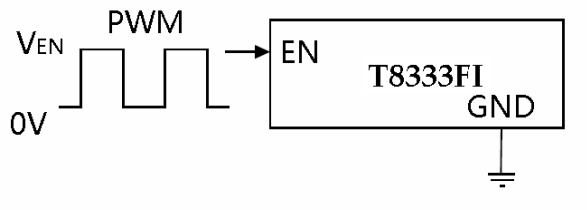
+Note that the DIM pin turns on voltage is 0.143V, 100% brightness setting corresponds to DIM pin above 2.3V. The DIM pin voltage < 0.1V, the LED controller will stop the gate driver.



Output current adjustment by PWM control

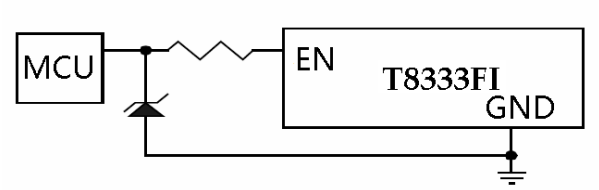
- **Directly driving EN input**

A pulse-width-modulation (PWM) signal with can be applied to the EN pin, as shown below, to adjust the output current to a value below the one programmed by R_{SENSE}.

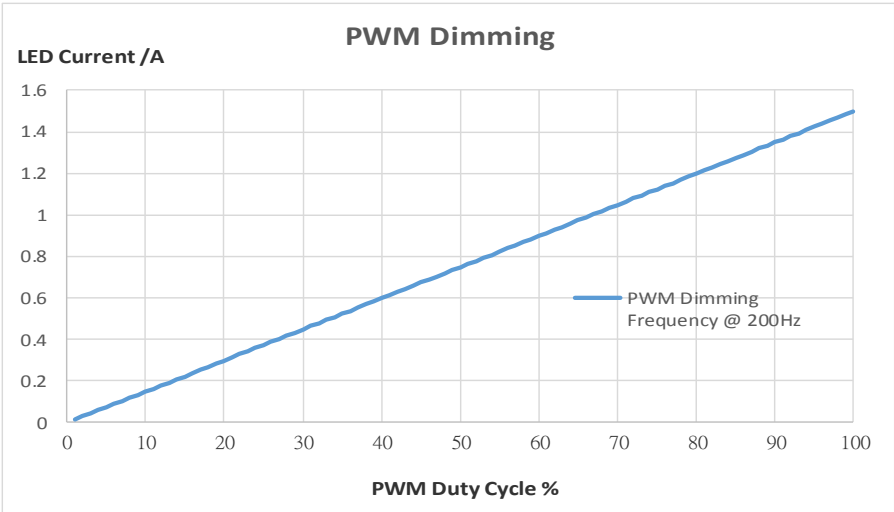


- **Driving the EN input from a microcontroller**

Another possibility is to drive the device from the open drain output of a microcontroller. The diagram below shows one method of doing this:



If the NMOS transistor inside the microcontroller has high drain capacitance / source capacitance, this arrangement can inject a negative spike into EN input of the T8333FI and cause erratic operation. The addition of a schottky clamp diode (cathode to EN) to ground and inclusion of a series resistor (10K) will prevent this. See the section on PWM dimming for more details of the various modes of control using high frequency and low frequency PWM signals.



Testing Condition: Vin=12V, LED voltage and full load current = 15V, 1.5A.

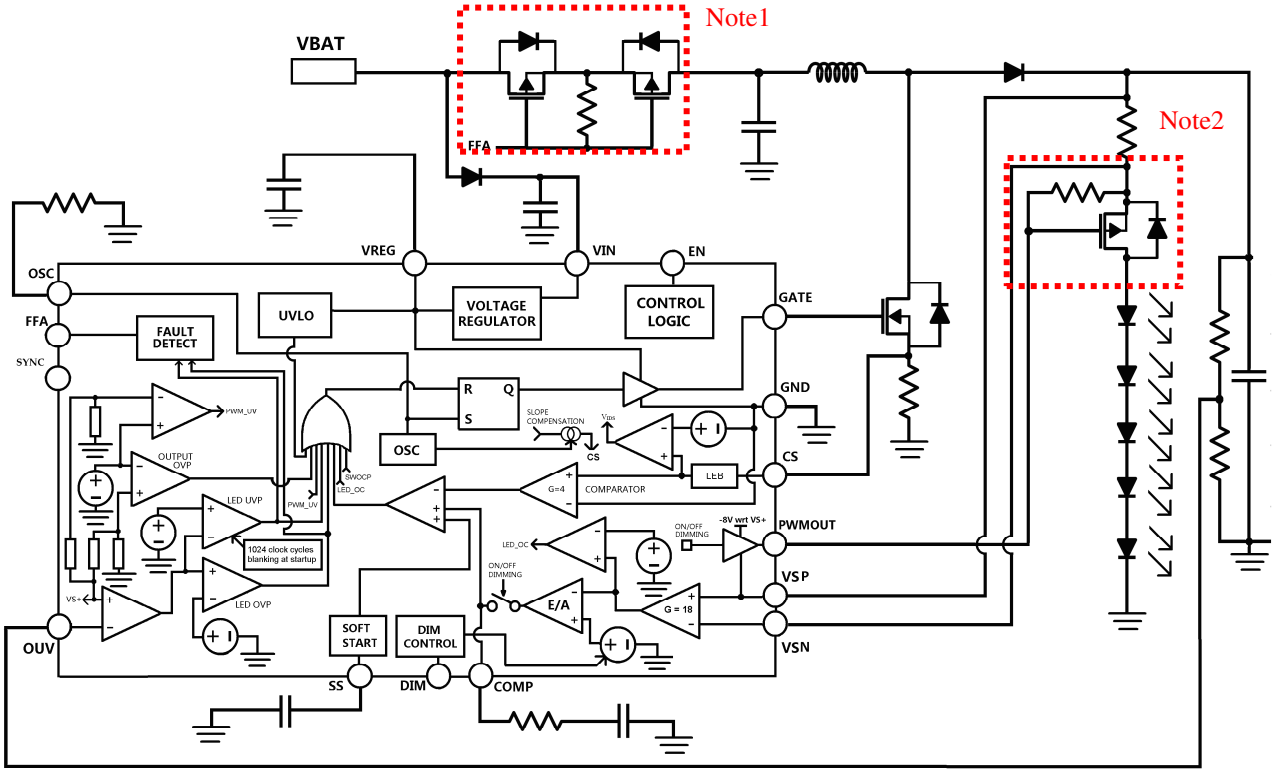
Fault Table

Fault Descriptions	Actions on Pin Drivers			Conditions	Other Actions
	FFA	PWMOUT	GATE		
Normal Operation	**Pull Low**	**ON**	**Switching**	**No Fault**	
VREG under-voltage	Pull Low	OFF	OFF	VREG < $VREG_{UV}$ (~ 4V)	N/A
Programmable Under-Voltage	Open Drain	OFF	OFF	VSP-Vouv < V_{SCL} (~0.3V)	Go for hiccup mode 8192 clock cycles.
Programmable Over-Voltage	Pull Low	OFF	OFF	VSP-Vouv > V_{OCL} (~1.2V)	Go for hiccup mode 8192 clock cycles.
Over-temperature	Pull Low	OFF	OFF	T_{SD} > ~170°C Hysteresis = 35°C	N/A
Vin under-voltage	Open Drain	OFF	OFF	VIN < VIN_{UV} (~4.5V)	N/A
PWMOUT under-voltage	Pull Low	OFF	OFF	VSP < PWM_{UV} (~5.5V)	N/A
VSP Fixed over-voltage	Pull Low	OFF	OFF	VSP > VIN_{OVP} (~65V)	N/A
Switch Over current	Pull Low	OFF	OFF	Vcs > SWOCP (~0.4V for 8 clock cycles).	Go for hiccup mode 8192 clock cycles.
LED over-current	Pull Low	OFF	OFF	VSP-VSN > VOCLED (~ 0.15V)	Go for hiccup mode 8192 clock cycles.

Remark:
OFF = turn off P-channel MOSFET in PWMOUT; GATE is at $V_{OL.}$

TYPICAL APPLICATION CIRCUITS

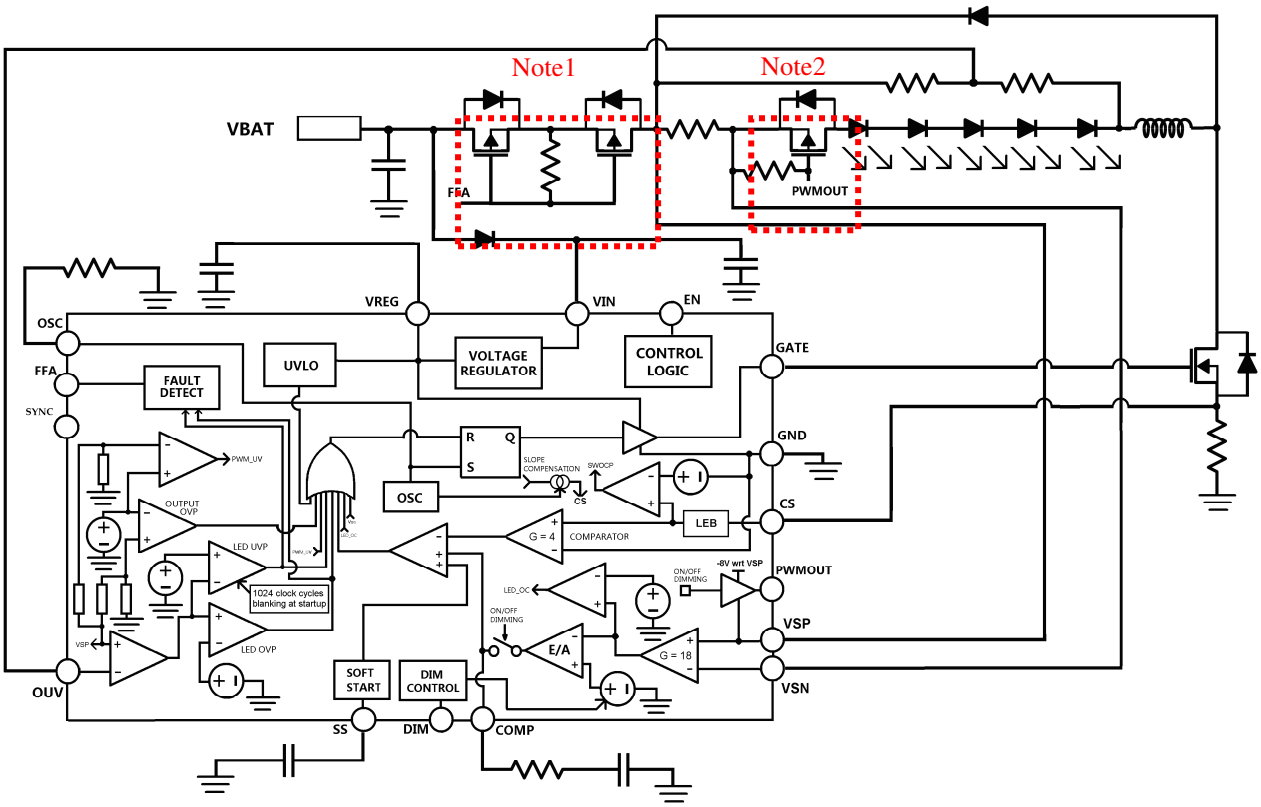
The T8333FI can be configured as Boost, Buck, Buck-Boost and SEPIC. The application circuits are shown below:



Boost Converter which is for VBAT < VLED

Note: VLED must be less than MOSFET rating.

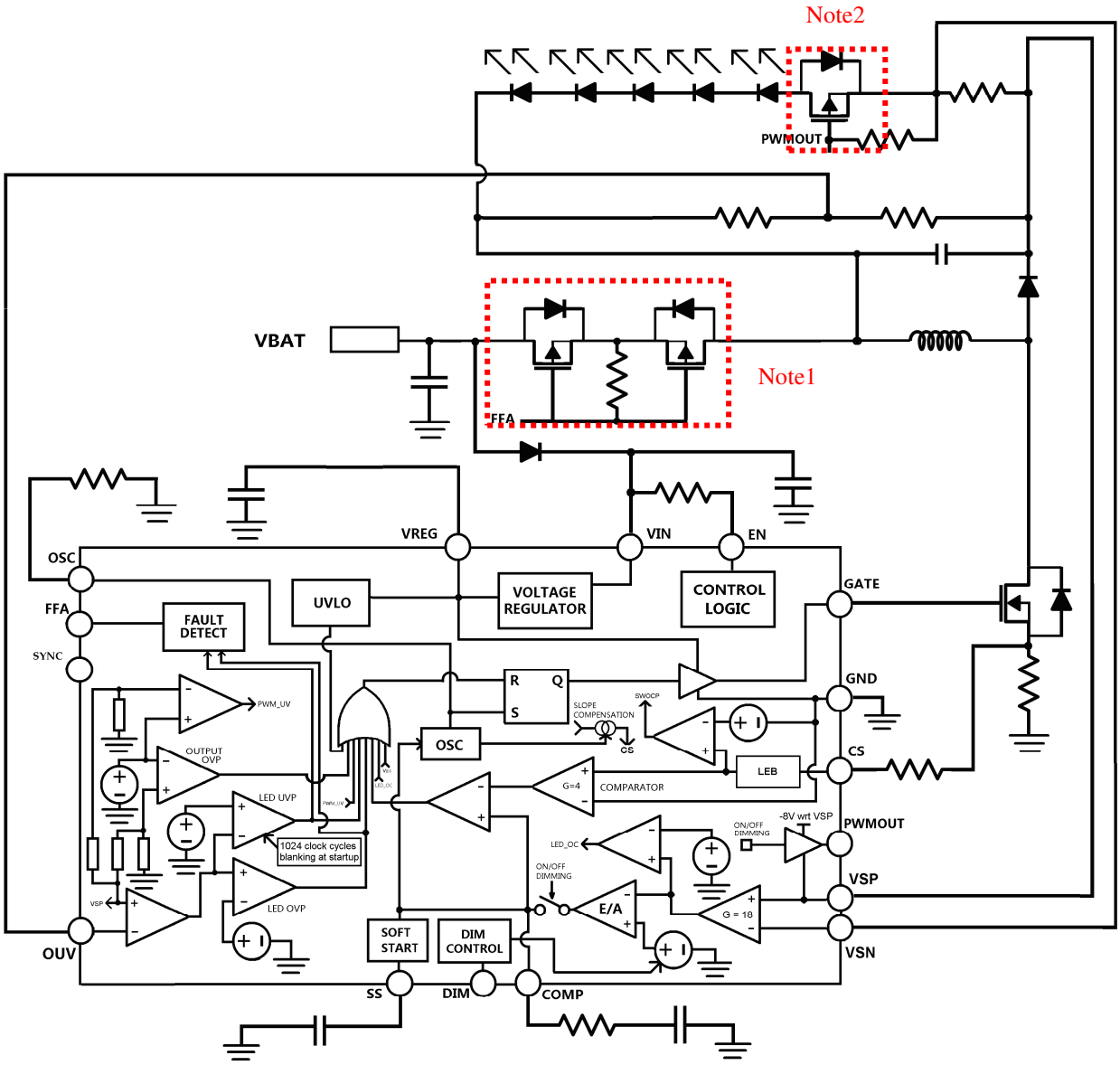
Note1： option for safety protection
Note2： option for high precision PWM dimming



Buck Converter which is for VBAT > VLED

Note: VBAT must be less than MOSFET rating.

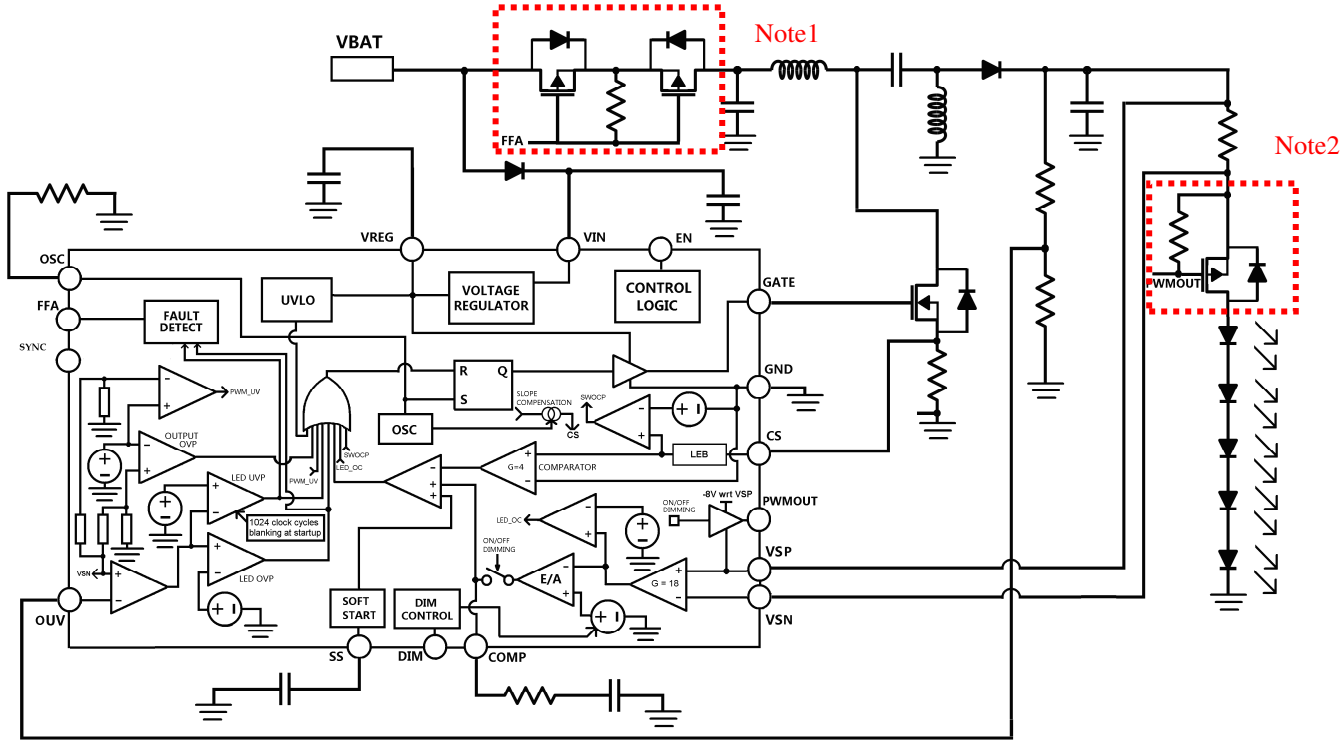
Note1： option for safety protection
Note2： option for high precision PWM dimming



Buck-Boost which is for VBAT < VLED or VBAT > VLED.

Note: VBAT +VLED must be less than MOSFET rating.

Note1： option for safety protection
Note2： option for high precision PWM dimming



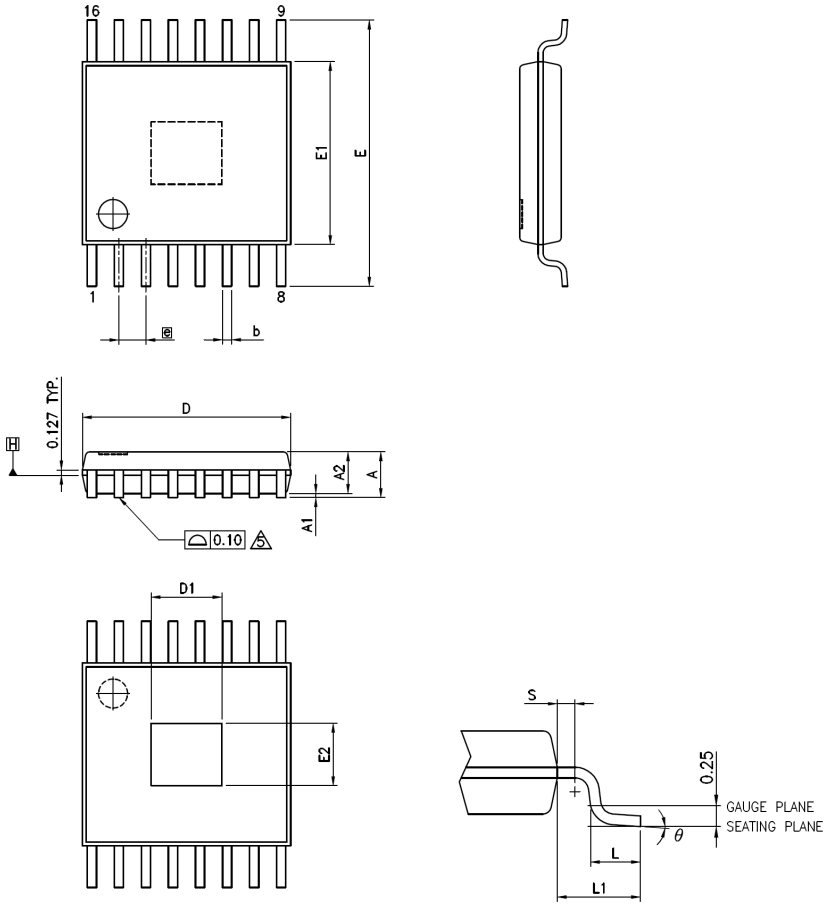
SEPIC which is for VBAT < VLED or VBAT > VLED.

Note: VBAT +VLED must be less than MOSFET rating.

Note1： option for safety protection
Note2： option for high precision PWM dimming

PACKAGE INFORMATION

Package Type: TSSOP16



THERMALLY ENHANCED VARIATIONS ONLY

VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.00	–	0.15
A2	0.80	1.00	1.05
b	0.19	–	0.30
D	4.90	5.00	5.10
E1	4.30	4.40	4.50
E		6.40 BSC	
e		0.65 BSC	
L1		1.00 REF	
L	0.45	0.60	0.75
S	0.20	–	–
θ	0°	–	8°

THERMALLY ENHANCED DIMENSIONS(SHOWN IN MM)

PAD SIZE	E2		D1	
	MIN.	MAX.	MIN.	MAX.
118X11E	2.40	3.00	2.40	3.00

NOTES:
1. JEDEC OUTLINE :
   STANDARD : MO-153 AB REV.F
   THERMALLY ENHANCED : MO-153 ABT REV.F
2. DIMENSION 'D' DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
3. DIMENSION 'E1' DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
4. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE 'b' DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07 MM.
5. DIMENSIONS 'D' AND 'E1' TO BE DETERMINED AT DATUM PLANE H .