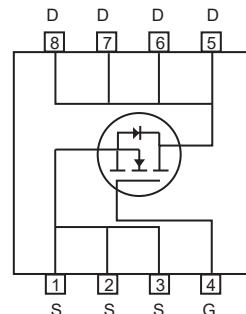
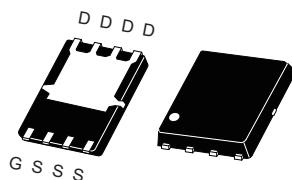


## N-Channel Enhancement Mode Field Effect Transistor

### FEATURES

- 30V, 255A,  $R_{DS(ON)} = 1 \text{ m}\Omega$  @ $V_{GS} = 10\text{V}$ .  
 $R_{DS(ON)} = 1.4 \text{ m}\Omega$  @ $V_{GS} = 4.5\text{V}$ .
- Super high dense cell design for extremely low  $R_{DS(ON)}$ .
- High power and current handing capability.
- RoHS compliant.
- Surface mount Package.



P-PAK 5X6

### ABSOLUTE MAXIMUM RATINGS $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Limit	Units
Drain-Source Voltage	$V_{DS}$	30	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D @ R_{0JC}$	255	A
	$I_D @ R_{0JA}$	65	A
Drain Current-Pulsed <sup>a</sup>	$I_{DM} @ R_{0JC}$	1020	A
	$I_{DM} @ R_{0JA}$	260	A
Maximum Power Dissipation	$P_D$	98	W
Single Pulsed Avalanche Energy <sup>e</sup>	$E_{AS}$	375	mJ
Single Pulsed Avalanche Current <sup>e</sup>	$I_{AS}$	50	A
Operating and Store Temperature Range	$T_J, T_{stg}$	-55 to 150	$^\circ\text{C}$

### Thermal Characteristics

Parameter	Symbol	Limit	Units
Thermal Resistance, Junction-to-Case	$R_{0JC}$	1.28	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Ambient <sup>b</sup>	$R_{0JA}$	20	$^\circ\text{C/W}$

Details are subject to change without notice.

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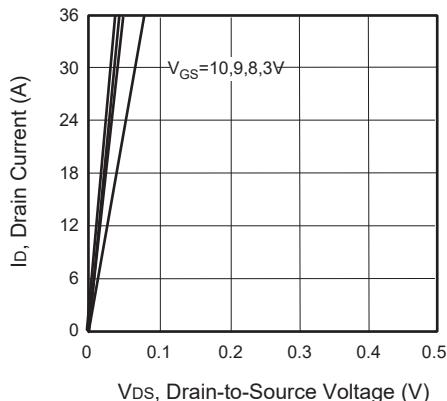
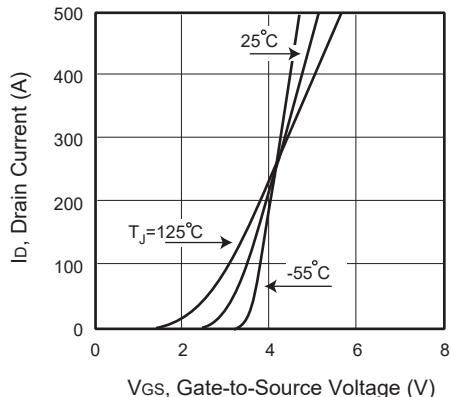
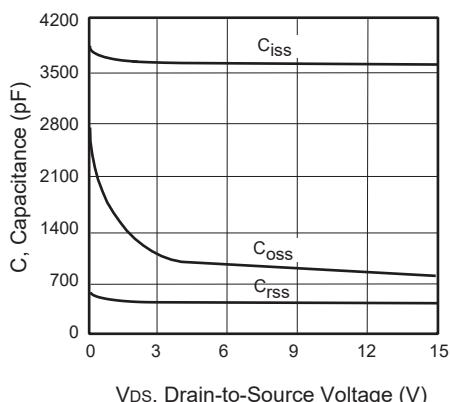
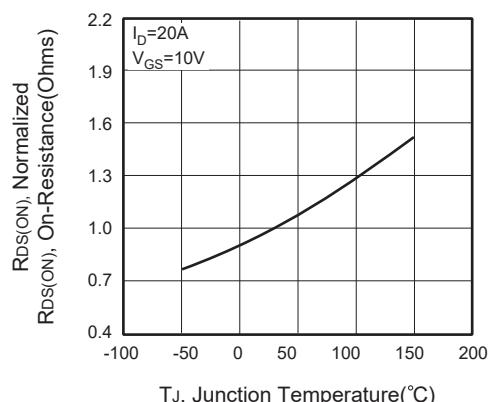
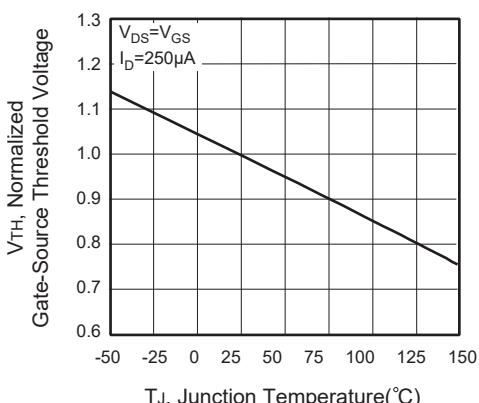
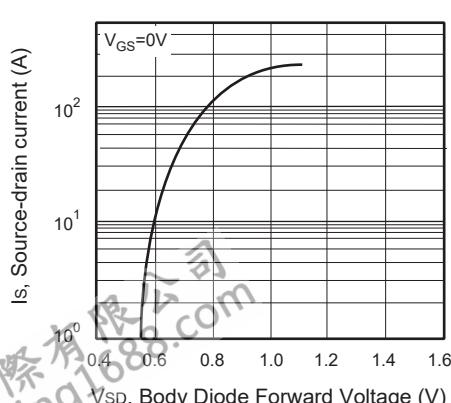
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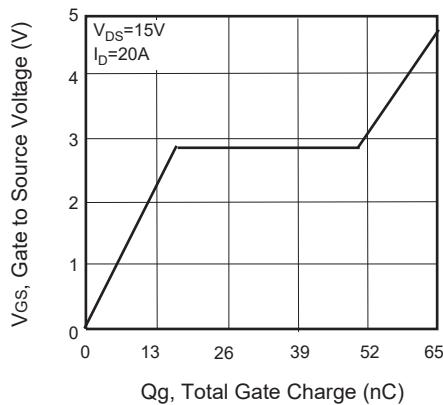
**Electrical Characteristics**  $T_C = 25^\circ\text{C}$  unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$\text{BV}_{\text{DSS}}$	$V_{\text{GS}} = 0\text{V}, I_D = 250\mu\text{A}$	30			V
Zero Gate Voltage Drain Current	$I_{\text{DSS}}$	$V_{\text{DS}} = 30\text{V}, V_{\text{GS}} = 0\text{V}$			1	$\mu\text{A}$
Gate Body Leakage Current, Forward	$I_{\text{GSSF}}$	$V_{\text{GS}} = 20\text{V}, V_{\text{DS}} = 0\text{V}$			100	nA
Gate Body Leakage Current, Reverse	$I_{\text{GSSR}}$	$V_{\text{GS}} = -20\text{V}, V_{\text{DS}} = 0\text{V}$			-100	nA
<b>On Characteristics</b> <sup>c</sup>						
Gate Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{GS}} = V_{\text{DS}}, I_D = 250\mu\text{A}$	1		2	V
Static Drain-Source On-Resistance	$R_{\text{DS}(\text{on})}$	$V_{\text{GS}} = 10\text{V}, I_D = 20\text{A}$		0.85	1	$\text{m}\Omega$
		$V_{\text{GS}} = 4.5\text{V}, I_D = 15\text{A}$		1.1	1.4	$\text{m}\Omega$
<b>Dynamic Characteristics</b> <sup>d</sup>						
Input Capacitance	$C_{\text{iss}}$	$V_{\text{DS}} = 15\text{V}, V_{\text{GS}} = 0\text{V}, f = 1.0 \text{ MHz}$		3660		pF
Output Capacitance	$C_{\text{oss}}$			910		pF
Reverse Transfer Capacitance	$C_{\text{rss}}$			410		pF
<b>Switching Characteristics</b> <sup>d</sup>						
Turn-On Delay Time	$t_{\text{d}(\text{on})}$	$V_{\text{DD}} = 15\text{V}, I_D = 1\text{A}, V_{\text{GS}} = 10\text{V}, R_{\text{GEN}} = 6\Omega$		37		ns
Turn-On Rise Time	$t_r$			30		ns
Turn-Off Delay Time	$t_{\text{d}(\text{off})}$			391		ns
Turn-Off Fall Time	$t_f$			149		ns
Total Gate Charge	$Q_g$	$V_{\text{DS}} = 15\text{V}, I_D = 20\text{A}, V_{\text{GS}} = 4.5\text{V}$		64		nC
Gate-Source Charge	$Q_{\text{gs}}$			17		nC
Gate-Drain Charge	$Q_{\text{gd}}$			34		nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
Drain-Source Diode Forward Current <sup>b</sup>	$I_S$				89	A
Drain-Source Diode Forward Voltage <sup>c</sup>	$V_{\text{SD}}$	$V_{\text{GS}} = 0\text{V}, I_S = 10\text{A}$			1.1	V

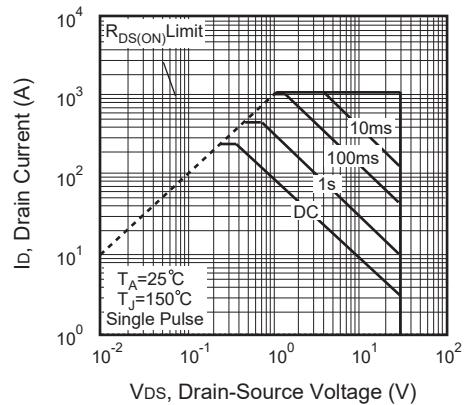
## Notes :

- a.Repetitive Rating : Pulse width limited by maximum junction temperature.
- b.Surface Mounted on FR4 Board,  $t \leq 10$  sec.
- c.Pulse Test : Pulse Width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 2\%$ .
- d.Guaranteed by design, not subject to production testing.  
e.L = 0.3mH,  $I_{AS} = 50\text{A}$ ,  $V_{DD} = 24\text{V}$ ,  $R_G = 25\Omega$ , Starting  $T_J = 25^\circ\text{C}$ .

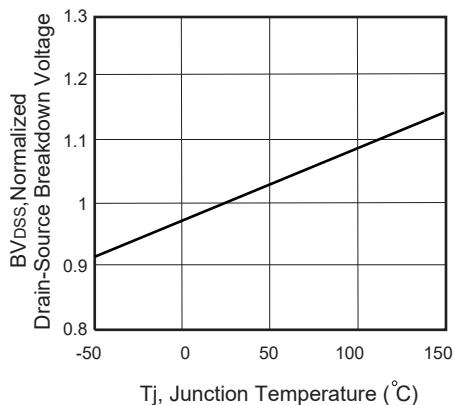
**Figure 1. Output Characteristics****Figure 2. Transfer Characteristics****Figure 3. Capacitance****Figure 4. On-Resistance Variation with Temperature****Figure 5. Gate Threshold Variation with Temperature****Figure 6. Body Diode Forward Voltage Variation with Source Current**



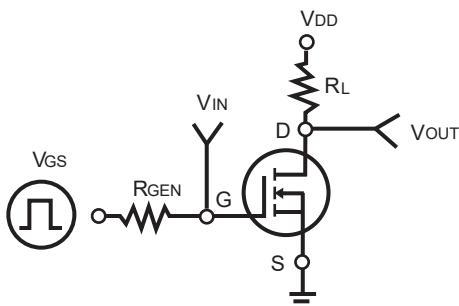
**Figure 7. Gate Charge**



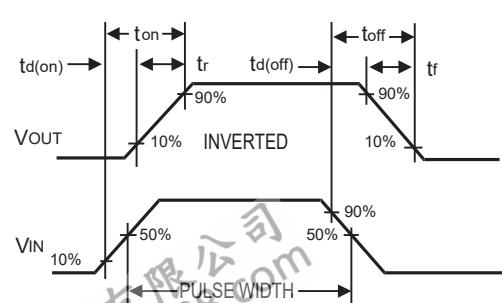
**Figure 8. Maximum Safe Operating Area**



**Figure 9. Breakdown Voltage Variation VS Temperature**



**Figure 10. Switching Test Circuit**



**Figure 11. Switching Waveforms**

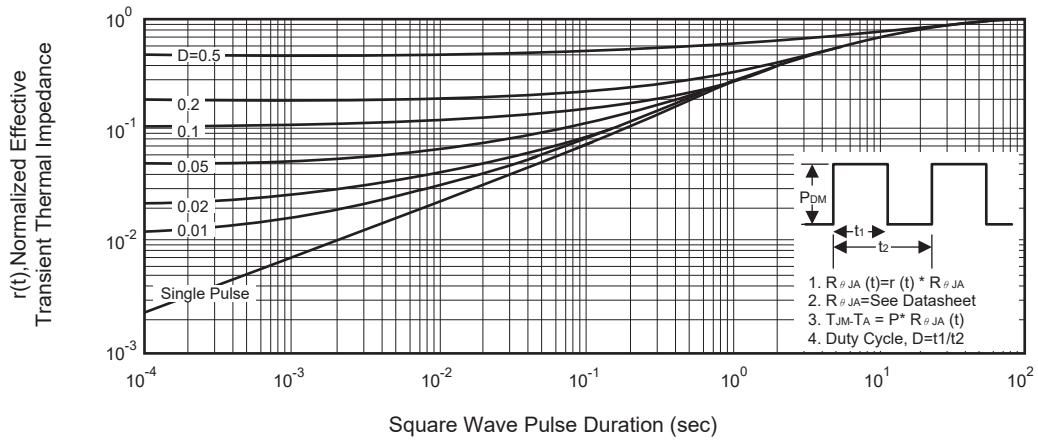


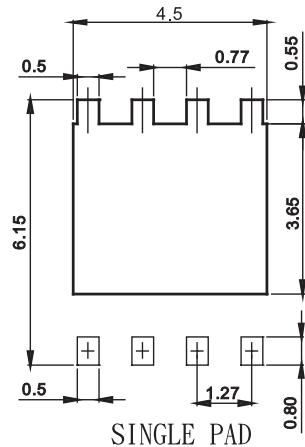
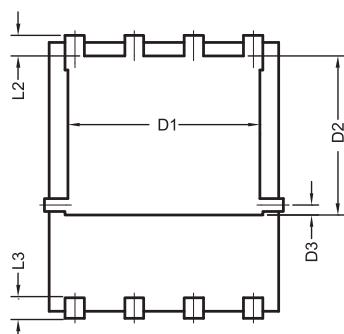
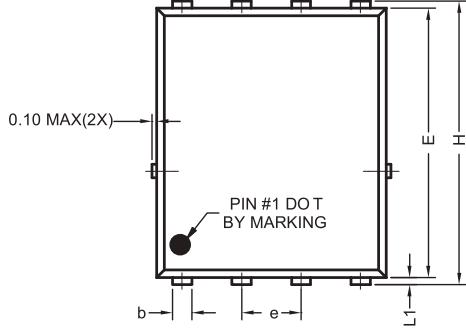
Figure 12. Normalized Thermal Transient Impedance Curve



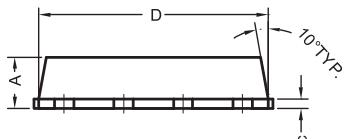
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## P-PAK5X6 產品外觀尺寸圖 (Product Outline Dimension)

### SINGLE PAD 尺寸圖



RECOMMENDED LAND PATTERN



SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.800	1.170	0.031	0.046
b	0.340	0.490	0.013	0.019
c	0.20	0.34	0.008	0.013
D	4.800	5.100	0.009	0.011
D1	3.800	4.200	0.150	0.165
D2	3.180	3.78	0.125	0.149
D3	0.150	0.360	0.006	0.0142
E	5.650	5.900	0.222	0.232
e	1.270 TYP		0.050 TYP	
H	5.900	6.150	0.232	0.242
L1	0.050	0.250	0.002	0.010
L2	0.380	0.620	0.015	0.024
L3	0.380	0.800	0.015	0.031