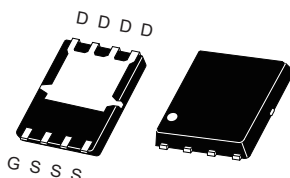


N-Channel Enhancement Mode Field Effect Transistor

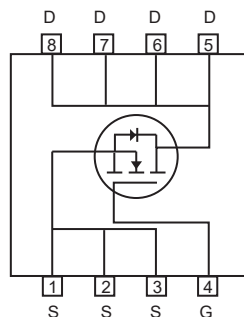
PRELIMINARY

FEATURES

- 100V, 55A, $R_{DS(ON)} = 12m\Omega$ @ $V_{GS} = 10V$.
- Super high dense cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability.
- RoHS compliant.
- Surface mount Package.



P-PAK 5X6



ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Limit	Units
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	$I_D @ R_{\theta JC}$	55	A
Drain Current-Continuous	$I_D @ R_{\theta JA}$	16	A
Drain Current-Pulsed ^a	$I_{DM} @ R_{\theta JC}$	200	A
Drain Current-Pulsed ^a	$I_{DM} @ R_{\theta JA}$	64	A
Maximum Power Dissipation	P_D	69	W
Single Pulsed Avalanche Energy ^e	E_{AS}	73	mJ
Single Pulsed Avalanche Current ^e	I_{AS}	22	A
Operating and Store Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Limit	Units
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.8	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Ambient ^b	$R_{\theta JA}$	20	$^\circ\text{C/W}$

This is preliminary information on a new product in development now .
Details are subject to change without notice .

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Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0V, I_D = 250\mu A$	100			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 100V, V_{GS} = 0V$			1	μA
Gate Body Leakage Current, Forward	I_{GSSF}	$V_{GS} = 20V, V_{DS} = 0V$			100	nA
Gate Body Leakage Current, Reverse	I_{GSSR}	$V_{GS} = -20V, V_{DS} = 0V$			-100	nA
On Characteristics ^c						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 250\mu A$	2		4	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 20A$		9.5	12	m Ω
Dynamic Characteristics ^d						
Input Capacitance	C_{iss}	$V_{DS} = 50V, V_{GS} = 0V, f = 1.0\text{ MHz}$		--		pF
Output Capacitance	C_{oss}			--		pF
Reverse Transfer Capacitance	C_{rss}			--		pF
Switching Characteristics ^d						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 50V, I_D = 20A, V_{GS} = 10V, R_{GEN} = 6\Omega$		--		ns
Turn-On Rise Time	t_r			--		ns
Turn-Off Delay Time	$t_{d(off)}$			--		ns
Turn-Off Fall Time	t_f			--		ns
Total Gate Charge	Q_g	$V_{DS} = 50V, I_D = 20A, V_{GS} = 10V$		--		nC
Gate-Source Charge	Q_{gs}			--		nC
Gate-Drain Charge	Q_{gd}			--		nC
Drain-Source Diode Characteristics and Maximum Ratings						
Drain-Source Diode Forward Current ^b	I_S				55	A
Drain-Source Diode Forward Voltage ^c	V_{SD}	$V_{GS} = 0V, I_S = 20A$			1.2	V
Notes : a.Repetitive Rating : Pulse width limited by maximum junction temperature. b.Surface Mounted on FR4 Board, $t \leq 10\text{ sec}$. c.Pulse Test : Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$. d.Guaranteed by design, not subject to production testing. e.L = 0.3mH, $I_{AS} = 22A, V_{DD} = 50V, R_G = 25\Omega$, Starting $T_J = 25^\circ C$.						