



LP2950/2951

LINEAR INTEGRATED CIRCUIT

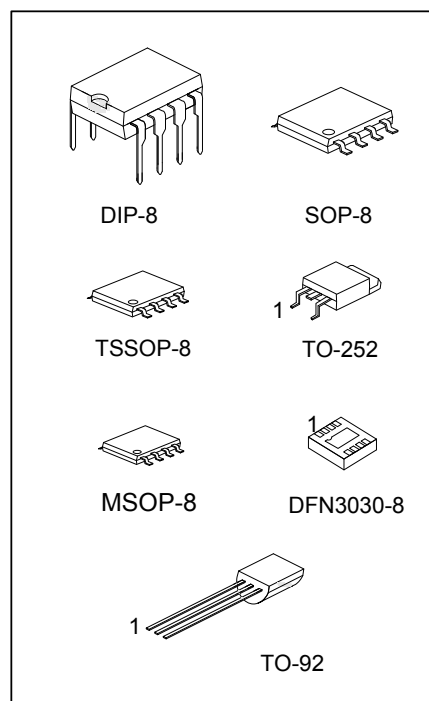
100 mA LOW-DROPOUT
VOLTAGE REGULATOR

■ DESCRIPTION

The UTC LP2950/2951 are monolithic integrated voltage regulators with low dropout voltage, and low quiescent current. It includes many features that suitable for different applications.

■ FEATURES

- * Fixed output versions, 2.5V, 3.0V, 3.3V, 3.6V and 5.0V, are available
- * High accuracy output voltage
- * Extremely low quiescent current and dropout voltage
- * Extremely tight load and line regulation
- * Current and thermal limiting
- * Very low temperature coefficient
- * Logic controlled shutdown and err flog available for 8 pin package
- * Output voltage programmable for LP2951



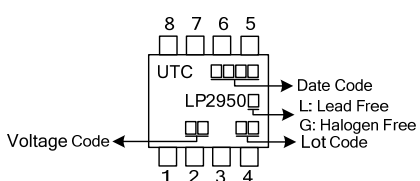
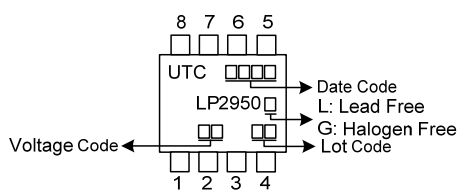
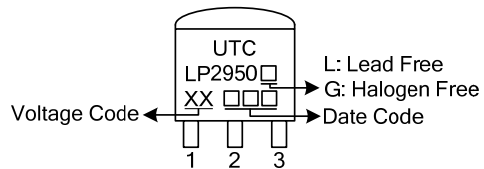
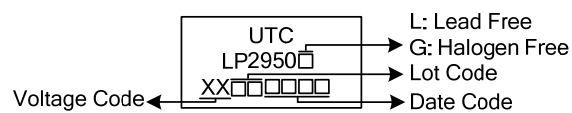
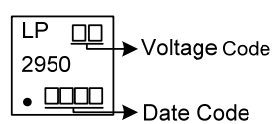
■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
LP2950L-xx-D08-T	LP2950G-xx-D08-T	DIP-8	Tube
LP2950L-xx-S08-R	LP2950G-xx-S08-R	SOP-8	Tape Reel
LP2950L-xx-T92-B	LP2950G-xx-T92-B	TO-92	Tape Box
LP2950L-xx-T92-K	LP2950G-xx-T92-K	TO-92	Bulk
LP2950L-xx-TN3-R	LP2950G-xx-TN3-R	TO-252	Tape Reel
LP2950L-xx-K08-3030-R	LP2950G-xx-K08-3030-R	DFN3030-8	Tape Reel
LP2951L-D08-T	LP2951G-D08-T	DIP-8	Tube
LP2951L-S08-R	LP2951G-S08-R	SOP-8	Tape Reel
LP2951L-SM1-R	LP2951G-SM1-R	MSOP-8	Tape Reel
LP2951L-P08-R	LP2951G-P08-R	TSSOP-8	Tape Reel
LP2951L-K08-3030-R	LP2951G-K08-3030-R	DFN3030-8	Tape Reel

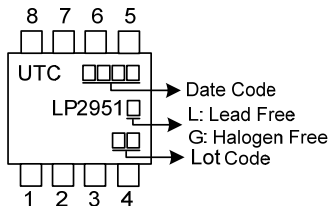
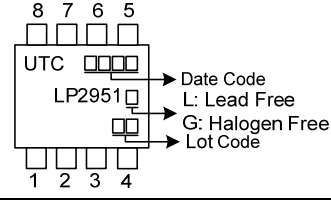
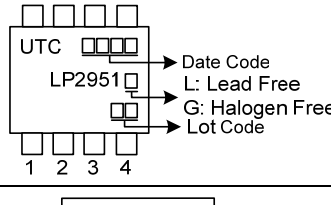
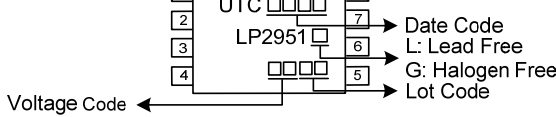
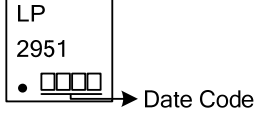
Note: Pin Assignment: I: V_{IN} O: V_{OUT} G: GND

LP2950G-xx-D08-T	(1) Packing Type (2) Package Type (3) Output Voltage Code (4) Green Package	(1) T: Tube, B: Tape Box, K: Bulk, R: Tape Reel (2) D08: DIP-8, S08: SOP-8, SM1: MSOP-8, P08: TSSOP-8, TN3: TO-252, T92: TO-92, K08-3030: DFN3030-8 (3) xx: refer to Output Voltage Code (4) G: Halogen Free and Lead Free, L: Lead Free
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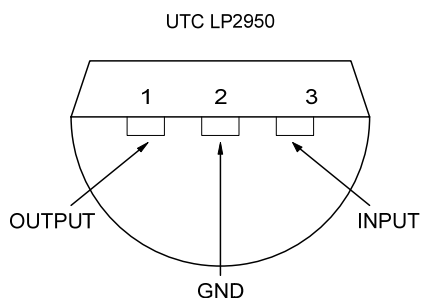
MARKING INFORMATION (For LP2950)

PACKAGE	VOLTAGE CODE	MARKING
DIP-8	25: 2.5V 30: 3.0V 33: 3.3V 36: 3.6V 50: 5.0V	
SOP-8		
TO-92		
TO-252		
DFN3030-8		

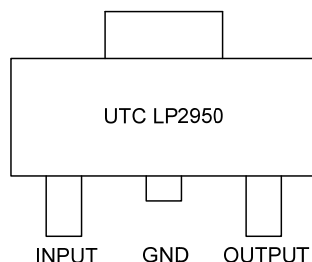
MARKING INFORMATION (For LP2951)

PACKAGE	MARKING
DIP-8	 Diagram showing the marking layout for the DIP-8 package. The top row of pins (8, 7, 6, 5) contains the UTC logo and a four-digit date code. The bottom row of pins (1, 2, 3, 4) contains the LP2951 part number and a two-digit lot code. Arrows indicate the following: Date Code (from the four-digit code), L: Lead Free (from the 'L' in LP2951), G: Halogen Free (from the 'G' in LP2951), and Lot Code (from the two-digit code).
SOP-8	 Diagram showing the marking layout for the SOP-8 package. The top row of pins (8, 7, 6, 5) contains the UTC logo and a four-digit date code. The bottom row of pins (1, 2, 3, 4) contains the LP2951 part number and a two-digit lot code. Arrows indicate the following: Date Code (from the four-digit code), L: Lead Free (from the 'L' in LP2951), G: Halogen Free (from the 'G' in LP2951), and Lot Code (from the two-digit code).
MSOP-8	 Diagram showing the marking layout for the MSOP-8 package. The top row of pins (8, 7, 6, 5) contains the UTC logo and a four-digit date code. The bottom row of pins (1, 2, 3, 4) contains the LP2951 part number and a two-digit lot code. Arrows indicate the following: Date Code (from the four-digit code), L: Lead Free (from the 'L' in LP2951), G: Halogen Free (from the 'G' in LP2951), and Lot Code (from the two-digit code).
TSSOP-8	 Diagram showing the marking layout for the TSSOP-8 package. The top row of pins (8, 7, 6, 5) contains the UTC logo and a four-digit date code. The bottom row of pins (1, 2, 3, 4) contains the LP2951 part number and a two-digit lot code. Arrows indicate the following: Date Code (from the four-digit code), L: Lead Free (from the 'L' in LP2951), G: Halogen Free (from the 'G' in LP2951), Lot Code (from the two-digit code), and Voltage Code (from the 'V' in LP2951).
DFN3030-8	 Diagram showing the marking layout for the DFN3030-8 package. The top row of pins (8, 7, 6, 5) contains the LP logo and a four-digit date code. The bottom row of pins (1, 2, 3, 4) contains the 2951 part number and a two-digit lot code. Arrows indicate the following: Date Code (from the four-digit code), L: Lead Free (from the 'L' in LP2951), G: Halogen Free (from the 'G' in LP2951), and Lot Code (from the two-digit code).

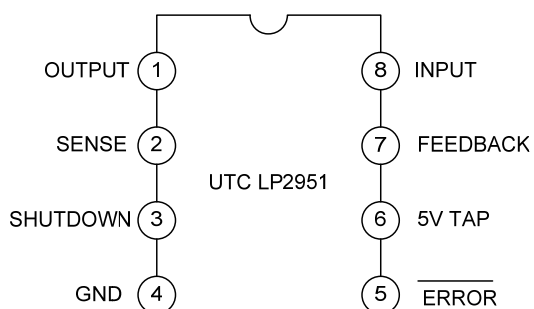
PIN CONFIGURATIONS



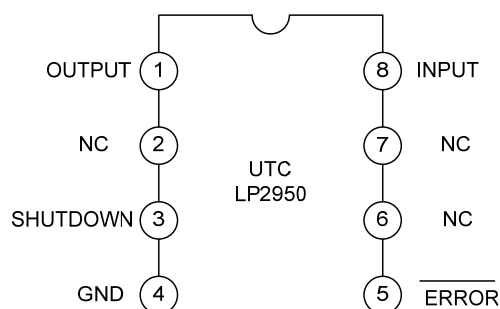
TO-92 Plastic Package Bottom View



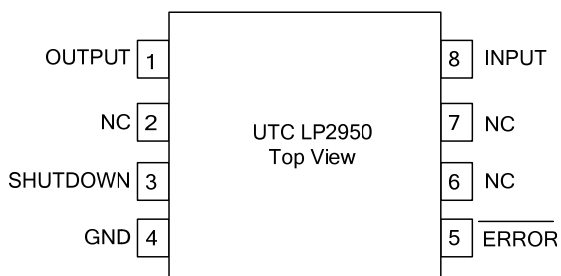
SOT-252 Package



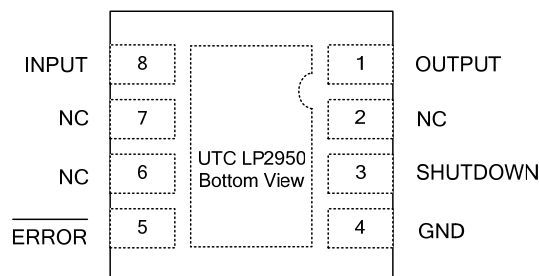
SOP-8, DIP-8 or TSSOP-8 Package
For UTC LP2951



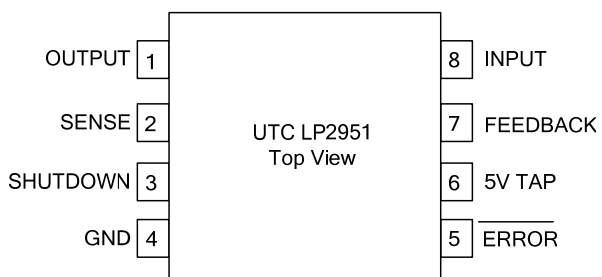
SOP-8 or DIP-8 Package For UTC
LP2950



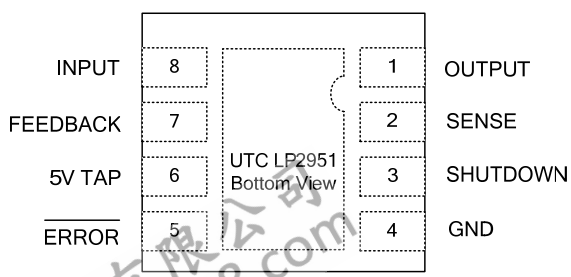
DFN3030-8 Plastic Package Top View



DFN3030-8 Plastic Package Bottom View



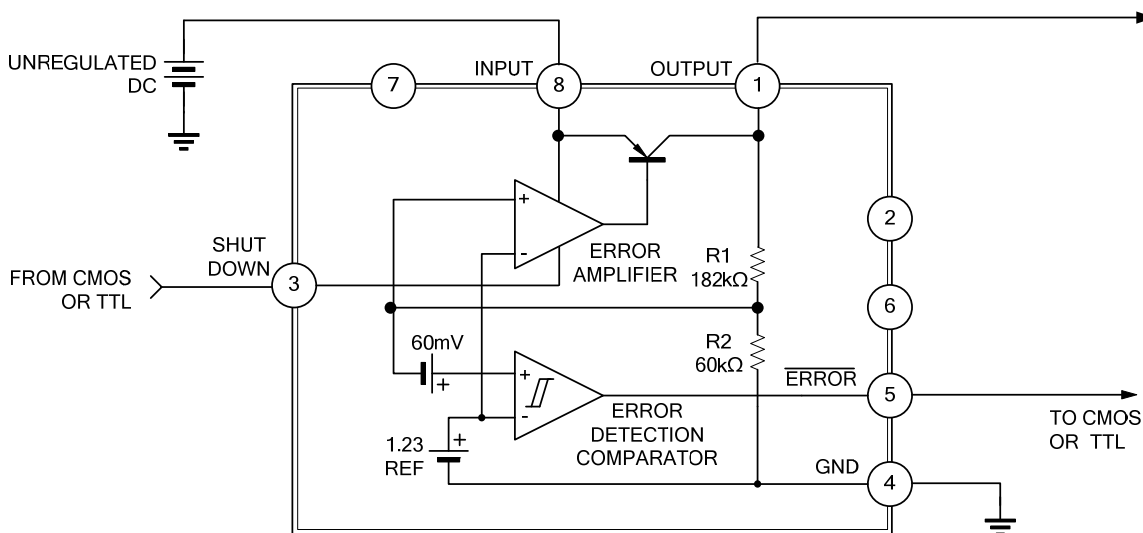
DFN3030-8 Plastic Package Top View



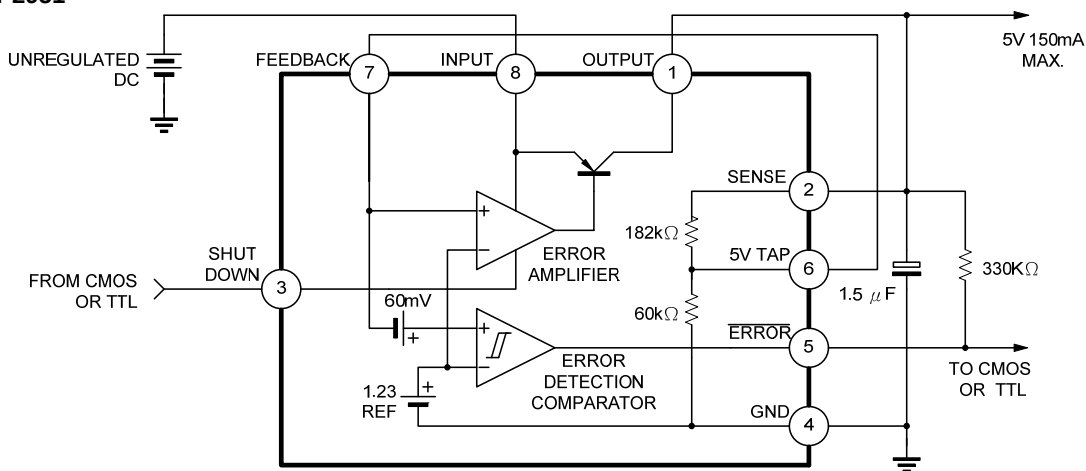
DFN3030-8 Plastic Package Bottom View

■ BLOCK DIAGRAM

FOR LP2950



FOR LP2951



■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.3 ~ +30	V
Feedback Voltage	V_{FB}	-1.5 ~ +30	V
Shutdown Voltage	V_{SHDN}	-0.3 ~ +30	V
Power Dissipation	P_D	Internally Limited	W
Operation Junction Temperature	T_J	-40 ~ +125	°C
Storage Temperature	T_{STG}	-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

PARAMETER	SYMBOL	RATING	UNIT
Junction-to-Ambient	TO-92	180	°C/W
	TO-252	92	
	TSSOP-8	150	
	MSOP-8	190	
	SOP-8	143	
	DIP-8	105	
	DFN3030-8	64 (Note)	
Junction-to-Case	TO-92	83	°C/W
	TO-252	6	
	TSSOP-8	50	
	MSOP-8	55	
	SOP-8/DIP-8	45	
	DFN3030-8	9 (Note)	

Note: The data tested by surface mounted on a 2 inch² FR-4 board with 2OZ copper.

■ ELECTRICAL CHARACTERISTICS ($T_J=25^{\circ}\text{C}$, $V_{IN}=6\text{V}$, $I_L=100\mu\text{A}$, $C_L=1\mu\text{F}$, unless otherwise specified.)

For All Version:

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Output Voltage	V_{OUT}	$T_J=25^{\circ}\text{C}$ (Note 1)	$V_{OUT}\times 0.98$	V_{OUT}	$V_{OUT}\times 1.02$	V
Output Voltage	V_{OUT}	$100\mu\text{A}\leq I_L\leq 100\text{mA}$, $T_J\leq T_J(\text{max})$	$V_{OUT}\times 0.98$	V_{OUT}	$V_{OUT}\times 1.02$	V
Output Voltage Temperature Coefficient	TcV_o		20		100	ppm/°C
Line Regulation	ΔV_{OUT}	$6\text{V}\leq V_{IN}\leq 30\text{V}$	0.03	0.1	0.2	%
Load Regulation	ΔV_{OUT}	$100\mu\text{A}\leq I_L\leq 100\text{mA}$	0.04	0.1	0.2	%
Dropout Voltage	V_D	$I_L=100\mu\text{A}$	50	80	150	mV
		$I_L=100\text{mA}$ (Note 2)	380	450	600	
Ground Current	I_G	$I_L=100\mu\text{A}$		120	140	μA
		$I_L=100\text{mA}$		12	14	
Dropout Ground Current		$V_{IN}=4.5\text{V}$, $I_L=100\mu\text{A}$		170	200	μA
Current Limit	I_{LIMIT}	$V_{OUT}=0$	130	190	250	mA
Output Noise (10Hz ~ 100KHz) (Bypass=0.01 μF pins 7 to 1 (LP2951))	eN	$C_L=1\mu\text{F}$			430	μV
		$C_L=200\mu\text{F}$			160	
		$C_L=3.3\mu\text{F}$			100	

■ ELECTRICAL CHARACTERISTICS(Cont.)

For UTC LP2950 8-Pin Version Only

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Error Comparator						
Output Leakage Current	$I_{O(LEAK)}$	$V_{OH}=30V$			1	μA
Output Low Voltage	V_{OL}	$V_{IN}=4.5V, I_{OL}=400\mu A$			280	mV
Threshold Voltage	Upper	V_{THU} (Note 3)	3.2			%VO
	Lower	V_{THL} (Note 3)			7.6	%VO
Hysteresis	V_{HYS}	(Note 3)		15		mV
Shutdown Input						
Input Logic Voltage	Low	V_{IL} Regulator ON			0.70	V
	High	V_{IH} Regulator OFF	2.0			
Shutdown Pin Input Current	I_{SHDN}	$V_{SHDN}=2.4V$		30	50	μA
		$V_{SHDN}=30V$		450	600	μA
Regulator Output Current Shutdown	I_{DFF}	$V_{SHDN} \geq 2V, V_{IN} \leq 30V, V_{OUT}=0$ Feedback pin tied to 5V Tap.		3	10	μA

For UTC LP2951 8-Pin Version Only

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Reference Voltage	V_{REF}		1.22	1.235	1.25	V
Reference Voltage	V_{REF}	Over temperature(Note 4)	1.19		1.27	V
Feedback pin Bias Current	I_{FB}			20	40	nA
Reference Voltage Temperature Coefficient	$V_{REF(TC)}$			50		ppm/°C
Feedback Bias Current Temperature Coefficient	$I_{FB(TC)}$			0.1		nA/°C
Error Comparator						
Output Leakage Current	$I_{O(LEAK)}$	$V_{OH}=30V$			1	μA
Output Low Voltage	V_{OL}	$V_{IN}=4.5V, I_{OL}=400\mu A$			250	mV
Threshold Voltage	Upper	V_{THU} (Note 3)	3.2			%VO
	Lower	V_{THL} (Note 3)			7.6	%VO
Hysteresis	V_{HYS}	(Note 3)		15		mV
Shutdown Input						
Input Logic Voltage	Low	V_{IL} Regulator ON			0.70	V
	High	V_{IH} Regulator OFF	2.0			
Shutdown Pin Input Current	I_{SHDN}	$V_{SHDN}=2.4V$		30	50	μA
		$V_{SHDN}=30V$		450	600	μA
Regulator Output Current Shutdown	I_{DFF}	$V_{SHDN} \geq 2V, V_{IN} \leq 30V, V_{OUT}=0$ Feedback pin tied to 5V Tap.		3	10	μA

Note: 1. Additional conditions for 8-pin versions are FB pin tied to 5V_{TAP}, Output tied to Sense ($V_{OUT}=5V$) and $V_{SHDN} \leq 0.8V$.

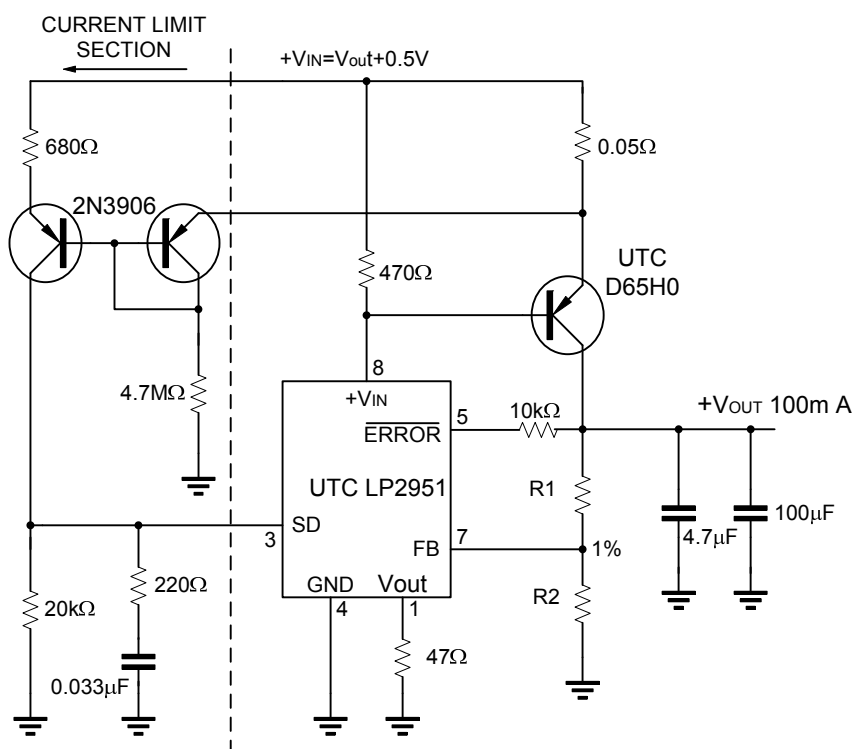
2. Dropout Voltage is defined as the input to output differential at which the output voltage drops 100mV below its nominal value measured at 1V differential.

3. Comparator thresholds are expressed in terms of percentage value of voltage output.

4. $V_{REF} \leq V_{OUT} \leq (V_{IN}-1V)$, $2.3V \leq V_{IN} \leq 30V$, $100\mu A \leq I_L \leq 100mA$, $T_J \leq T_{J(MAX)}$

■ TYPICAL APPLICATION CIRCUIT

10 Ampere Low Dropout Regulator



$$V_{OUT} = 1.23V * (1 + R1/R2)$$

For 5V output use internal resistors. Wire pin 6 to 7 and wire pin 2 to +Vout

Fig.1

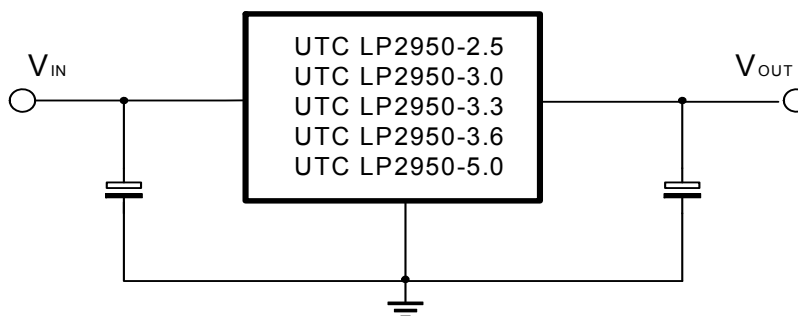


Fig.2

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