

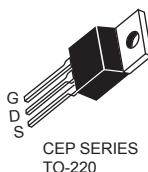
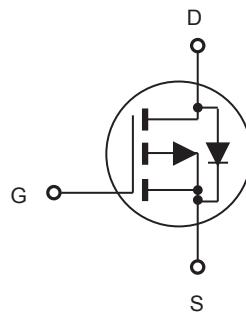


# CEP35P10/CEB35P10 CEF35P10

## P-Channel Enhancement Mode Field Effect Transistor

### FEATURES

- -100V, -32A,  $R_{DS(ON)} = 76\text{m}\Omega$  @ $V_{GS} = -10\text{V}$ .  
 $R_{DS(ON)} = 92\text{m}\Omega$  @ $V_{GS} = -4.5\text{V}$ .
- Super high dense cell design for extremely low  $R_{DS(ON)}$ .
- High power and current handing capability.
- Lead-free plating ; RoHS compliant.
- TO-220 & TO-263 package.

CEB SERIES  
TO-263(DD-PAK)CEP SERIES  
TO-220

### ABSOLUTE MAXIMUM RATINGS $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Limit	Units
Drain-Source Voltage	$V_{DS}$	-100	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	-32	A
Drain Current-Pulsed <sup>a</sup>	$I_{DM}$	-128	A
Maximum Power Dissipation @ $T_C = 25^\circ\text{C}$ - Derate above $25^\circ\text{C}$	$P_D$	125 0.83	W W/ $^\circ\text{C}$
Single Pulsed Avalanche Energy <sup>e</sup>	$E_{AS}$	450	mJ
Single Pulsed Avalanche Current <sup>e</sup>	$I_{AS}$	30	A
Operating and Store Temperature Range	$T_J, T_{Stg}$	-55 to 175	$^\circ\text{C}$

### Thermal Characteristics

Parameter	Symbol	Limit	Units
Thermal Resistance, Junction-to-Case	$R_{JC}$	1.2	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Ambient	$R_{JA}$	62.5	$^\circ\text{C/W}$



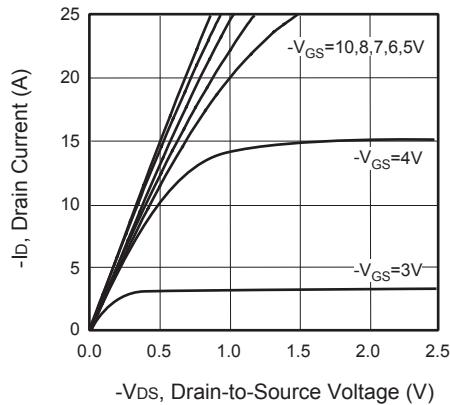
# CEP35P10/CEB35P10 CEF35P10

## Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

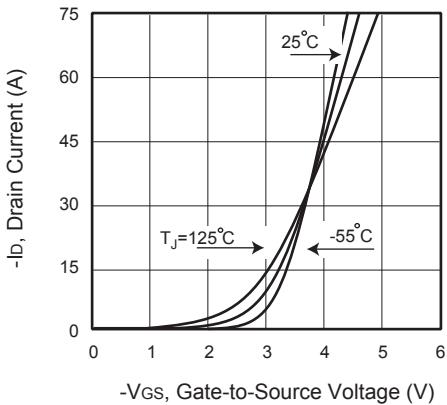
Parameter	Symbol	Test Condition	Min	Typ	Max	Units
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$\text{BV}_{\text{DSS}}$	$V_{\text{GS}} = 0\text{V}, I_D = -250\mu\text{A}$	-100			V
Zero Gate Voltage Drain Current	$I_{\text{DSS}}$	$V_{\text{DS}} = -100\text{V}, V_{\text{GS}} = 0\text{V}$			-1	$\mu\text{A}$
Gate Body Leakage Current, Forward	$I_{\text{GSSF}}$	$V_{\text{GS}} = 20\text{V}, V_{\text{DS}} = 0\text{V}$			100	nA
Gate Body Leakage Current, Reverse	$I_{\text{GSSR}}$	$V_{\text{GS}} = -20\text{V}, V_{\text{DS}} = 0\text{V}$			-100	nA
<b>On Characteristics<sup>c</sup></b>						
Gate Threshold Voltage	$V_{\text{GS(th)}}$	$V_{\text{GS}} = V_{\text{DS}}, I_D = -250\mu\text{A}$	-1		-3	V
Static Drain-Source On-Resistance	$R_{\text{DS(on)}}$	$V_{\text{GS}} = -10\text{V}, I_D = -16\text{A}$		63	76	$\text{m}\Omega$
		$V_{\text{GS}} = -4.5\text{V}, I_D = -8\text{A}$		72	92	$\text{m}\Omega$
<b>Dynamic Characteristics<sup>d</sup></b>						
Input Capacitance	$C_{\text{iss}}$	$V_{\text{DS}} = -25\text{V}, V_{\text{GS}} = 0\text{V}, f = 1.0 \text{ MHz}$		2590		pF
Output Capacitance	$C_{\text{oss}}$			320		pF
Reverse Transfer Capacitance	$C_{\text{rss}}$			45		pF
<b>Switching Characteristics<sup>d</sup></b>						
Turn-On Delay Time	$t_{\text{d(on)}}$	$V_{\text{DD}} = -50\text{V}, I_D = -18\text{A}, V_{\text{GS}} = -10\text{V}, R_{\text{GEN}} = 3.3\Omega$		17		ns
Turn-On Rise Time	$t_r$			6		ns
Turn-Off Delay Time	$t_{\text{d(off)}}$			75		ns
Turn-Off Fall Time	$t_f$			10		ns
Total Gate Charge	$Q_g$	$V_{\text{DS}} = -80\text{V}, I_D = -18\text{A}, V_{\text{GS}} = -10\text{V}$		75		nC
Gate-Source Charge	$Q_{\text{gs}}$			9		nC
Gate-Drain Charge	$Q_{\text{gd}}$			18		nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
Drain-Source Diode Forward Current <sup>b</sup>	$I_S$				-32	A
Drain-Source Diode Forward Voltage <sup>c</sup>	$V_{\text{SD}}$	$V_{\text{GS}} = 0\text{V}, I_S = -16\text{A}$			-1.2	V

**Notes :**

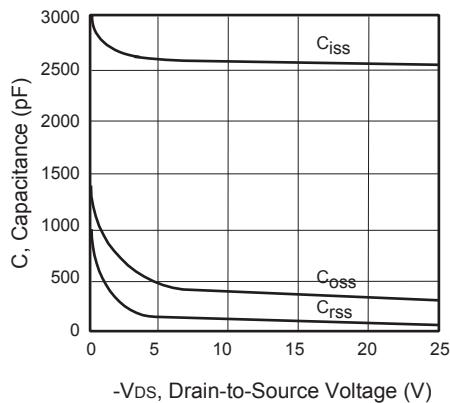
- a.Repetitive Rating : Pulse width limited by maximum junction temperature.□
- b.Surface Mounted on FR4 Board,  $t \leq 10 \text{ sec.}$ □
- c.Pulse Test : Pulse Width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 2\%$ .□
- d.Guaranteed by design, not subject to production testing.□  
e.L = 1mH,  $I_{AS} = 30\text{A}$ ,  $V_{DD} = 25\text{V}$ ,  $R_G = 25\Omega$ , Starting  $T_J = 25^\circ\text{C}$ . □



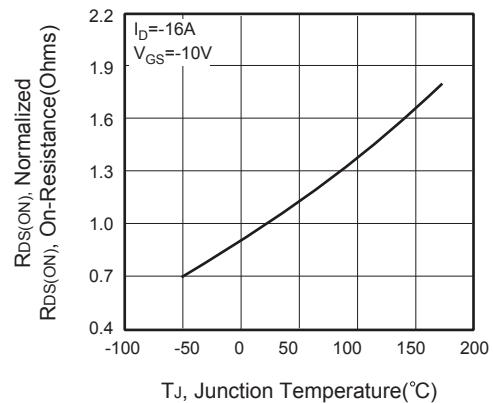
**Figure 1. Output Characteristics**



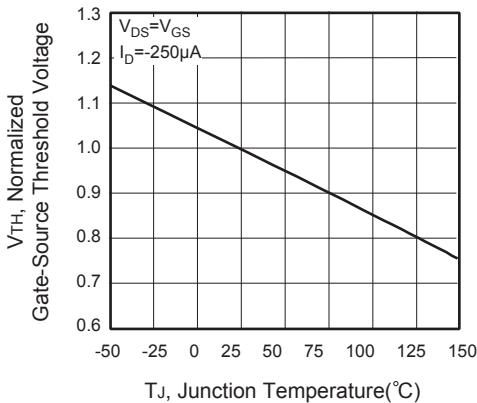
**Figure 2. Transfer Characteristics**



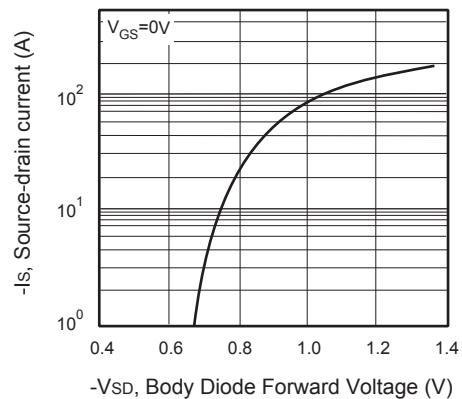
**Figure 3. Capacitance**



**Figure 4. On-Resistance Variation with Temperature**



**Figure 5. Gate Threshold Variation with Temperature**



**Figure 6. Body Diode Forward Voltage Variation with Source Current**

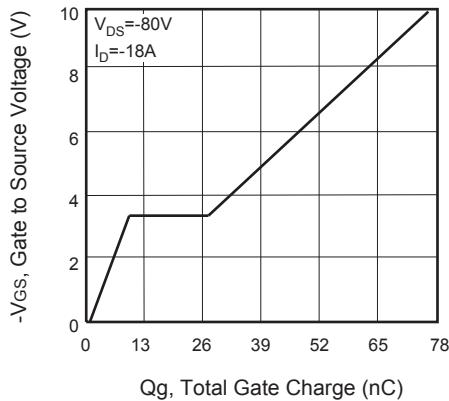


Figure 7. Gate Charge

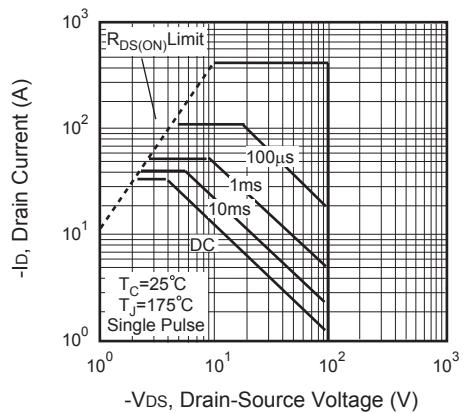


Figure 8. Maximum Safe Operating Area

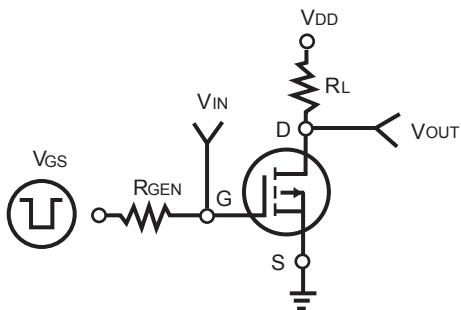


Figure 9. Switching Test Circuit

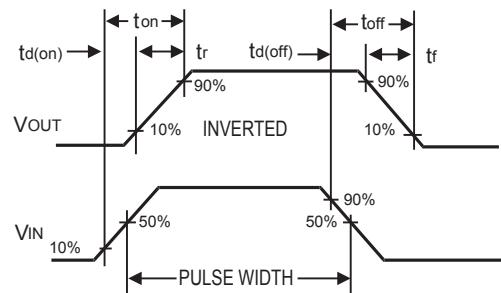


Figure 10. Switching Waveforms

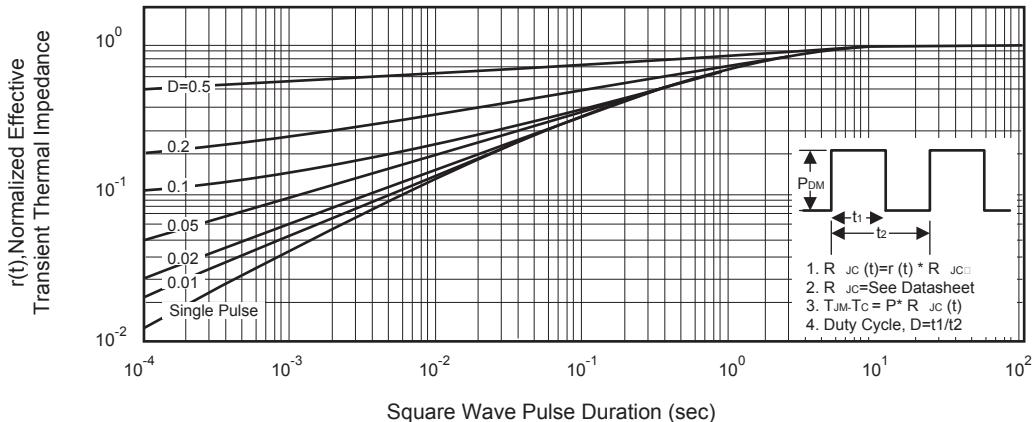


Figure 11. Normalized Thermal Transient Impedance Curve