



12N30

Power MOSFET

12A, 300V N-CHANNEL POWER MOSFET

DESCRIPTION

The UTC **12N30** is an N-channel mode power MOSFET using UTC's advanced technology to provide customers with planar stripe and DMOS technology. This technology specializes in allowing a minimum on-state resistance and superior switching performance. It also can withstand high energy pulse in the avalanche and commutation mode.

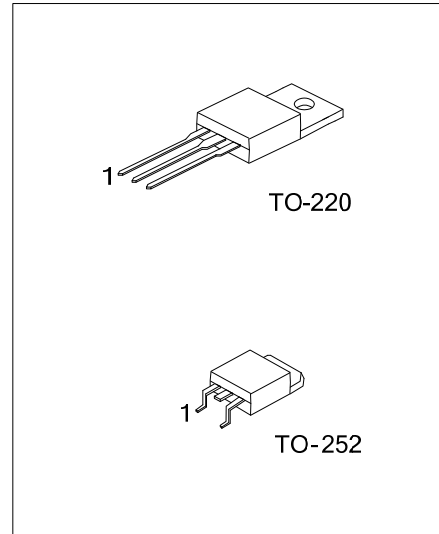
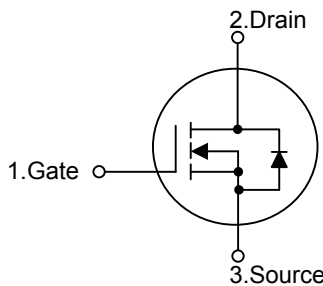
The UTC **12N30** is universally applied in electronic lamp ballast based on half bridge topology and high efficient switched mode power supply.

FEATURES

* $R_{DS(ON)} \leq 0.47\Omega @ V_{GS}=10V, I_D=6.0A$

* High switching speed

SYMBOL



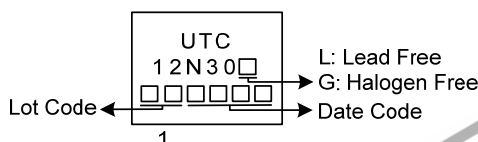
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
12N30L-TA3-T	12N30G-TA3-T	TO-220	G	D	S	Tube
12N30L-TN3-R	12N30G-TN3-R	TO-252	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>12N30G-TA3-T</p> <p>(1) Packing Type (2) Package Type (3) Green Package</p>	<p>(1) T: Tube, R: Tape Reel (2) TA3: TO-220, TN3: TO-252 (3) G: Halogen Free and Lead Free, L: Lead Free</p>
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MARKING



■ ABSOLUTE MAXIMUM RATINGS ($T_c=25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	300	V
Gate-Source Voltage		V_{GSS}	± 20	V
Drain Current	Continuous ($T_c=25^\circ\text{C}$)	I_D	12	A
	Pulsed (Note 2)	I_{DM}	48	A
Single Pulsed Avalanche Energy		E_{AS}	300	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	8	V/ns
Power Dissipation	TO-220	P_D	98	W
	TO-252		83	W
Junction Temperature		T_J	+150	$^\circ\text{C}$
Storage Temperature		T_{STG}	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating : Pulse width limited by maximum junction temperature.

3. $L = 4.1\text{mH}$, $I_{AS} = 12\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$

4. $I_{SD} \leq 12\text{A}$, $di/dt \leq 200\text{A/s}$, $V_{DD} \leq BV_{DSS}$ Starting $T_J = 25^\circ\text{C}$

■ THERMAL CHARACTERISTICS

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient		θ_{JA}	62.5	$^\circ\text{C/W}$
Junction to Case	TO-220	θ_{JC}	1.25	$^\circ\text{C/W}$
	TO-252		1.5 (Note)	$^\circ\text{C/W}$

Note: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

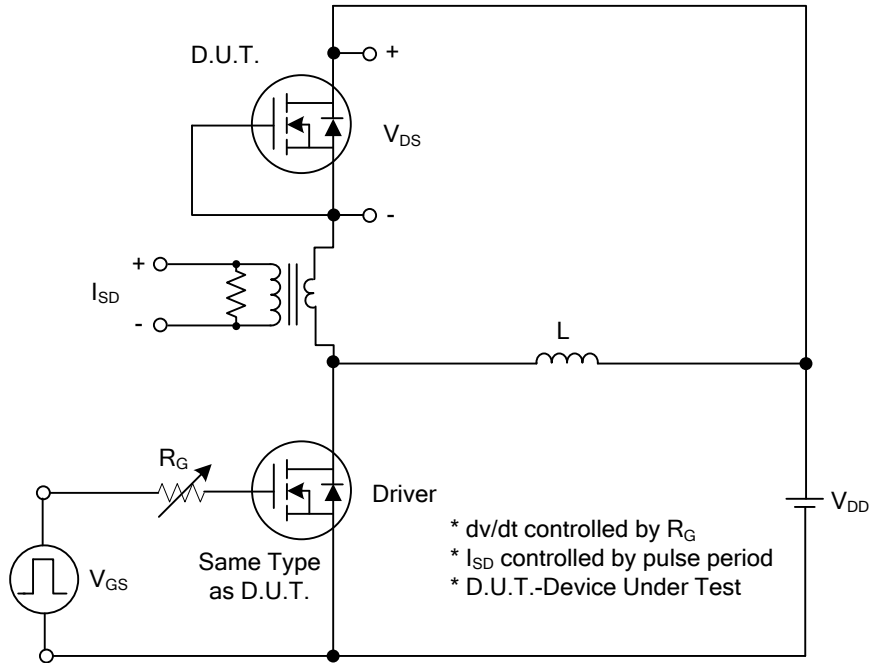
■ ELECTRICAL CHARACTERISTICS ($T_c=25^\circ\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	300			V
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=300\text{V}$, $V_{GS}=0\text{V}$			10	μA
Gate- Source Leakage Current	Forward	I_{GSS}			+100	nA
	Reverse				-100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	2.0		4.0	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=6.0\text{A}$			0.47	Ω
DYNAMIC PARAMETERS						
Input Capacitance	C_{ISS}	$V_{GS}=0\text{V}$, $V_{DS}=25\text{V}$, $f=1.0\text{MHz}$		740		pF
Output Capacitance	C_{OSS}			110		pF
Reverse Transfer Capacitance	C_{RSS}			12		pF
SWITCHING PARAMETERS						
Total Gate Charge	Q_G	$V_{DD}=100\text{V}$, $V_{GS}=10\text{V}$, $I_D=12\text{A}$ $I_G=1\text{mA}$ (Note 1, 2)		19		nC
Gate-Source Charge	Q_{GS}			5		nC
Gate-Drain Charge	Q_{GD}			5.1		nC
Turn-ON Delay Time	$t_{D(ON)}$	$V_{DD}=100\text{V}$, $V_{GS}=10\text{V}$, $I_D=12\text{A}$, $R_G=25\Omega$ (Note 1, 2)		10		ns
Rise Time	t_R			17		ns
Turn-OFF Delay Time	$t_{D(OFF)}$			50		ns
Fall-Time	t_F			19		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Body-Diode Continuous Current	I_S				12	A
Maximum Body-Diode Pulsed Current	I_{SM}				48	A
Drain-Source Diode Forward Voltage	V_{SD}	$I_S=12\text{A}$, $V_{GS}=0\text{V}$			1.4	V
Reverse Recovery Time	t_{rr}	$I_S=12\text{A}$, $V_{GS}=0\text{V}$, $di/dt=100\text{A}/\mu\text{s}$		200		ns
Reverse Recovery Charge	Q_{rr}				1.5	

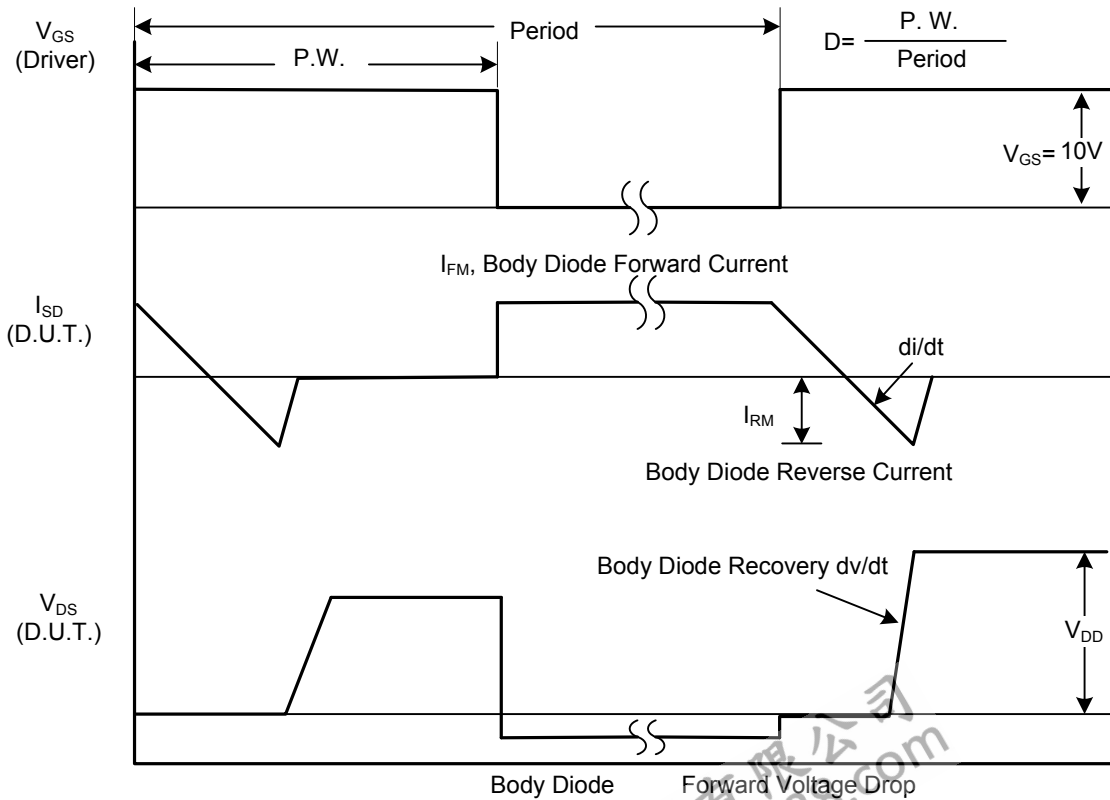
Notes: 1. Pulse Test : Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

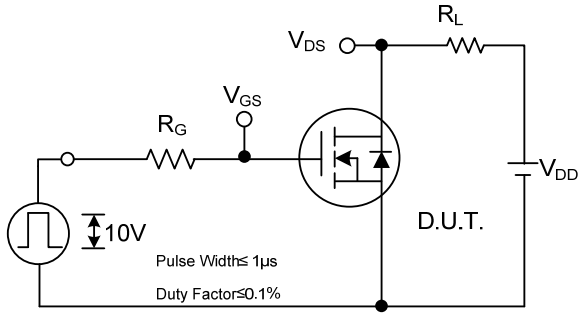


Peak Diode Recovery dv/dt Test Circuit

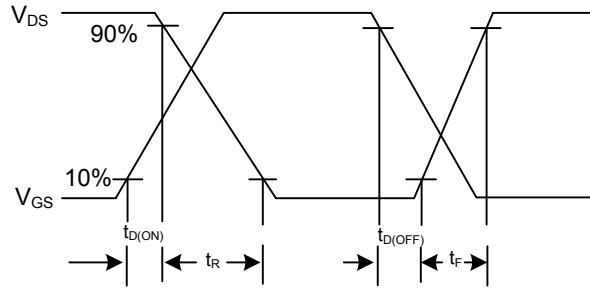


Peak Diode Recovery dv/dt Waveforms

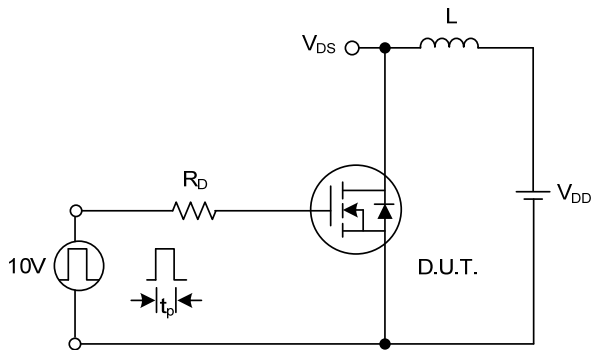
TEST CIRCUITS AND WAVEFORMS



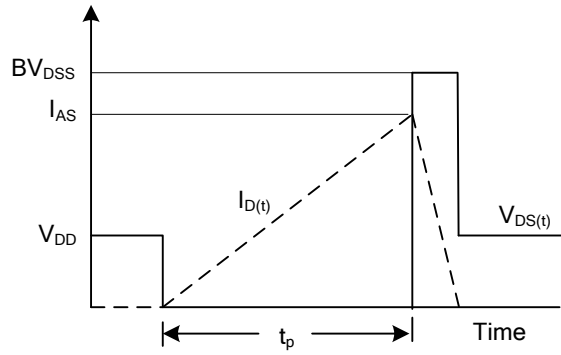
Switching Test Circuit



Switching Waveforms

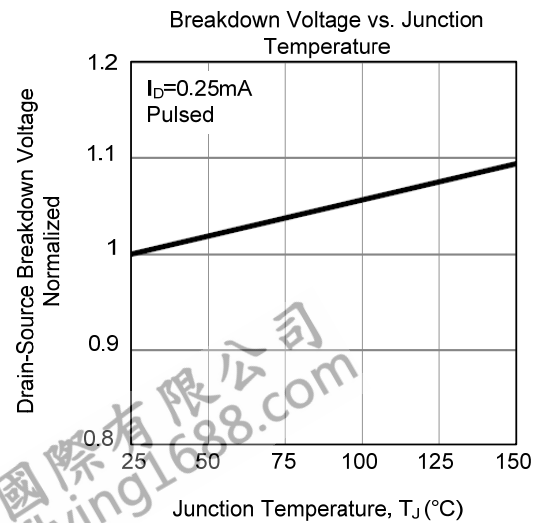
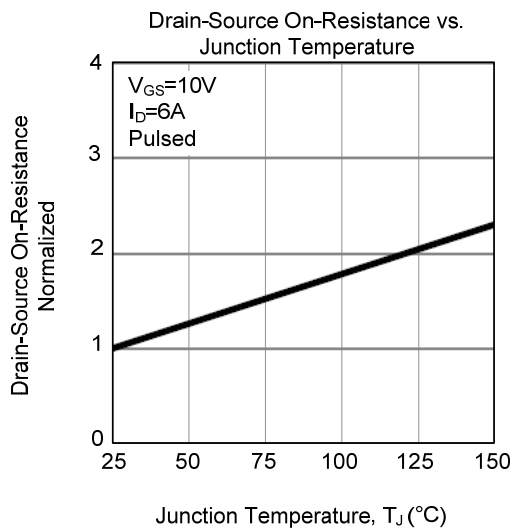
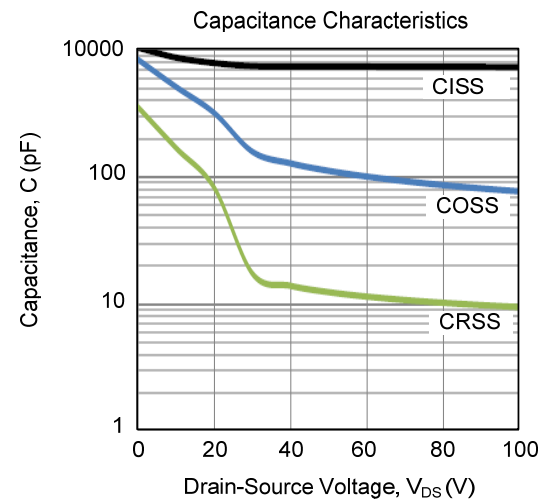
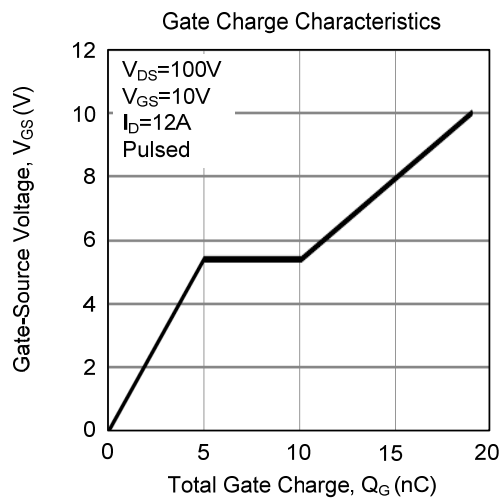
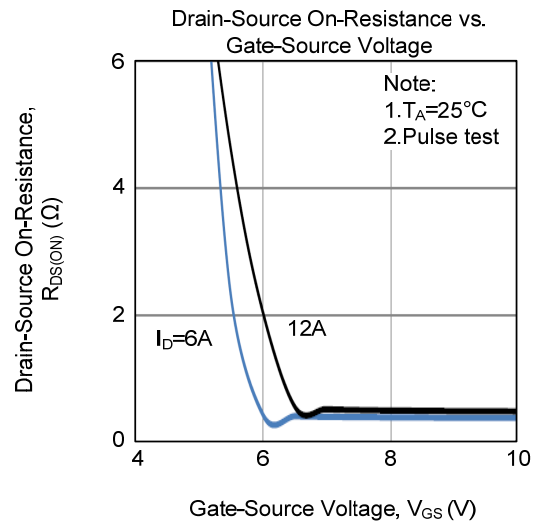
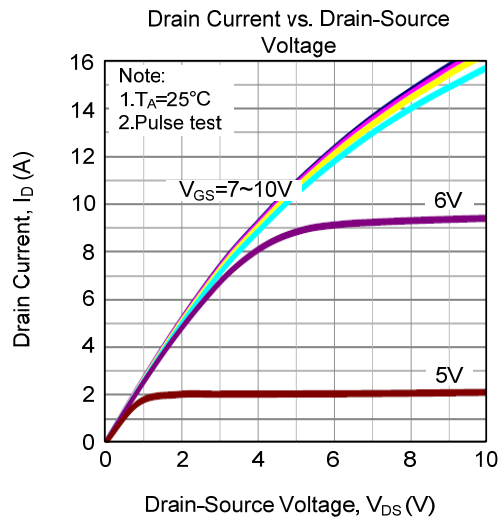


Unclamped Inductive Switching Test Circuit

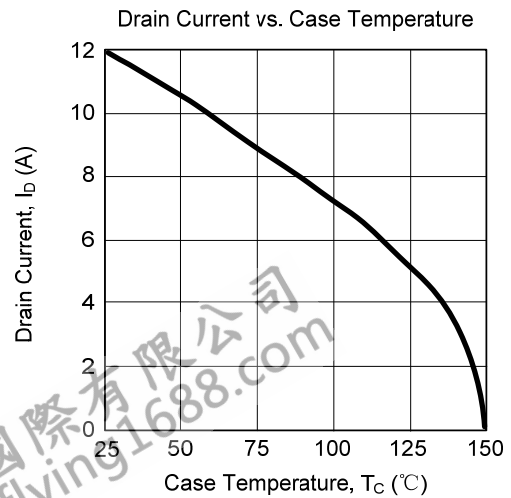
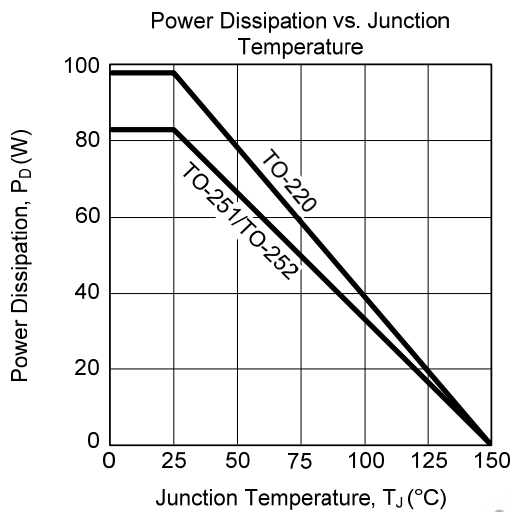
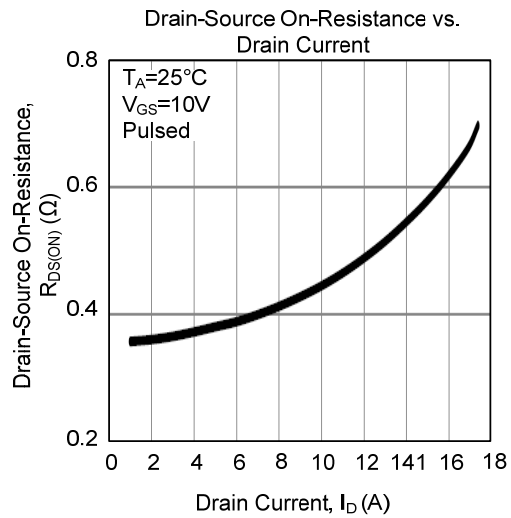
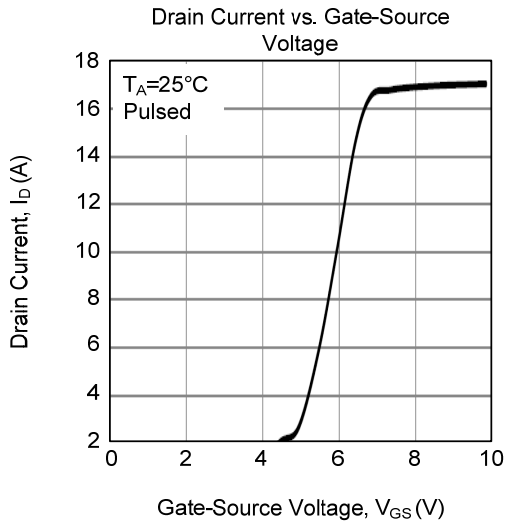
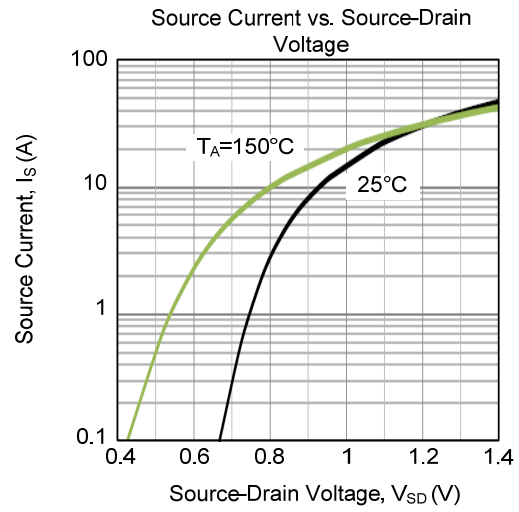
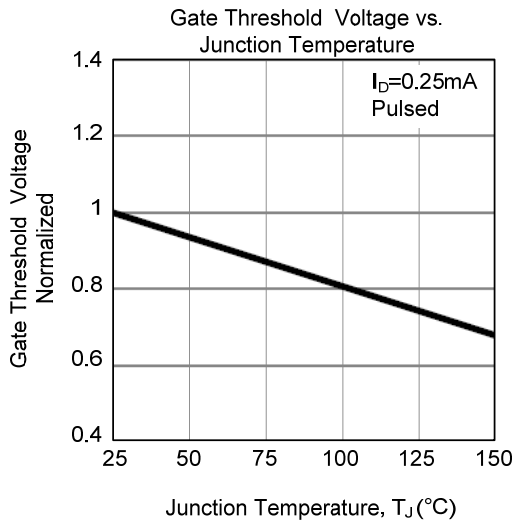


Unclamped Inductive Switching Waveforms

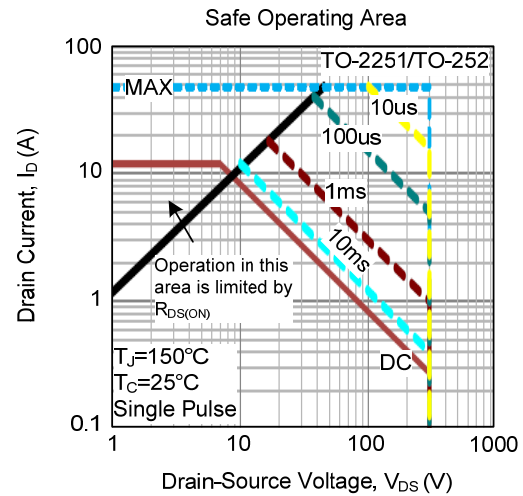
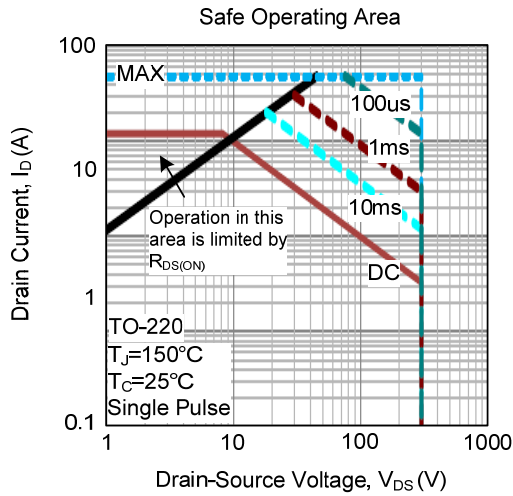
TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS (Cont.)



TYPICAL CHARACTERISTICS (Cont.)



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