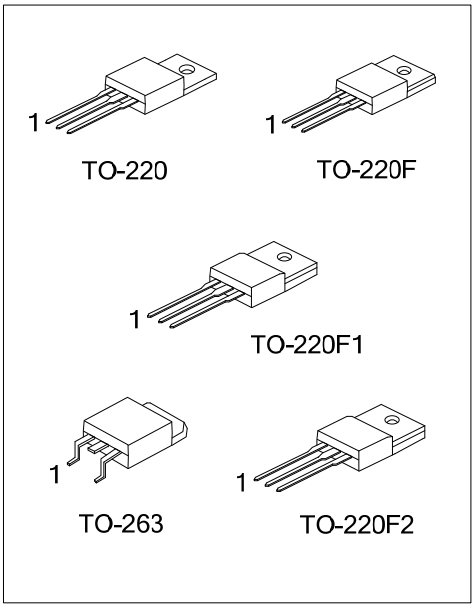
12N50K-MT

Power MOSFET

12A, 500V N-CHANNEL POWER MOSFET



■ DESCRIPTION

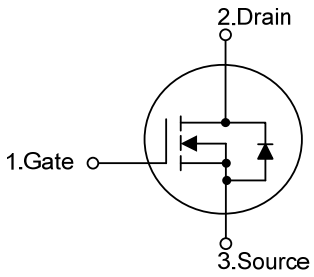
The UTC **12N50K-MT** is an N-channel mode power MOSFET using UTC's advanced technology to provide customers with planar stripe and DMOS technology. This technology allows a minimum on-state resistance and superior switching performance. It also can withstand high energy pulse in the avalanche and commutation mode.

The UTC **12N50K-MT** is generally applied in high efficiency switch mode power supplies, active power factor correction and electronic lamp ballasts based on half bridge topology.

■ FEATURES

* $R_{DS(ON)}$ < 0.52 Ω @ V_{GS} = 10 V, I_D = 6.0 A
* High Switching Speed
* 100% Avalanche Tested

■ SYMBOL



■ ORDERING INFORMATION

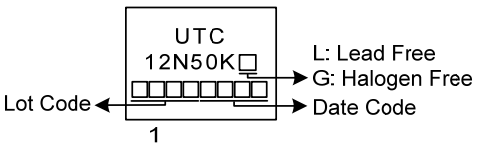
Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
12N50KL-TA3-T	12N50KG-TA3-T	TO-220	G	D	S	Tube
12N50KL-TF1-T	12N50KG-TF1-T	TO-220F1	G	D	S	Tube
12N50KL-TF2-T	12N50KG-TF2-T	TO-220F2	G	D	S	Tube
12N50KL-TF3-T	12N50KG-TF3-T	TO-220F	G	D	S	Tube
12N50KL-TQ2-T	12N50KG-TQ2-T	TO-263	G	D	S	Tube
12N50KL-TQ2-R	12N50KG-TQ2-R	TO-263	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

12N50KG-TA3-T
(1)Packing Type
(2)Package Type
(3)Green Package

(1) T: Tube, R: Tape Reel
(2) TA3: TO-220, TF3: TO-220F, TF1: TO-220F1, TF2: TO-220F2, TQ2: TO-263
(3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



■ ABSOLUTE MAXIMUM RATINGS (T_C=25°C, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	500	V
Gate-Source Voltage		V_{GSS}	±30	V
Drain Current	Continuous (T_C=25°C)	I_D	12 (Note 2)	A
	Pulsed (Note 3)	I_{DM}	48 (Note 2)	A
Avalanche Current (Note 3)		I_{AR}	12	A
Avalanche Energy	Single Pulsed (Note 4)	E_{AS}	600	mJ
Peak Diode Recovery dv/dt (Note 5)		dv/dt	3.5	V/ns
Power Dissipation	TO-220/TO-263	P_D	200	W
	TO-220F		50	W
	TO-220F1/TO-220F2		54	W
Junction Temperature		T_J	+150	°C
Storage Temperature		T_{STG}	-55 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. Drain current limited by maximum junction temperature
3. Repetitive Rating: Pulse width limited by maximum junction temperature
4. L =8.33mH, I_{AS} = 12A, V_{DD} = 50V, R_G = 25Ω, Starting T_J = 25°C
5. I_{SD} ≤ 12A, di/dt ≤ 200A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C

■ THERMAL DATA

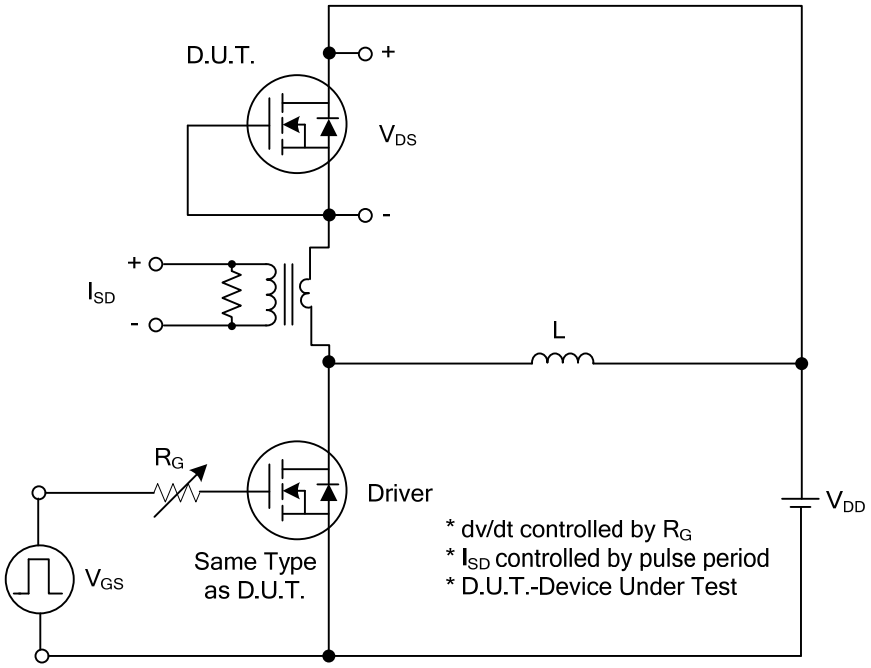
PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient		θ_{JA}	62.5	°C/W
Junction to Case	TO-220/TO-263	θ_{JC}	0.625	°C/W
	TO-220F		2.5	°C/W
	TO-220F1/TO-220F2		2.31	°C/W

■ ELECTRICAL CHARACTERISTICS (T_C=25°C, unless otherwise specified)

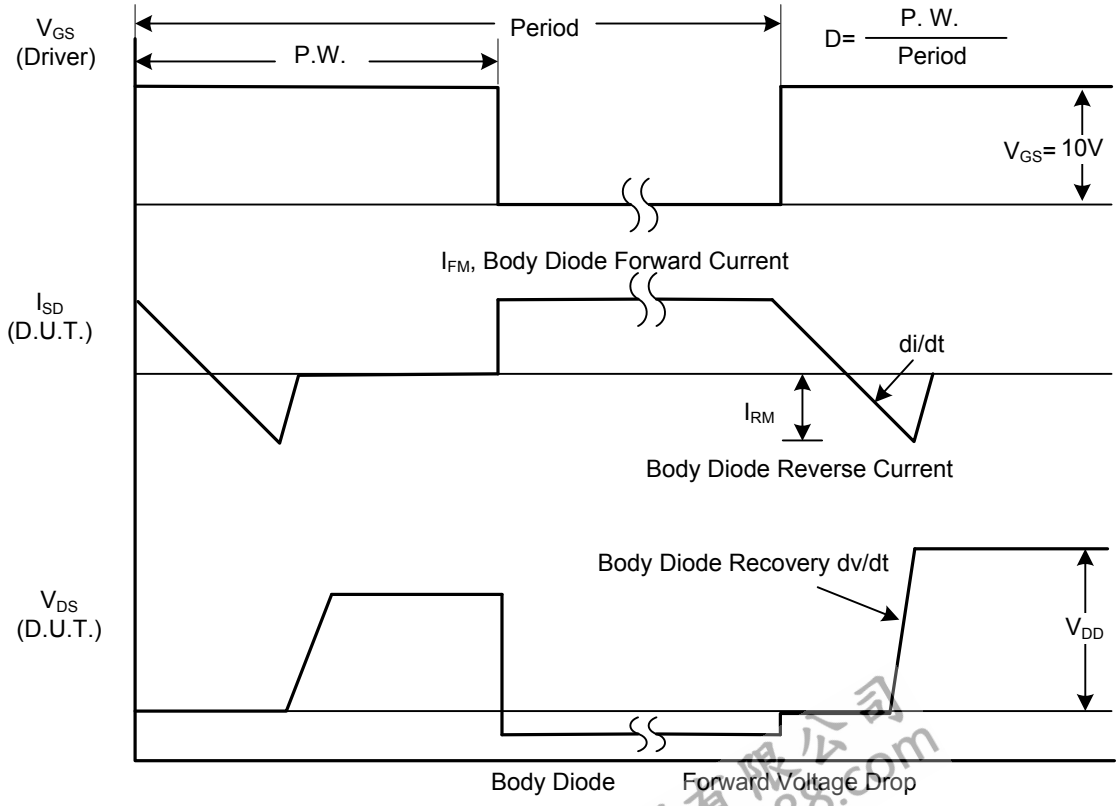
PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV_{DSS}	I_D=250μA, V_{GS}=0V	500			V
Drain-Source Leakage Current		I_{DSS}	V_{DS}=500V, V_{GS}=0V			10	μA
Gate- Source Leakage Current	Forward	I_{GSS}	V_{GS}=+30V, V_{DS}=0V			+100	nA
	Reverse		V_{GS}=-30V, V_{DS}=0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		$V_{GS(TH)}$	V_{DS}=V_{GS}, I_D=250μA	2.0		4.0	V
Static Drain-Source On-State Resistance		$R_{DS(ON)}$	V_{GS}=10V, I_D=6.0A		0.39	0.52	Ω
DYNAMIC PARAMETERS							
Input Capacitance		C_{ISS}	V_{GS}=0V, V_{DS}=25V, f=1.0MHz		1900		pF
Output Capacitance		C_{OSS}			200		pF
Reverse Transfer Capacitance		C_{RSS}			9.3		pF
SWITCHING PARAMETERS							
Total Gate Charge		Q_G	V_{GS}=10V, V_{DS}=300V, I_D=12A I_G=1mA (Note 1, 2)		38		nC
Gate to Source Charge		Q_{GS}			13		nC
Gate to Drain Charge		Q_{GD}			7		nC
Turn-ON Delay Time		$t_{D(ON)}$	V_{DD}=30V, I_D=0.5A, R_G=25Ω (Note 1, 2)		75		ns
Rise Time		t_R			125		ns
Turn-OFF Delay Time		$t_{D(OFF)}$			190		ns
Fall-Time		t_F			125		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Body-Diode Continuous Current		I_S				12	A
Maximum Body-Diode Pulsed Current		I_{SM}				48	A
Drain-Source Diode Forward Voltage		V_{SD}	I_S=12A, V_{GS}=0V			1.5	V
Reverse Recovery Time		t_{rr}	I_S=12A, V_{GS}=0V di/dt=100A/μs (Note 1)		400		ns
Reverse Recovery Charge		Q_{rr}			4.3		μC

Notes: 1. Pulse Test: Pulse width ≤ 300μs, Duty cycle ≤ 2%.
2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

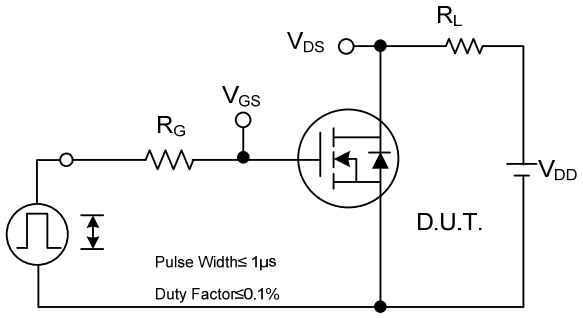


Peak Diode Recovery dv/dt Test Circuit

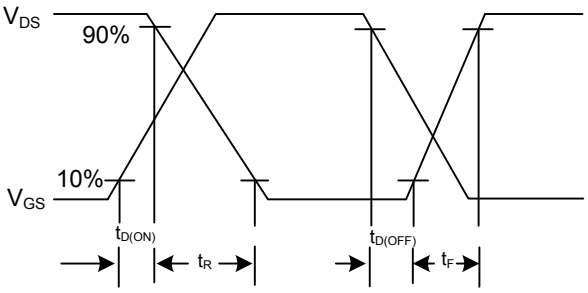


Peak Diode Recovery dv/dt Waveforms

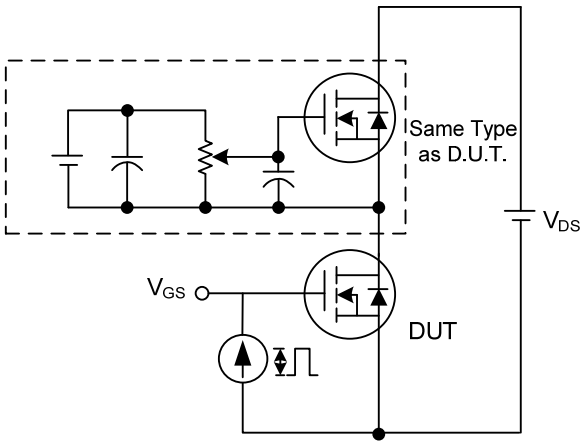
■ TEST CIRCUITS AND WAVEFORMS



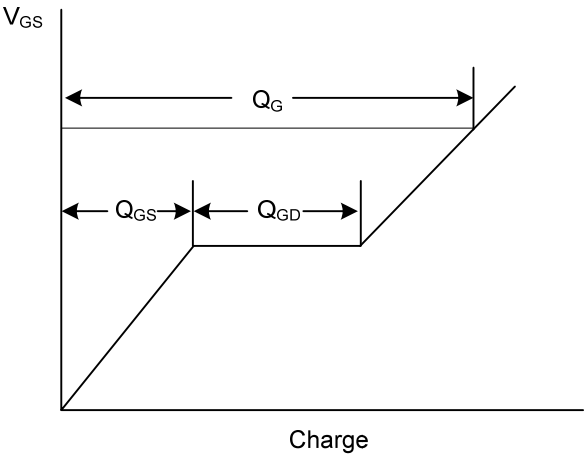
Switching Test Circuit



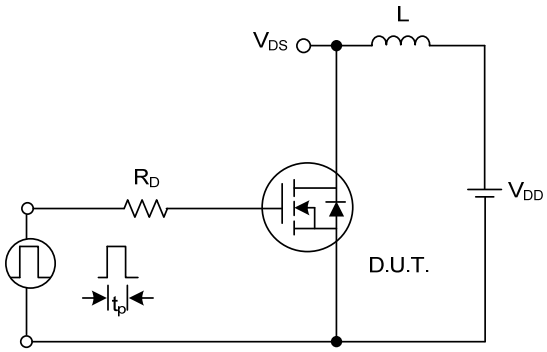
Switching Waveforms



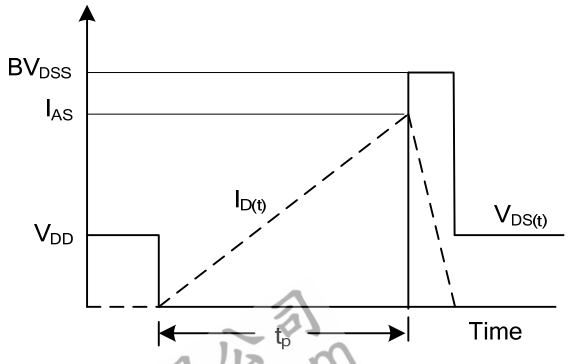
Gate Charge Test Circuit



Gate Charge Waveform



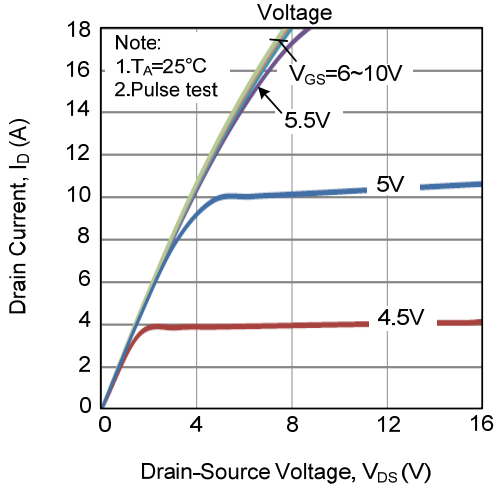
Unclamped Inductive Switching Test Circuit



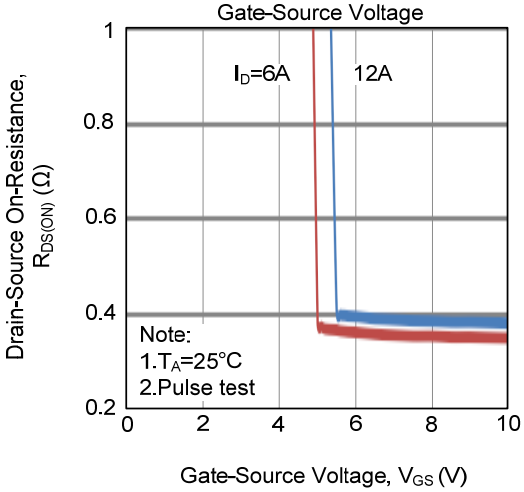
Unclamped Inductive Switching Waveforms

■ TYPICAL CHARACTERISTICS

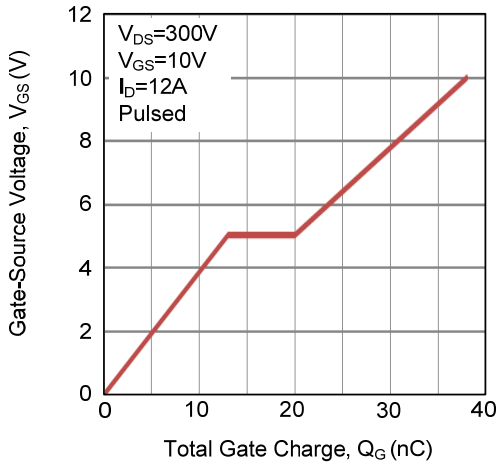
Drain Current vs. Drain-Source Voltage



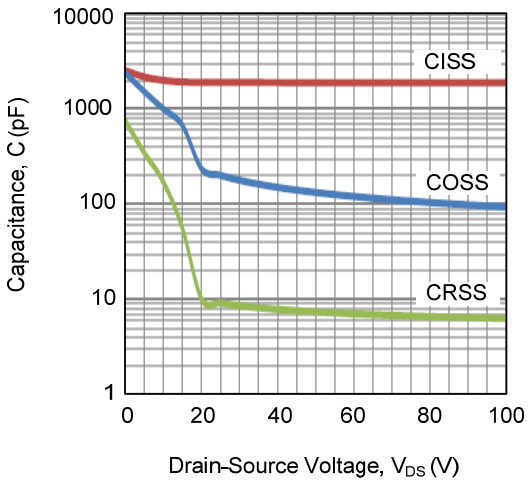
Drain-Source On-Resistance vs. Gate-Source Voltage



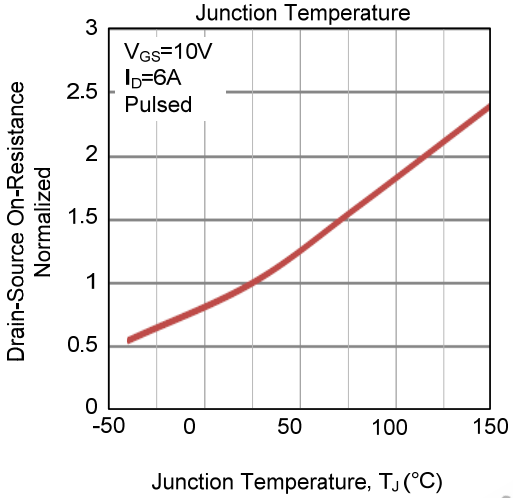
Gate Charge Characteristics



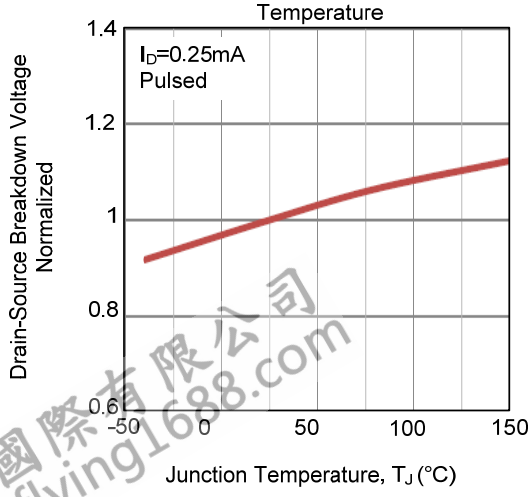
Capacitance Characteristics



Drain-Source On-Resistance vs. Junction Temperature

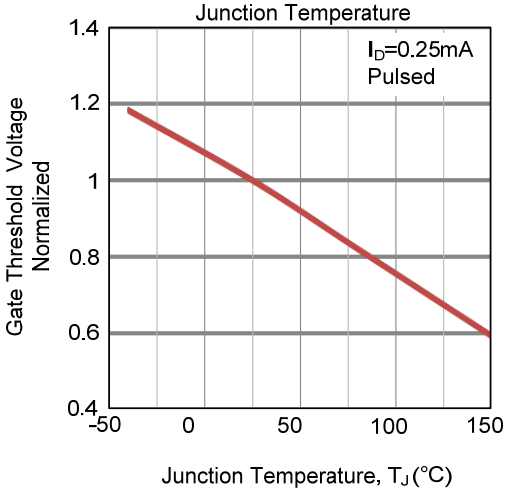


Breakdown Voltage vs. Junction Temperature

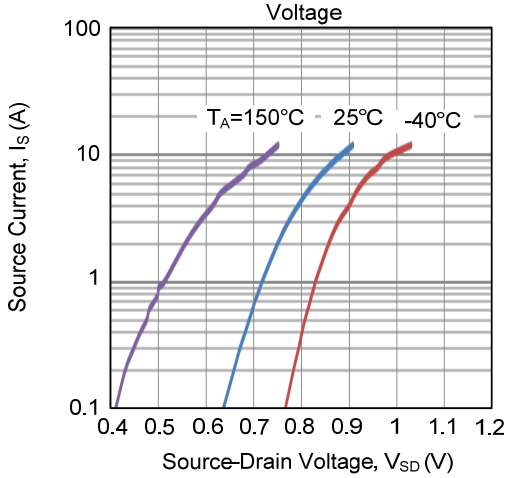


■ TYPICAL CHARACTERISTICS (Cont.)

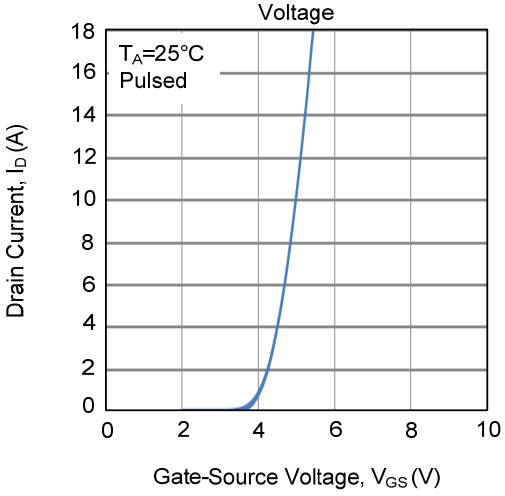
Gate Threshold Voltage vs. Junction Temperature



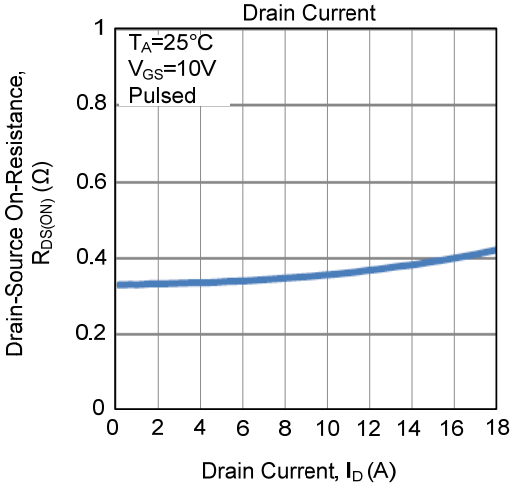
Source Current vs. Source-Drain Voltage



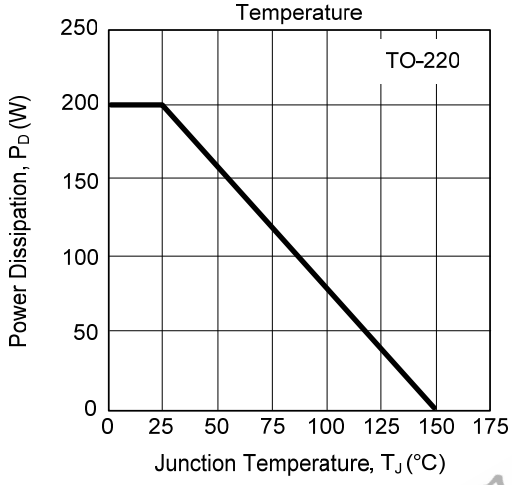
Drain Current vs. Gate-Source Voltage



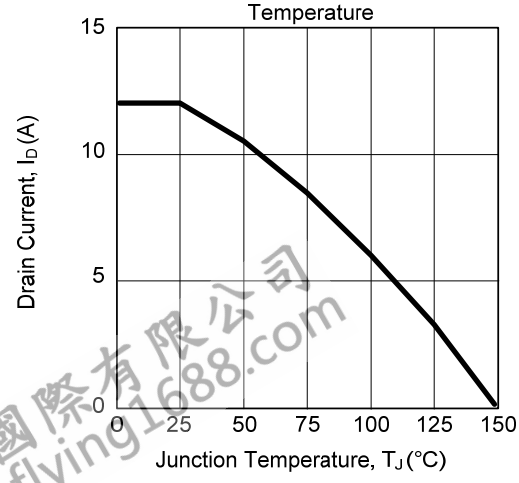
Drain-Source On-Resistance vs. Drain Current



Power Dissipation vs. Junction Temperature

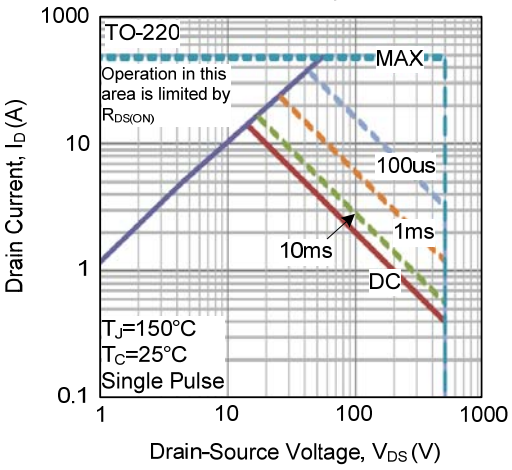


Drain Current vs. Junction Temperature



■ TYPICAL CHARACTERISTICS (Cont.)

Safe Operating Area



Maximum Safe Operating Area