



13N65-CQ

Preliminary

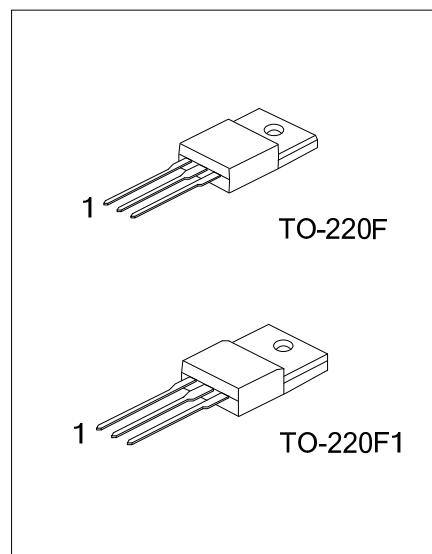
Power MOSFET

13A, 650V N-CHANNEL POWER MOSFET

DESCRIPTION

The UTC **13N65-CQ** is a N-channel mode power MOSFET using UTC's advanced technology to provide customers with planar stripe and DMOS technology. This technology allows a minimum on-state resistance and superior switching performance. It also can withstand high energy pulse in the avalanche and commutation mode.

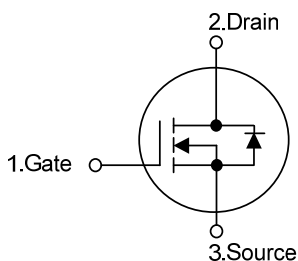
This power MOSFET is usually used at high speed switching applications in power supplies, PWM motor controls, high efficient DC to DC converters and bridge circuits.



FEATURES

- * $R_{DS(ON)} < 0.8\Omega @ V_{GS}=10V, I_D=4.75A$
- * Fast switching
- * 100% avalanche tested
- * Improved dv/dt capability

SYMBOL



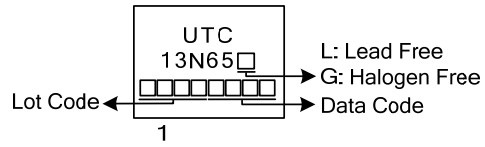
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
13N65L-TF1-T	13N65G-TF1-T	TO-220F1	G	D	S	Tube
13N65L-TF3-T	13N65G-TF3-T	TO-220F	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>13N65G-TF1-T</p> <p>(1) Packing Type</p> <p>(2) Package Type</p> <p>(3) Green Package</p>	<p>(1) T: Tube</p> <p>(2) TF1: TO-220F1, TF3: TO-220F</p> <p>(3) G: Halogen Free and Lead Free, L: Lead Free</p>
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MARKING



■ ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	650	V
Gate-Source Voltage		V_{GSS}	± 30	V
Drain Current	Continuous	I_D	13	A
	Pulsed (Note 2)	I_{DM}	52	A
Avalanche Current (Note 2)		I_{AR}	8.8	A
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	387	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	2.3	V/ns
Power Dissipation		P_D	53	W
Junction Temperature		T_J	+150	$^\circ\text{C}$
Storage Temperature		T_{STG}	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $L = 13\text{mH}$, $I_{AS} = 8.8\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 25\ \Omega$ Starting $T_J = 25^\circ\text{C}$

4. $I_{SD} \leq 13\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$

■ THERMAL DATA

PARAMETER	SYMBOL	RATING	UNIT
Junction to Ambient	θ_{JA}	62.5	$^\circ\text{C}/\text{W}$
Junction to Case	θ_{JC}	2.36	$^\circ\text{C}/\text{W}$

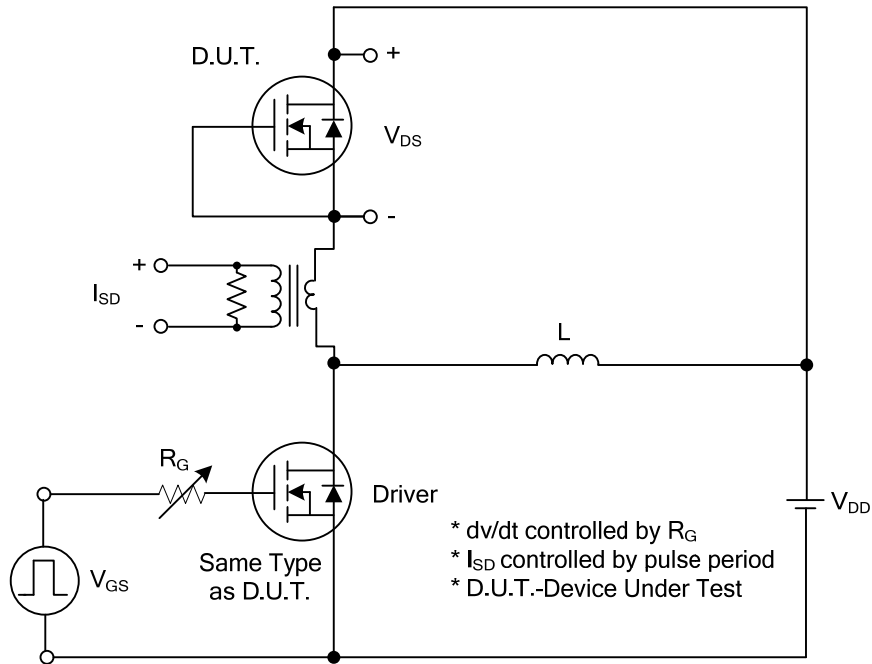
■ ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0\text{V}$, $I_D=250\mu\text{A}$	650			V
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=650\text{V}$, $V_{GS}=0\text{V}$			1	μA
Gate-Source Leakage Current	Forward	I_{GSS}			100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	2.0		4.0	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=6.5\text{A}$			0.80	Ω
DYNAMIC CHARACTERISTICS						
Input Capacitance	C_{ISS}	$V_{GS}=0\text{V}$, $V_{DS}=25\text{V}$, $f=1.0\text{MHz}$		1740		pF
Output Capacitance	C_{OSS}			164		pF
Reverse Transfer Capacitance	C_{RSS}			9.0		pF
SWITCHING CHARACTERISTICS						
Total Gate Charge (Note 1)	Q_G	$V_{DS}=50\text{V}$, $V_{GS}=10\text{V}$, $I_D=1.3\text{A}$, $I_G=100\mu\text{A}$ (Note 1, 2)		100		nC
Gate to Source Charge	Q_{GS}			12		nC
Gate to Drain Charge	Q_{GD}			16		nC
Turn-ON Delay Time (Note 1)	$t_{D(ON)}$	$V_{DD}=30\text{V}$, $V_{GS}=10\text{V}$, $I_D=0.5\text{A}$, $R_G=25\Omega$ (Note 1, 2)		90		ns
Rise Time	t_R			78		ns
Turn-OFF Delay Time	$t_{D(OFF)}$			350		ns
Fall-Time	t_F			100		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Body-Diode Continuous Current	I_S				13	A
Maximum Body-Diode Pulsed Current	I_{SM}				52	A
Drain-Source Diode Forward Voltage (Note 1)	V_{SD}	$I_S=13\text{A}$, $V_{GS}=0\text{V}$			1.4	V
Body Diode Reverse Recovery Time (Note 1)	t_{rr}	$I_S=13\text{A}$; $V_{GS}=0\text{V}$,		500		ns
Body Diode Reverse Recovery Charge	Q_{rr}	$di/dt=100\text{A}/\mu\text{s}$		4.26		μC

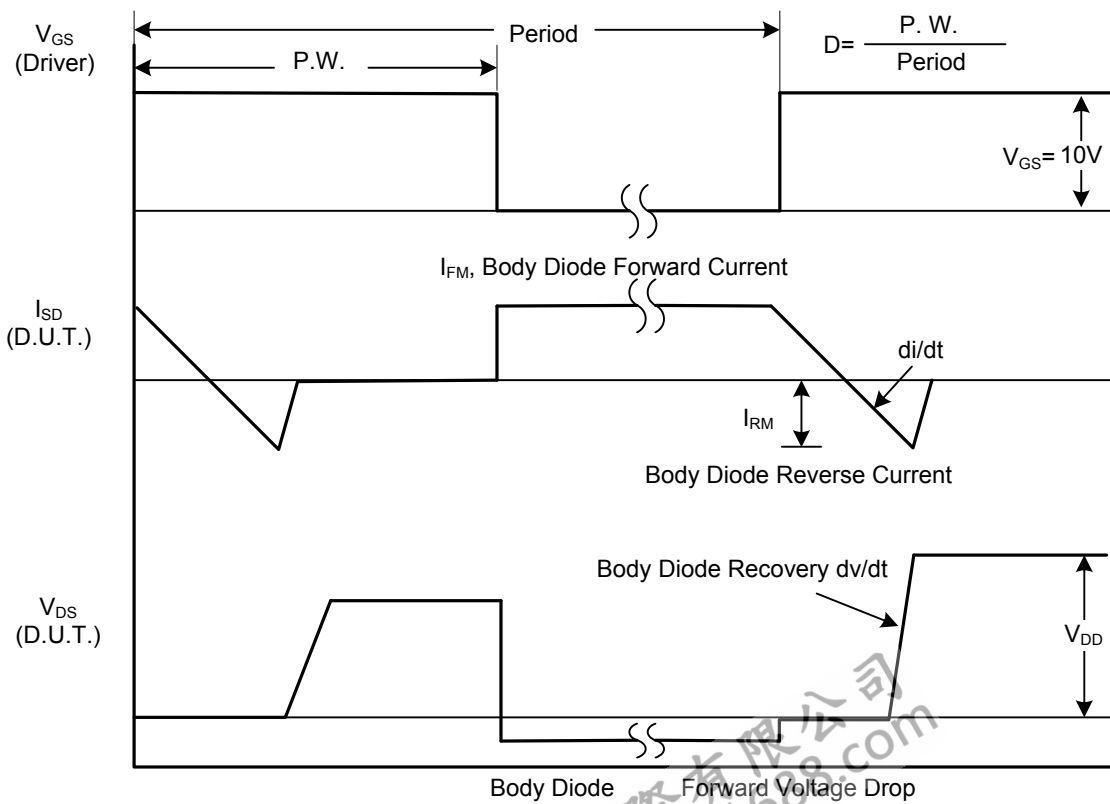
Notes: 1. Pulse Test : Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

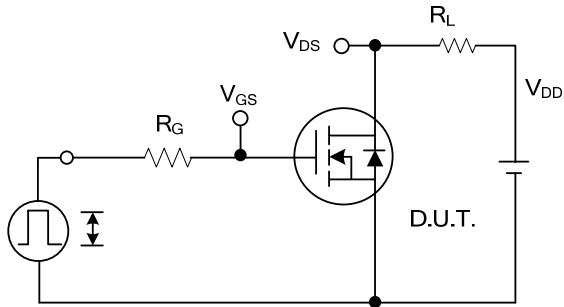


Peak Diode Recovery dv/dt Test Circuit

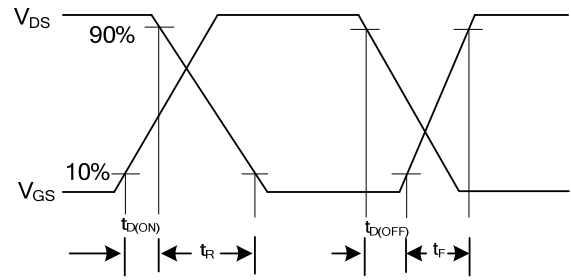


Peak Diode Recovery dv/dt Waveforms

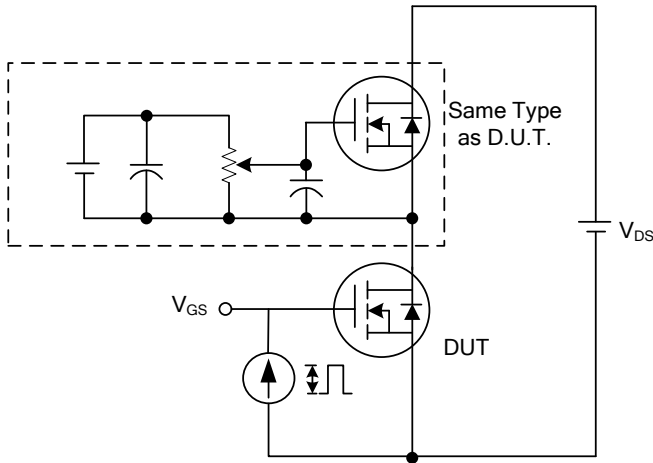
■ TEST CIRCUITS AND WAVEFORMS (Cont.)



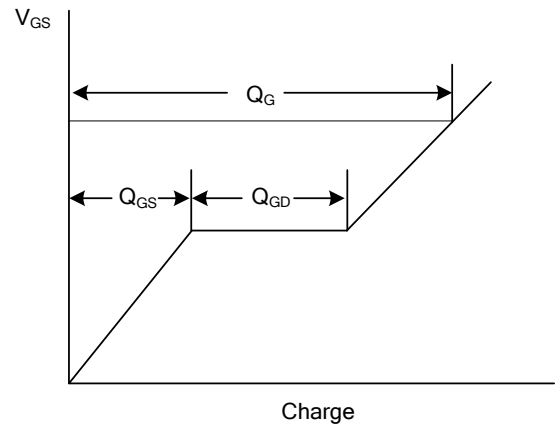
Switching Test Circuit



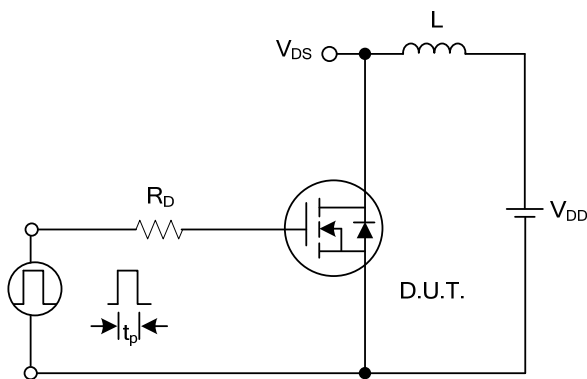
Switching Waveforms



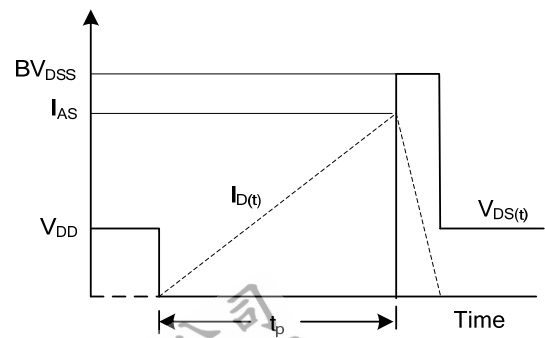
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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