

14N40K-MT

Preliminary

14A, 400V N-CHANNEL POWER MOSFET

DESCRIPTION

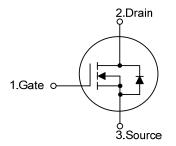
The UTC **14N40K-MT** is an N-Channel enhancement mode power MOSFET. The device adopts planar stripe and uses DMOS technology to minimize and provide lower on-state resistance and faster switching speed. It can also withstand high energy pulse under the avalanche and commutation mode conditions.

The UTC **14N40K-MT** is ideally suitable for high efficiency switch mode power supply, power factor correction and electronic lamp ballast based on half bridge topology.

FEATURES

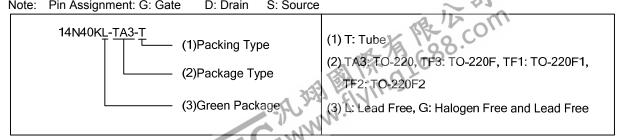
- * $R_{DS(ON)}$ < 0.34 Ω @ V_{GS} = 10V, I_D = 7A
- * Fast switching capability
- * Avalanche energy tested
- * Improved dv/dt capability, high ruggedness

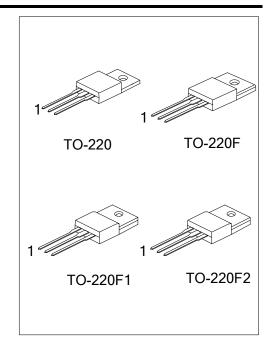
SYMBOL



ORDERING INFORMATION

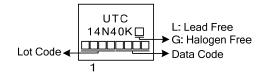
	Ordering Number		Dookogo	Pin Assignment			Deaking	
	Lead Free	Halogen Free	Package	1	2	3	Packing	
	14N40KL-TA3-T	14N40KG-TA3-T	TO-220	G	D	S	Tube	
	14N40KL-TF3-T	14N40KG-TF3-T	TO-220F	G	D	S	Tube	
	14N40KL-TF1-T	14N40KG-TF1-T	TO-220F1	G	D	S	Tube	
	14N40KL-TF2-T	14N40KG-TF2-T	TO-220F2	G	D	S	Tube	
Note: Pin Assignment: G: Gate		te D: Drain S: Source		~	37			





14N40K-MT

MARKING





ABSOLUTE MAXIMUM RATINGS (T_c = 25°C, unless otherwise specified)

PARAME	TER	SYMBOL	RATINGS	UNIT	
Drain-Source Voltage		V _{DSS}	400	V	
Gate-Source Voltage		V _{GSS}	±30	V	
Continuous Drain Current		I _D	14	А	
Pulsed Drain Current (Note 2)		I _{DM}	48	А	
Avalanche Current (Note 2)		I _{AR}	14	Α	
Single Pulsed Avalanche Ener	gy (Note 3)	E _{AS}	535	mJ	
Peak Diode Recovery dv/dt (N	ote 4)	dv/dt	4.5	V/ns	
	TO-220		150	W	
Power Dissipation (T _C =25°C)	TO-220F/TO-220F1 TO-220F2		40	W	
	TO-220		1.2	W/°C	
Derate above 25°C	TO-220F/TO-220F1 TO-220F2		0.32	W/°C	
Junction Temperature	•	TJ	+150	°C	
Storage Temperature		T _{STG}	-55~+150	°C	

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

- 2. Repetitive Rating : Pulse width limited by maximum junction temperature
- 3. L = 5.46mH, I_{AS} = 14A, V_{DD} = 50V, R_G= 25\Omega, Starting T_J = 25°C
- 4. $I_{SD} \le 14A$, di/dt $\le 200A/\mu s$, $V_{DD} \le BV_{DSS}$, Starting $T_J = 25^{\circ}C$

THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient		θ_{JA}	62.5	°C/W
	TO-220		0.83	°C/W
Junction to Case	TO-220F/TO-220F1 TO-220F2	θ _{JC}	3.125	°C/W



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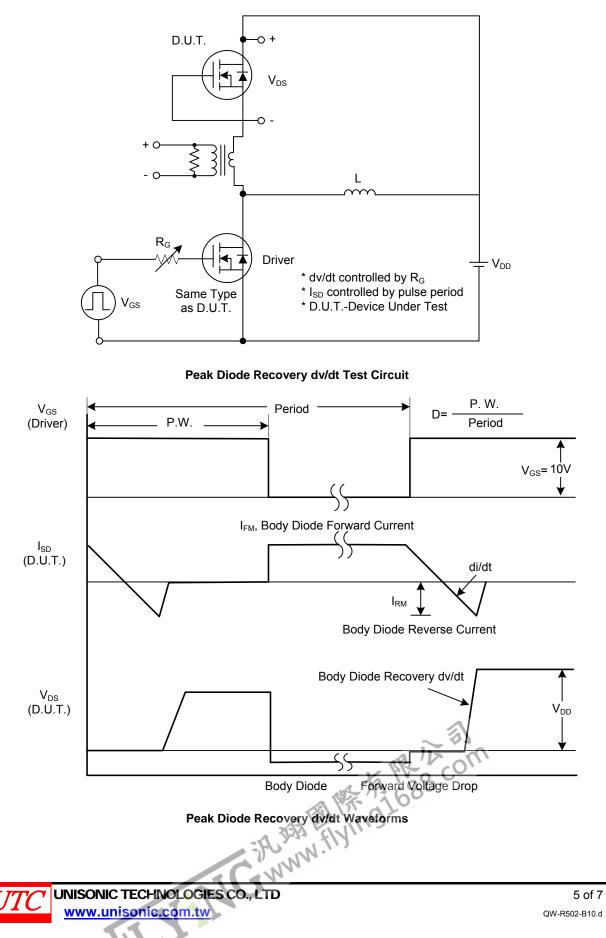
■ ELECTRICAL CHARACTERISTICS (T_c=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV _{DSS}	V_{GS} = 0V, I_{D} = 1mA	400			V
Drain-Source Leakage Current	I _{DSS}	$V_{DS} = 400 V, V_{GS} = 0 V$			10	μA
Gate-Source Leakage Current	I _{GSS}	$V_{GS} = 20V, V_{DS} = 0V$			100	nA
Gale-Source Leakage Current		V_{GS} = -20V, V_{DS} = 0V			-100	nA
Breakdown Voltage Temperature Coefficient	$\triangle BV_{\text{DSS}} / \triangle T_{\text{J}}$	I _D =250mA,Referenced to 25°C		0.5		V/°C
ON CHARACTERISTICS						
Gate Threshold Voltage	V _{GS(TH)}	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$			4.0	V
Static Drain-Source On-State Resistance				0.26	0.34	Ω
DYNAMIC CHARACTERISTICS						
Input Capacitance	CISS	V _{DS} =25V, V _{GS} =0V, f=1.0MHz		810		pF
Output Capacitance	C _{OSS}			190		рF
Reverse Transfer Capacitance	C _{RSS}			10.5		pF
SWITCHING CHARACTERISTICS						
Total Gate Charge	Q_G	−V _{DS} = 50V, V _{GS} = 10V, I _D = 0.3A, − −I _D =100µA (Note 1, 2)		34.9		nC
Gate-Source Charge	Q _{GS}			9.1		nC
Gate-Drain Charge	Q_{GD}			8.8		nC
Turn-On Delay Time	t _{D(ON)}	-V _{DS} = 30V, V _{GS} = 10V, I _D = -0.3A, -R _G = 25Ω (Note 1, 2)		66		nS
Turn-On Rise Time	t _R			96		nS
Turn-Off Delay Time	t _{D(OFF)}			200		nS
Turn-Off Fall Time	t _F			112		nS
DRAIN-SOURCE DIODE CHARACTERISTIC	CS AND MAXI	MUM RATINGS				
Drain-Source Diode Forward Voltage	V_{SD}	V _{GS} = 0V, I _S = 14A			1.4	V
Maximum Continuous Drain-Source Diode	I _S				14	А
Forward Current					14	А
Maximum Pulsed Drain-Source Diode	lau				56	А
Forward Current	I _{SM}				50	

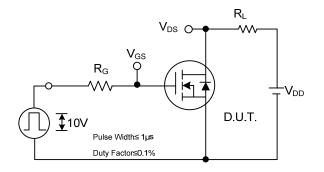
Notes: 1. Pulse Test : Pulse width≤300µs, Duty cycle≤2%.

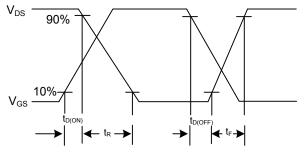
2. Essentially independent of operating ambient temperature.

TEST CIRCUITS AND WAVEFORMS



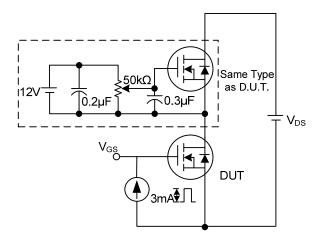
TEST CIRCUITS AND WAVEFORMS (Cont.)



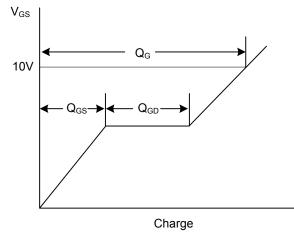


Switching Test Circuit

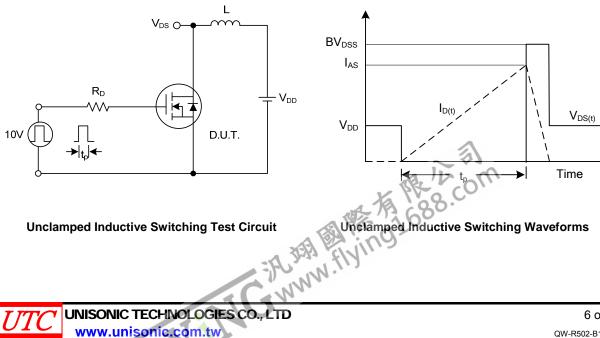




Gate Charge Test Circuit



Gate Charge Waveform



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