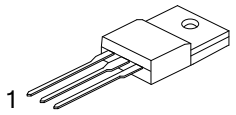
14A, 650V N-CHANNEL POWER MOSFET



TO-220F2

■ DESCRIPTION

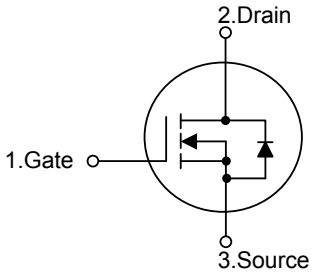
The UTC **14N65K-MT** is an N-Channel enhancement mode power MOSFET. The device adopts planar stripe and uses DMOS technology to minimize and provide lower on-state resistance and faster switching speed. It can also withstand high energy pulse under the avalanche and commutation mode conditions.

The UTC **14N65K-MT** is ideally suitable for high efficiency switch mode power supply, power factor correction and electronic lamp ballast based on half bridge topology.

■ FEATURES

* $R_{DS(ON)}$ < 0.63Ω @ V_{GS} = 10V, I_D = 7 A
* Fast switching capability
* Avalanche energy tested
* Improved dv/dt capability, high ruggedness

■ SYMBOL



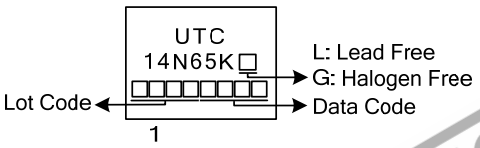
■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
14N65KL-TF2-T	14N65KG-TF2-T	TO-220F2	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

14N65KL-TF2-T (1)Packing Type (2)Package Type (3)Green Package	(1) T: Tube (2) TF2: TO-220F2 (3) L: Lead Free, G: Halogen Free and Lead Free

■ MARKING



■ ABSOLUTE MAXIMUM RATINGS (T_C = 25°C, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Drain-Source Voltage	V_{DSS}	650	V
Gate-Source Voltage	V_{GSS}	±30	V
Continuous Drain Current	I_D	14	A
Pulsed Drain Current (Note 2)	I_{DM}	48	A
Avalanche Current (Note 2)	I_{AR}	14	A
Single Pulsed Avalanche Energy (Note 3)	E_{AS}	325	mJ
Peak Diode Recovery dv/dt (Note 4)	dv/dt	4.5	V/ns
Power Dissipation (T_C=25°C)	P_D	150	W
Junction Temperature	T_J	+150	°C
Storage Temperature	T_{STG}	-55~+150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. Repetitive Rating : Pulse width limited by maximum junction temperature
3. L = 3.31mH, I_{AS} = 14A, V_{DD} = 50V, R_G= 25Ω, Starting T_J = 25°C
4. I_{SD}≤14A, di/dt ≤200A/μs, V_{DD}≤ BV_{DSS}, Starting T_J= 25°C

■ THERMAL DATA

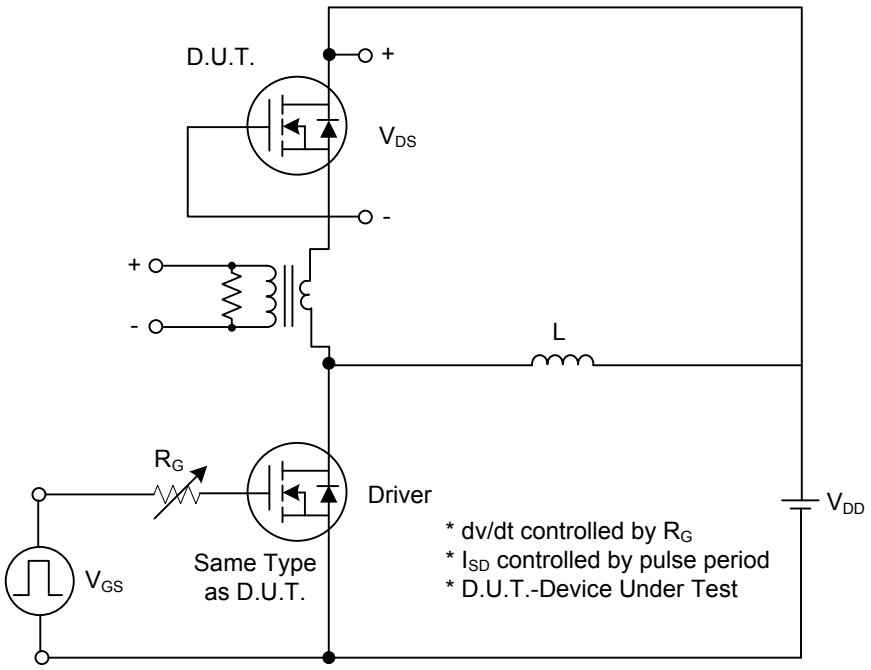
PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	62.5	°C/W
Junction to Case	θ_{JC}	0.83	°C/W

■ ELECTRICAL CHARACTERISTICS (T_C =25°C, unless otherwise specified)

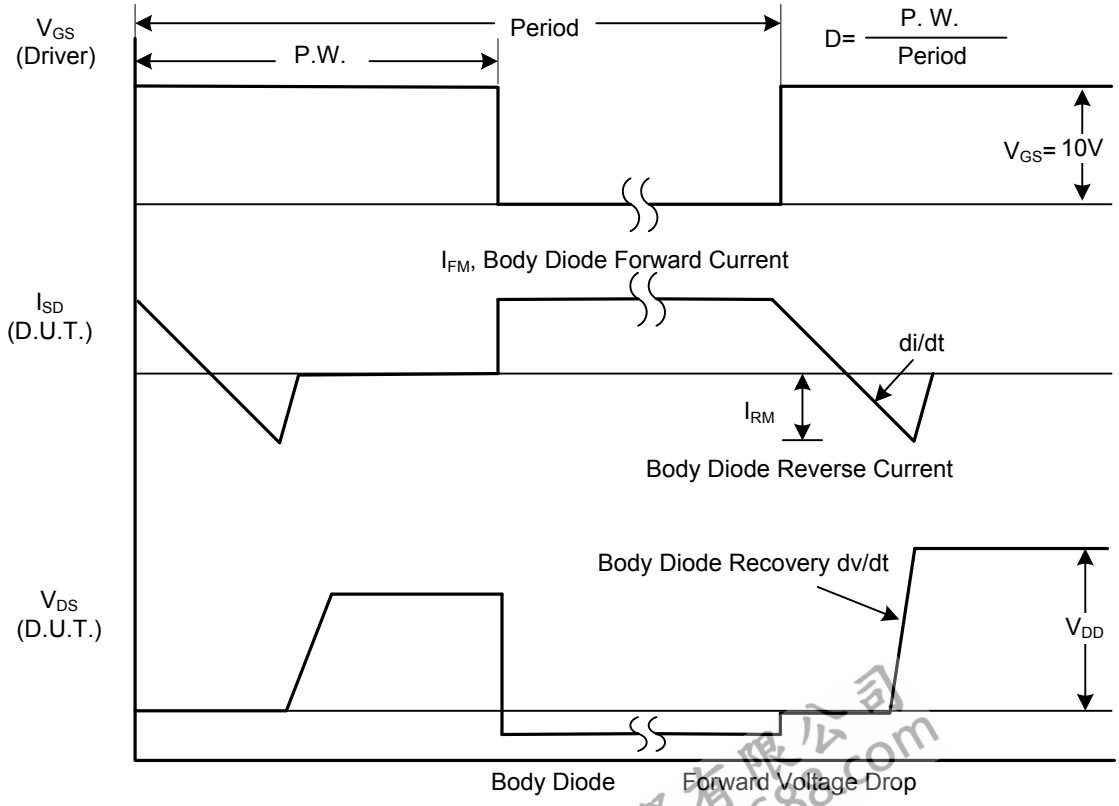
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = 250 μA	650			V
Drain-Source Leakage Current	I_{DSS}	V_{DS} = 650V, V_{GS} = 0V			10	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = 30V, V_{DS} = 0V			100	nA
		V_{GS} = -30V, V_{DS} = 0V			-100	nA
Breakdown Voltage Temperature Coefficient	$\triangle BV_{DSS}/\triangle T_J$	I_D=250mA,Referenced to 25°C		0.5		V/°C
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0		4.0	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 7A			0.63	Ω
DYNAMIC CHARACTERISTICS						
Input Capacitance	C_{ISS}	V_{DS}=25V, V_{GS}=0V, f=1.0MHz		980		pF
Output Capacitance	C_{OSS}			185		pF
Reverse Transfer Capacitance	C_{RSS}			10		pF
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	$t_{D(ON)}$	V_{DS}=30V, I_D=0.5A, R_G=25Ω (Note 1, 2)		89		nS
Turn-On Rise Time	t_R			116		nS
Turn-Off Delay Time	$t_{D(OFF)}$			388		nS
Turn-Off Fall Time	t_F			145		nS
Total Gate Charge	Q_G	V_{GS}=10V, V_{DS}=50V, I_D=1.3A (Note 1, 2)		47		nC
Gate-Source Charge	Q_{GS}			12.2		nC
Gate-Drain Charge	Q_{GD}			11.6		nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
Drain-Source Diode Forward Voltage	V_{SD}	V_{GS} = 0V, I_S = 14A			1.4	V
Maximum Continuous Drain-Source Diode Forward Current	I_S				14	A
Maximum Pulsed Drain-Source Diode Forward Current	I_{SM}				56	A

Notes: 1. Pulse Test : Pulse width≤300μs, Duty cycle≤2%
2. Essentially independent of operating ambient temperature

■ TEST CIRCUITS AND WAVEFORMS

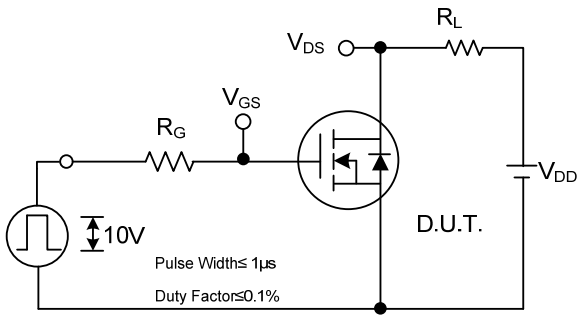


Peak Diode Recovery dv/dt Test Circuit

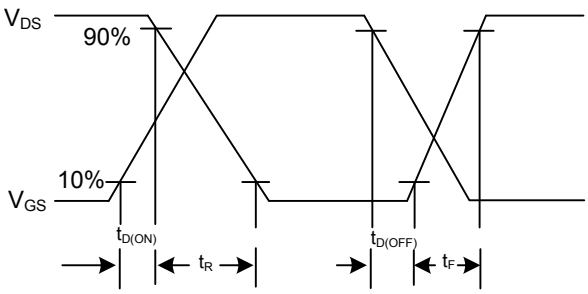


Peak Diode Recovery dv/dt Waveforms

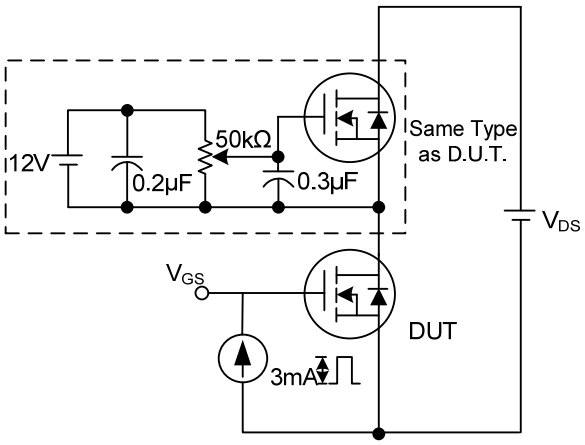
■ TEST CIRCUITS AND WAVEFORMS (Cont.)



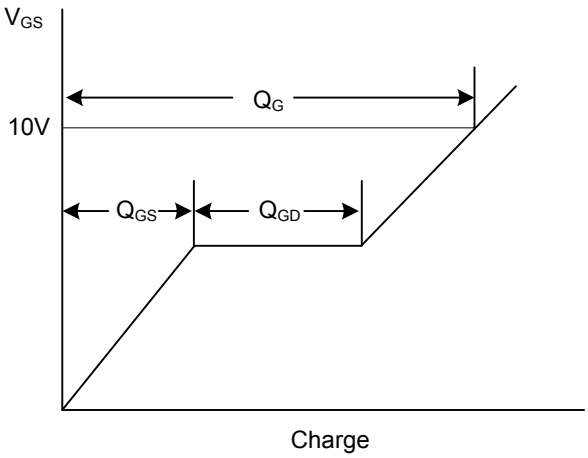
Switching Test Circuit



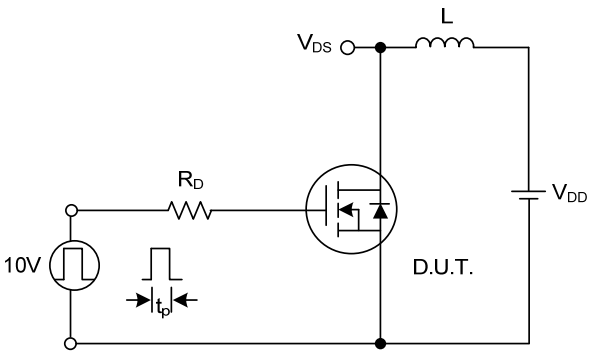
Switching Waveforms



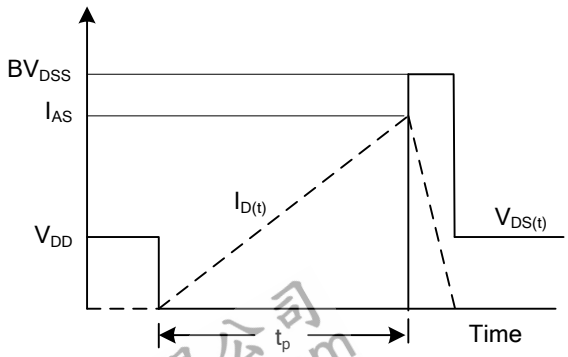
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms