

17A, 120V P-CHANNEL POWER MOSFET

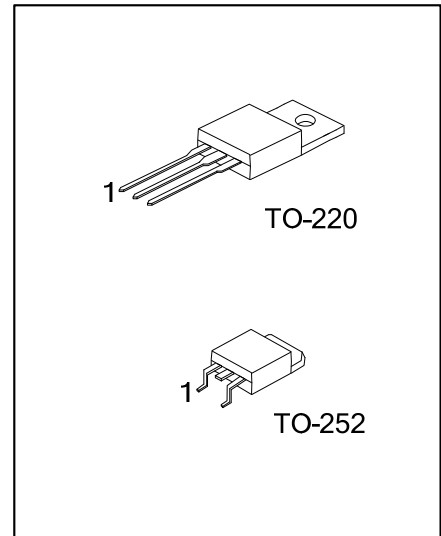
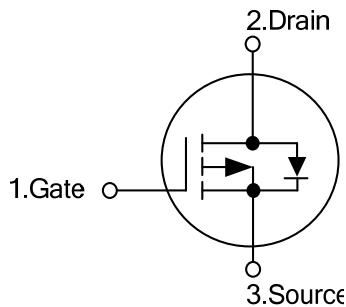
DESCRIPTION

The **17P12** uses advanced proprietary, planar stripe, DMOS technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with low gate voltages. This device is suitable to be used in low voltage applications such as audio amplifier, high efficiency switching DC/DC converters, and DC motor control.

FEATURES

- * $R_{DS(ON)} < 0.22\Omega$ @ $V_{GS}=-10V$, $I_D=-8.25A$
- * Low capacitance
- * Low gate charge
- * Fast switching capability
- * Avalanche energy specified

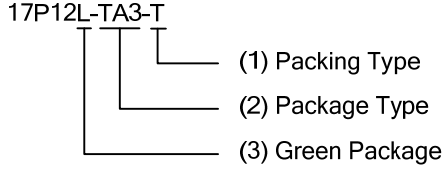
SYMBOL



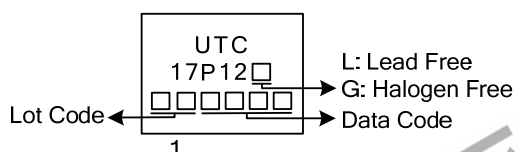
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
17P12L-TA3-T	17P12G-TA3-T	TO-220	G	D	S	Tube
17P12L-TN3-R	17P12G-TN3-R	TO-252	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>17P12L-TA3-T</p>  <p>(1) Packing Type (2) Package Type (3) Green Package</p>	<p>(1) T: Tube, R: Tape Reel (2) TA3: TO-220, TN3: TO-252 (3) L: Lead Free, G: Halogen Free and Lead Free</p>
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MARKING



■ ABSOLUTE MAXIMUM RATINGS ($T_C=25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Drain-Source Voltage	V_{DSS}	-120	V
Gate-Source Voltage	V_{GSS}	± 30	V
Continuous Drain Current	I_D	-17	A
Pulsed Drain Current (Note 2)	I_{DM}	-52	A
Avalanche Current (Note 2)	I_{AR}	-14	A
Single Pulsed Avalanche Energy (Note 3)	E_{AS}	340	mJ
Peak Diode Recovery dv/dt	dv/dt	5	V/ns
Power Dissipation	TO-220	100	W
	TO-252	70	W
Junction Temperature	T_J	+150	$^\circ\text{C}$
Storage Temperature	T_{STG}	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Pulse width limited by $T_{J(MAX)}$

3. $L=3.5\text{mH}$, $I_{AS}=-14\text{A}$, $V_{DD}=-50\text{V}$, $R_G=25\Omega$, Starting $T_J=25^\circ\text{C}$

4. $I_{SD}\leq-17\text{A}$, $di/dt \leq 200\mu\text{A/s}$, $V_{DD}\leq BV_{DSS}$, Starting $T_J=25^\circ\text{C}$

■ THERMAL DATA

PARAMETER	SYMBOL	RATING	UNIT
Junction to Ambient	TO-220	62.5	$^\circ\text{C/W}$
	TO-252	110	$^\circ\text{C/W}$
Junction to Case	TO-220	1.25	$^\circ\text{C/W}$
	TO-252	1.78	$^\circ\text{C/W}$

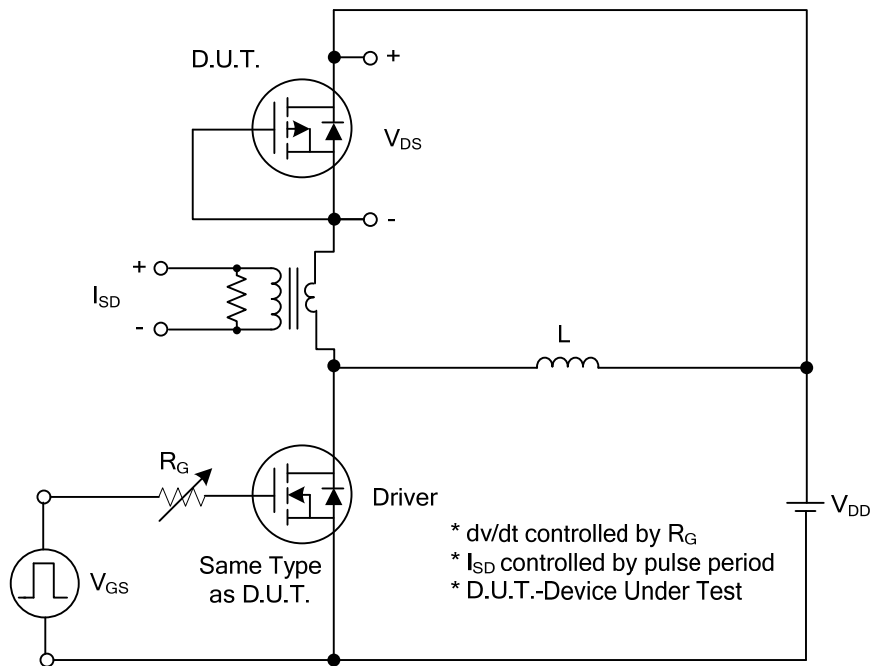
■ ELECTRICAL CHARACTERISTICS ($T_C=25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0\text{ V}, I_D=-250\mu\text{A}$	-120			V
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=-120\text{V}, V_{GS}=0\text{V}$			-1	μA
		$V_{DS}=-120\text{V}, T_C=125^\circ\text{C}$			-10	μA
Gate-Source Leakage Current	I_{GSS}	$V_{DS}=0\text{V}, V_{GS}=\pm 30\text{V}$			± 100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}, I_D=-250\mu\text{A}$	-2.0		-4.0	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	$V_{GS}=-10\text{V}, I_D=-8.25\text{A}$			0.22	Ω
DYNAMIC PARAMETERS						
Input Capacitance	C_{ISS}	$V_{DS}=-25\text{V}, V_{GS}=0\text{V}, f=1.0\text{MHz}$		1250		pF
Output Capacitance	C_{OSS}			390		pF
Reverse Transfer Capacitance	C_{RSS}			165		pF
SWITCHING PARAMETERS						
Total Gate Charge	Q_G	$V_{DS}=-50\text{V}, V_{GS}=-10\text{V}, I_D=-1.3\text{A}$ $I_G=-100\mu\text{A}$ (Note 1, 2)		160		nC
Gate Source Charge	Q_{GS}			13		nC
Gate Drain Charge	Q_{GD}			15		nC
Turn-ON Delay Time	$t_{D(ON)}$	$V_{DD}=-30\text{V}, V_{GS}=-10\text{V}, I_D=-0.5\text{A}$ $R_G=25\Omega$ (Note 1, 2)		50		ns
Turn-ON Rise Time	t_R			150		ns
Turn-OFF Delay Time	$t_{D(OFF)}$			400		ns
Turn-OFF Fall-Time	t_F			260		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Body-Diode Continuous Current	I_S				-17	A
Maximum Pulsed Drain-Source Diode Forward Current	I_{SM}				-52	A
Diode Forward Voltage	V_{SD}	$V_{GS}=0\text{V}, I_S=-17\text{A}$			-6	V
Body Diode Reverse Recovery Time	t_{rr}	$V_{GS}=0\text{V}, I_S=-17\text{A}$		152		ns
Body Diode Reverse Recovery Charge	Q_{rr}	$di_F/dt=100\text{A}/\mu\text{s}$ (Note 1)		0.72		μC

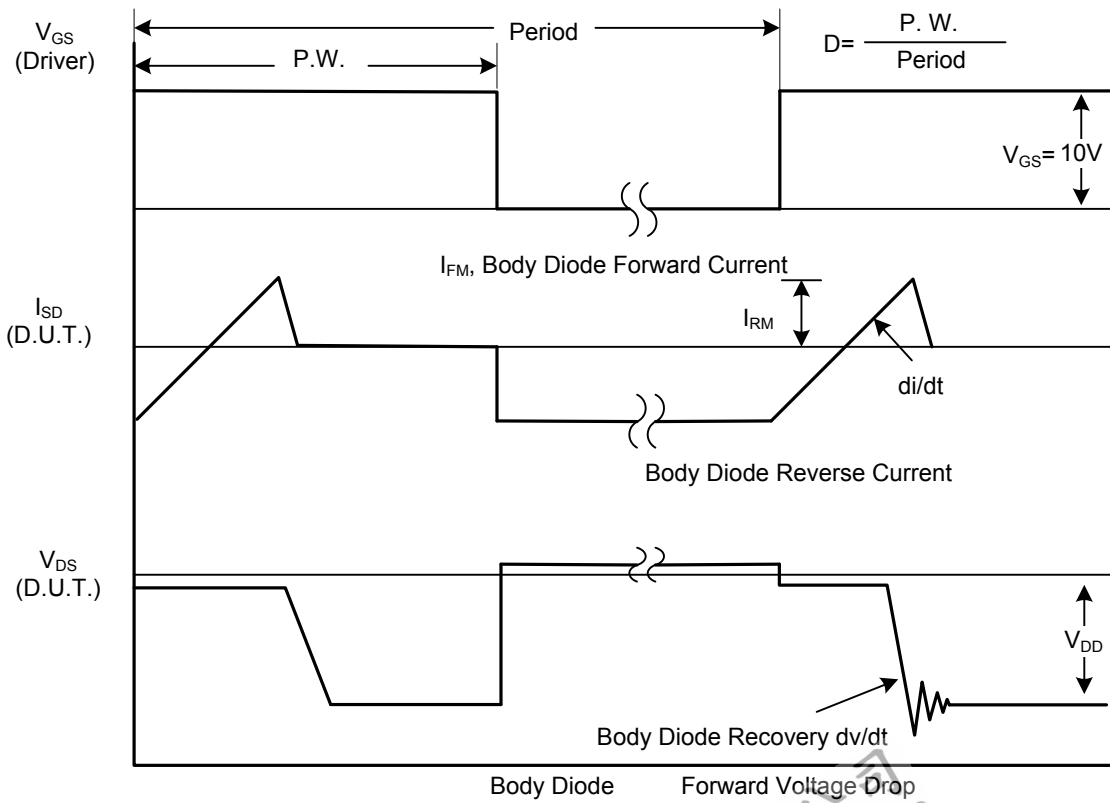
Notes: 1. Pulse Test : Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

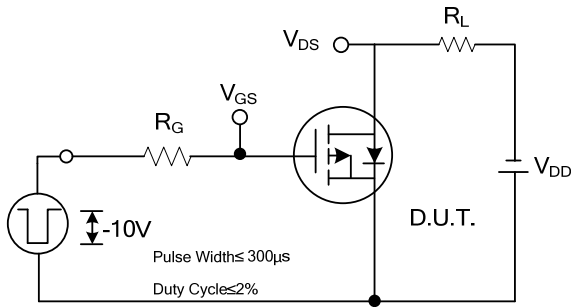


Peak Diode Recovery dv/dt Test Circuit

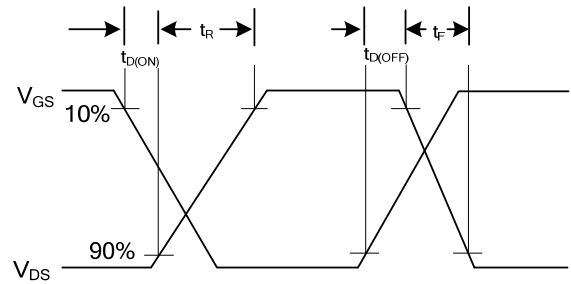


Peak Diode Recovery dv/dt Waveforms

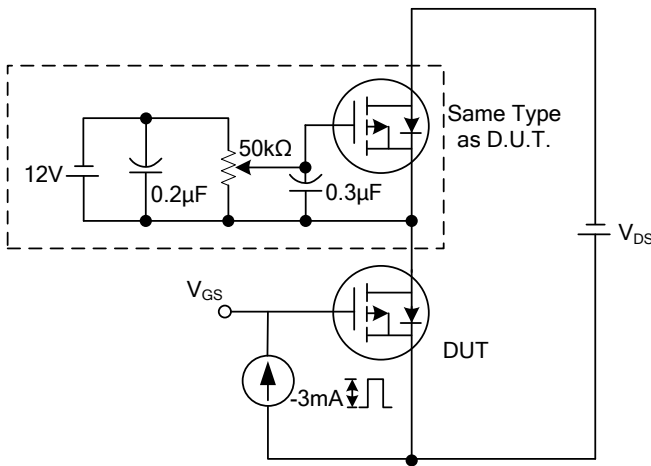
■ TEST CIRCUITS AND WAVEFORMS (Cont.)



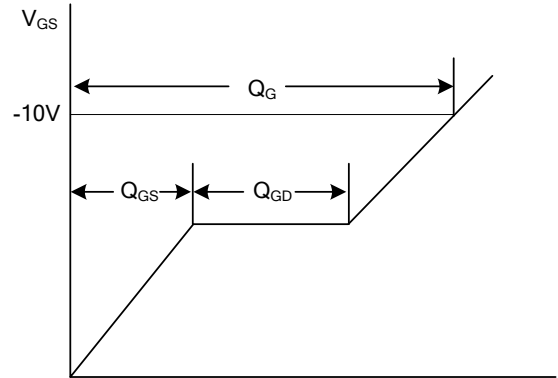
Switching Test Circuit



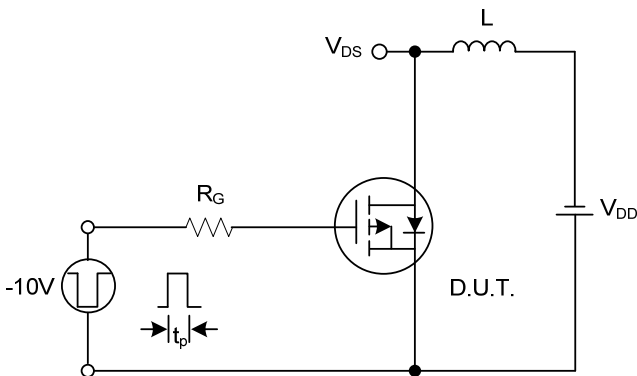
Switching Waveforms



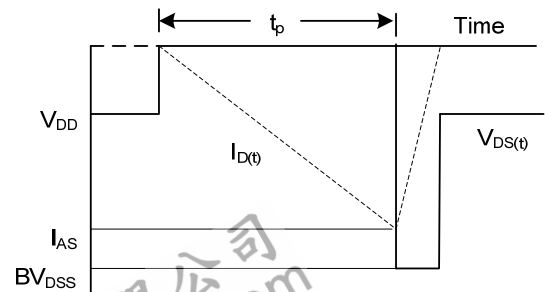
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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