



UNISONIC TECHNOLOGIES CO., LTD

20N65K-MT

Power MOSFET

20A, 650V N-CHANNEL POWER MOSFET

■ DESCRIPTION

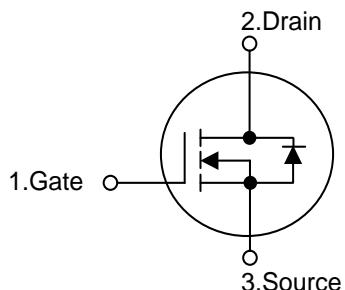
The UTC **20N65K-MT** is an N-channel Power MOSFET using UTC's advanced technology to provide customers a minimum on-state resistance and superior switching performance, etc.

The UTC **20N65K-MT** is generally applied in high efficient AC to DC converters, PWM motor controls and bridge circuits, etc.

■ FEATURES

- * $R_{DS(ON)} \leq 0.55 \Omega$ @ $V_{GS}=10V$, $I_D=10A$
- * High Switching Speed
- * Improved dv/dt capability

■ SYMBOL



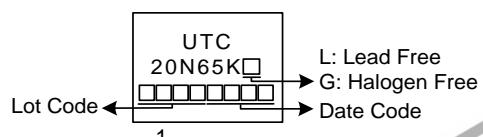
■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
20N65KL-TF1-T	20N65KG-TF1-T	TO-220F1	G	D	S	Tube
20N65KL-TF2-T	20N65KG-TF2-T	TO-220F2	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

20N65KG-TF1-T	(1)T: Tube (2)TF1: TO-220F1, TF2: TO-220F2 (3)G: Halogen Free and Lead Free, L: Lead Free
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■ MARKING



■ ABSOLUTE MAXIMUM RATINGS ($T_c = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	650	V
Gate-Source Voltage		V_{GSS}	± 30	V
Drain Current	Continuous	I_D	20	A
	Pulsed (Note 2)	I_{DM}	40	A
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	562	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	2.46	V/ns
Power Dissipation		P_D	55	W
Junction Temperature		T_J	+150	$^\circ\text{C}$
Storage Temperature		T_{STG}	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.
 Absolute maximum ratings are stress ratings only and functional device operation is not implied.
 2. Repetitive Rating: Pulse width limited by maximum junction temperature.
 3. $L = 10\text{mH}$, $I_{AS} = 10.5\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 25 \Omega$ Starting $T_J = 25^\circ\text{C}$
 4. $I_{SD} \leq 20\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$

■ THERMAL DATA

PARAMETER		SYMBOL	RATING	UNIT
Junction to Ambient		θ_{JA}	62.5	$^\circ\text{C/W}$
Junction to Case		θ_{JC}	2.27	$^\circ\text{C/W}$

■ ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, unless otherwise specified)

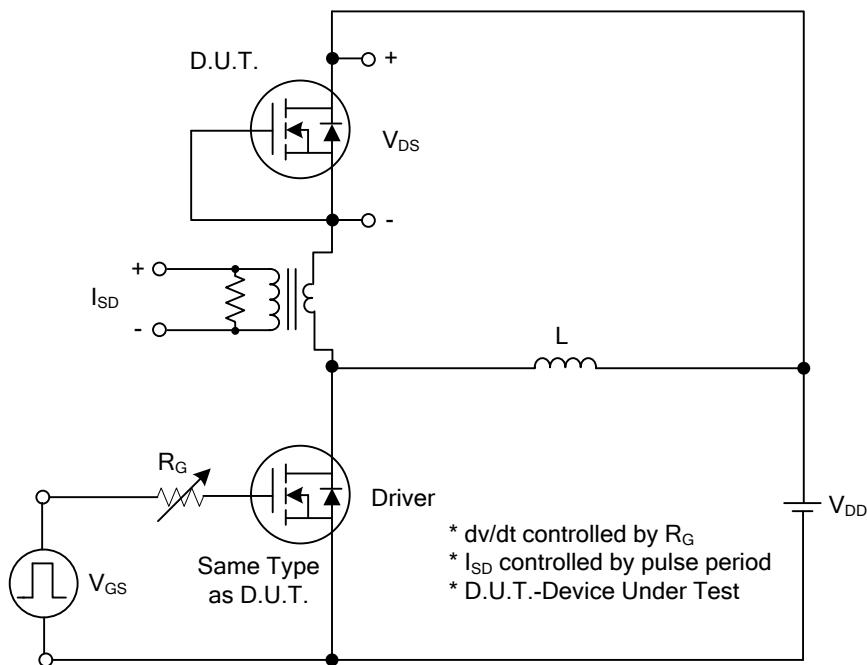
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0\text{V}$, $I_D = 250\mu\text{A}$	650			V
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=650\text{V}$, $V_{GS}=0\text{V}$			10	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=30\text{V}$, $V_{DS}=0\text{V}$			100	nA
		$V_{GS}=-30\text{V}$, $V_{DS}=0\text{V}$			-100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	2.0		4.0	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=10\text{A}$		0.515	0.55	Ω
DYNAMIC CHARACTERISTICS						
Input Capacitance	C_{iss}	$V_{GS}=0\text{V}$, $V_{DS}=25\text{V}$, $f=1.0\text{MHz}$		2512		pF
Output Capacitance	C_{oss}			231		pF
Reverse Transfer Capacitance	C_{rss}			14		pF
SWITCHING CHARACTERISTICS						
Total Gate Charge (Note 1)	Q_G	$V_{DS}=100\text{V}$, $V_{GS}=10\text{V}$, $I_D=20\text{A}$ $I_c=1\text{mA}$ (Note 1, 2)		54		nC
Gate-Source Charge	Q_{GS}			10		nC
Gate-Drain Charge	Q_{GD}			13		nC
Turn-on Delay Time (Note 1)	$t_{D(ON)}$	$V_{DS}=100\text{V}$, $V_{GS}=10\text{V}$, $I_D=20\text{A}$, $R_G=25\Omega$ (Note 1, 2)		28		ns
Rise Time	t_R			35		ns
Turn-off Delay Time	$t_{D(OFF)}$			140		ns
Fall-Time	t_F			76		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Body-Diode Continuous Current	I_S				20	A
Maximum Body-Diode Pulsed Current	I_{SM}				40	A
Drain-Source Diode Forward Voltage (Note 1)	V_{SD}	$V_{GS}=0\text{V}$, $I_S=20\text{A}$			1.4	V
Reverse Recovery Time (Note 1)	t_{rr}	$V_{GS}=0\text{V}$, $I_S=20\text{A}$, $di_F/dt=100\text{A}/\mu\text{s}$ (Note 1)		506		ns
Reverse Recovery Charge	Q_{rr}			9		μC

Notes: 1. Pulse Test : Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.

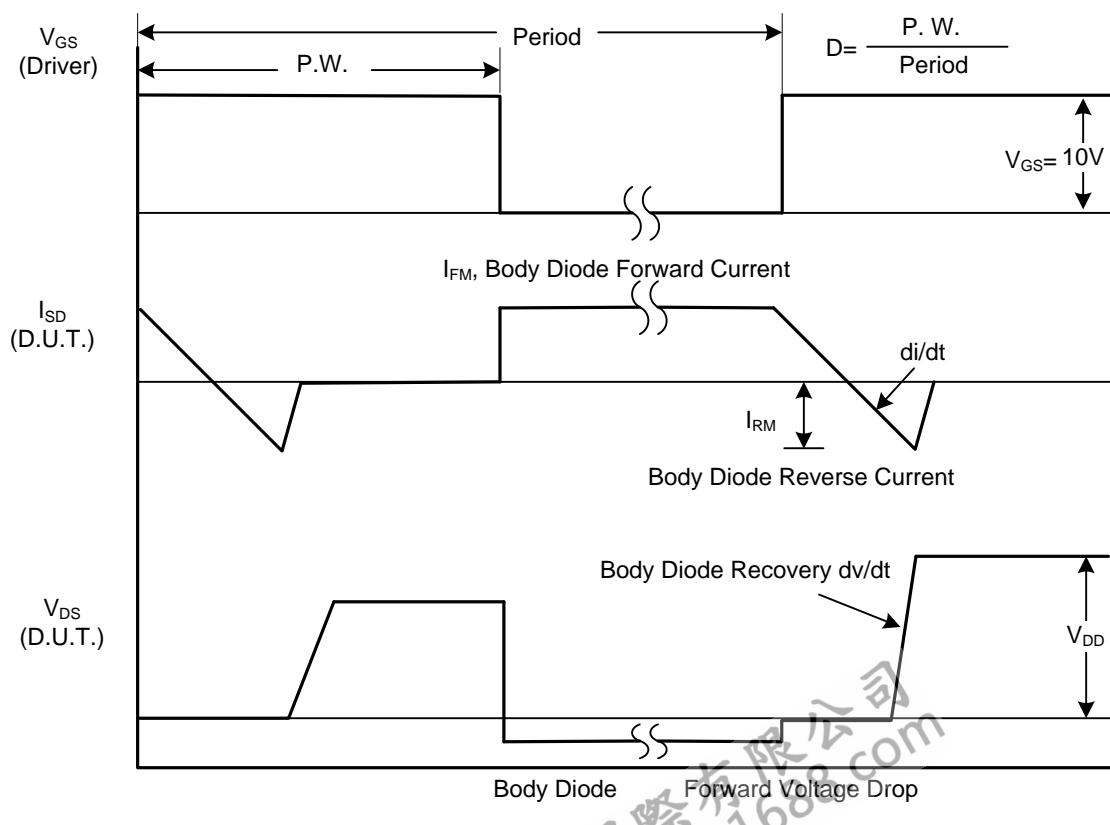
2. Essentially independent of operating temperature.



■ TEST CIRCUITS AND WAVEFORMS

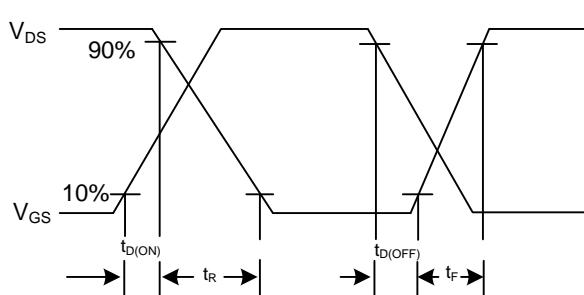
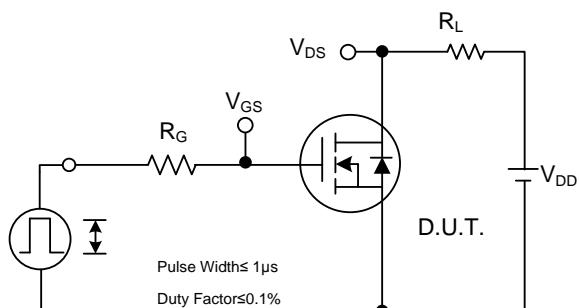


Peak Diode Recovery dv/dt Test Circuit



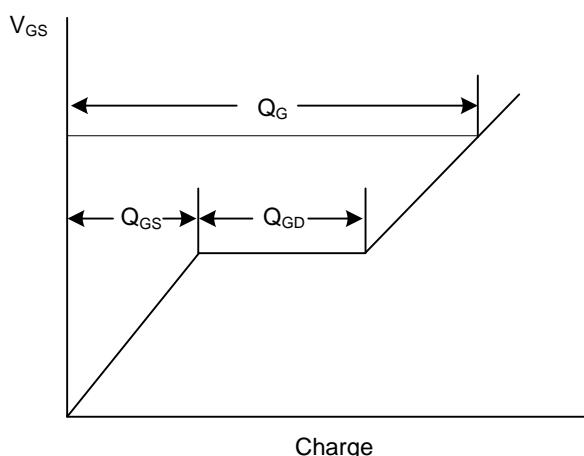
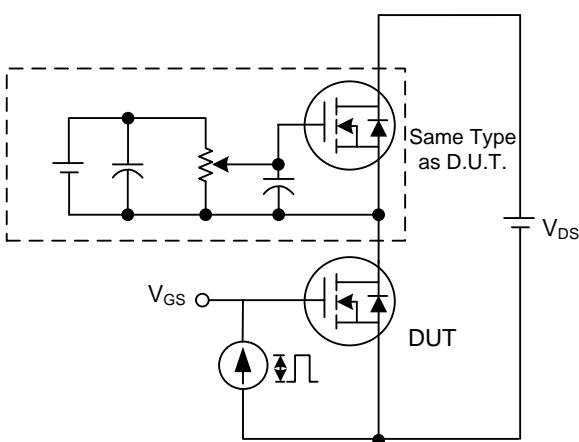
Peak Diode Recovery dv/dt Waveforms

■ TEST CIRCUITS AND WAVEFORMS



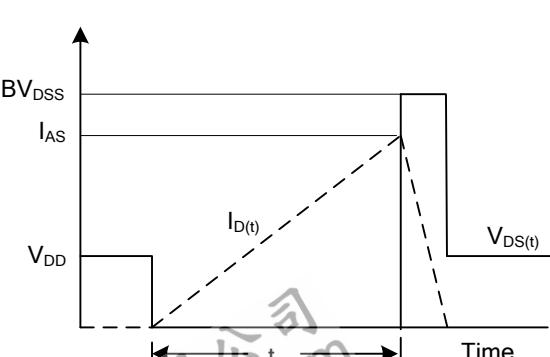
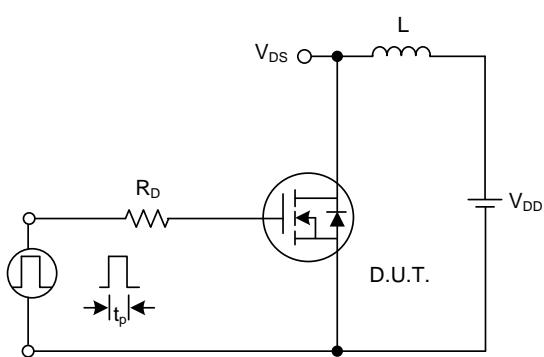
Switching Test Circuit

Switching Waveforms



Gate Charge Test Circuit

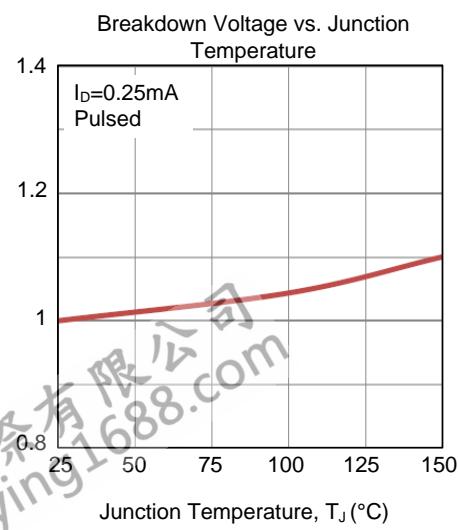
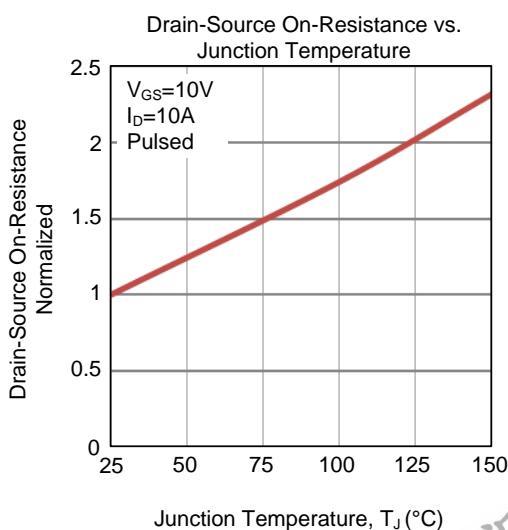
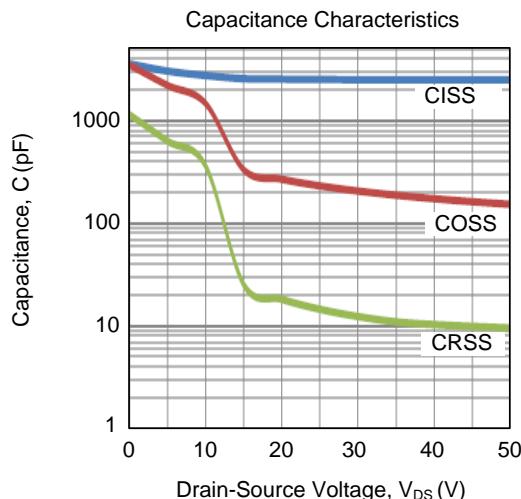
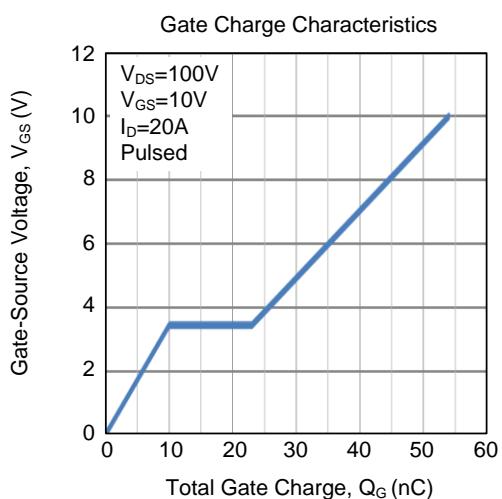
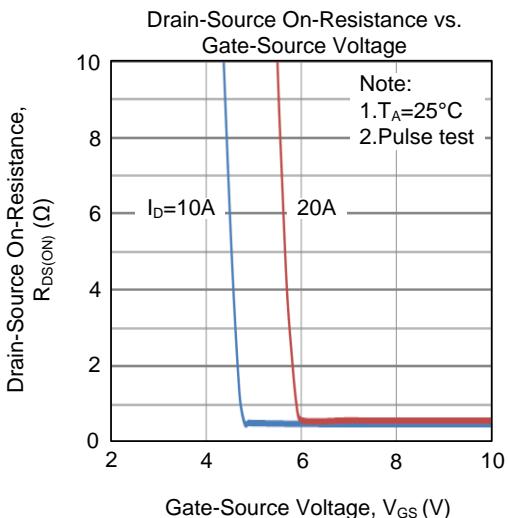
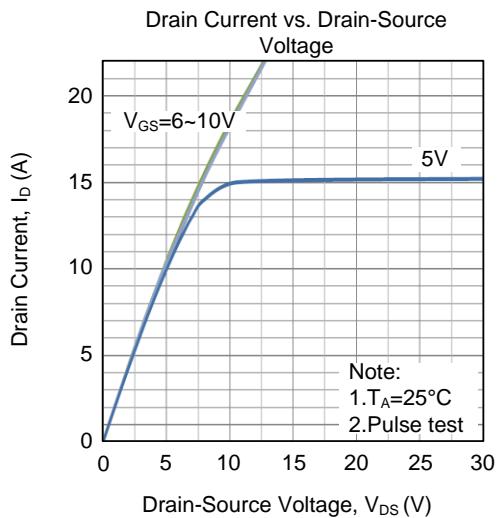
Gate Charge Waveform



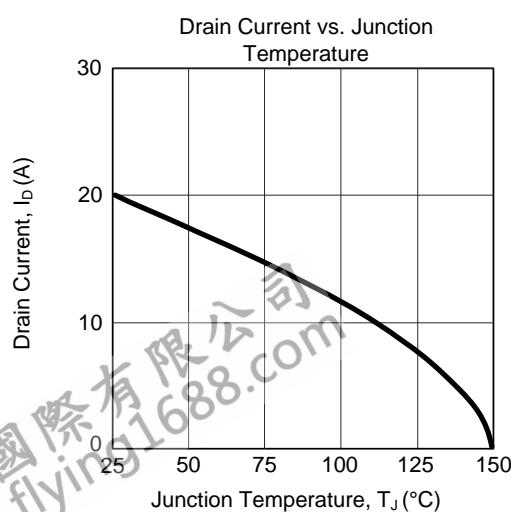
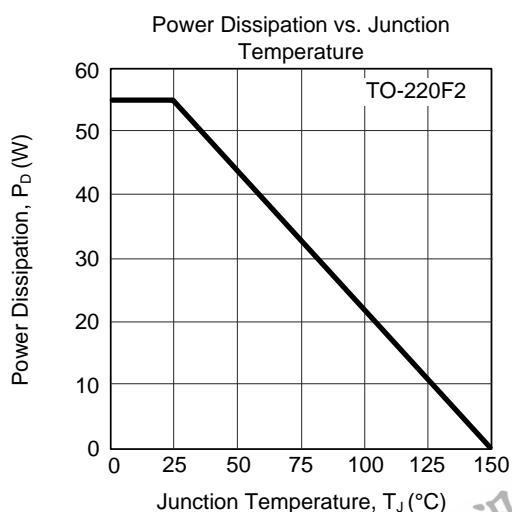
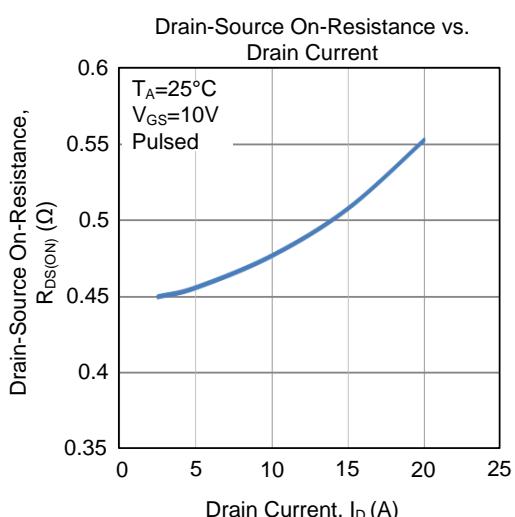
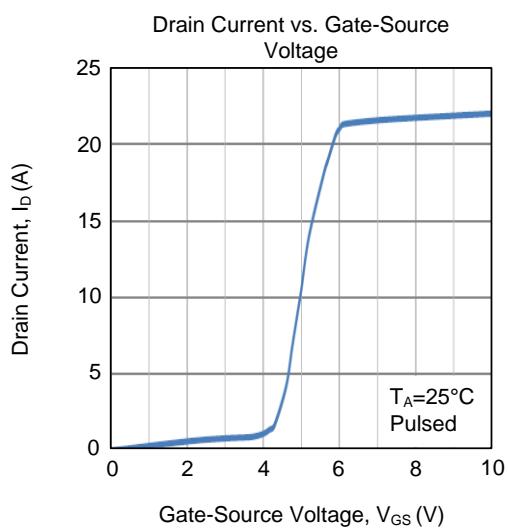
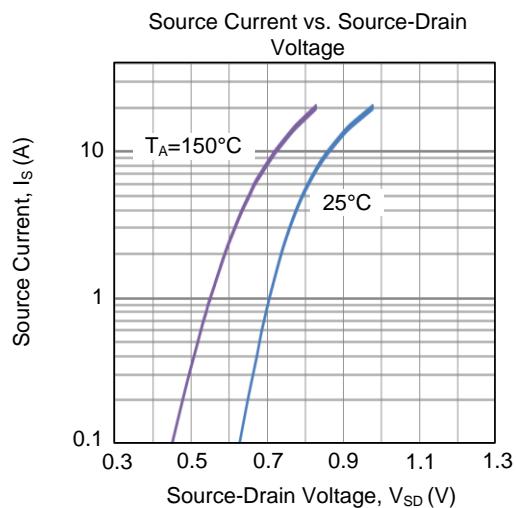
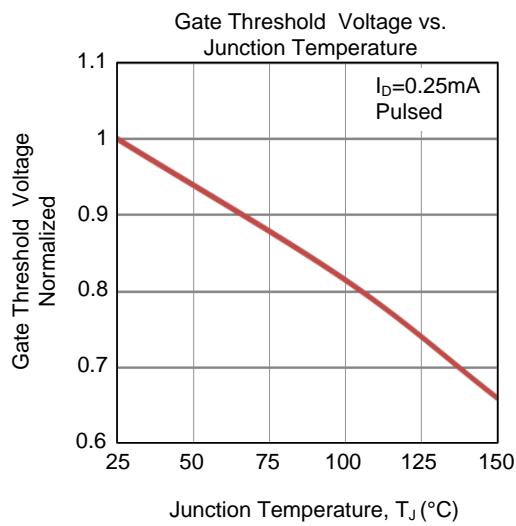
Unclamped Inductive Switching Test Circuit

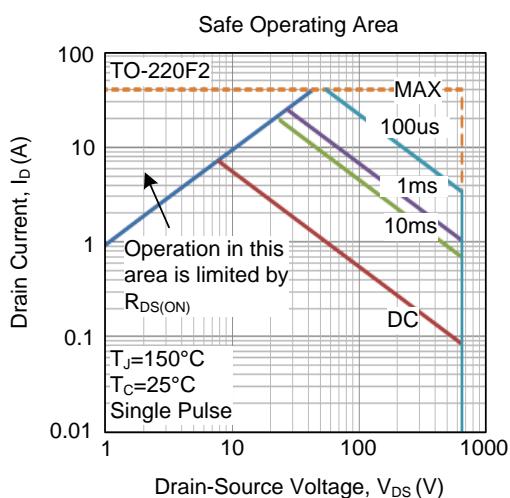
Unclamped Inductive Switching Waveforms

■ TYPICAL CHARACTERISTICS



■ TYPICAL CHARACTERISTICS (Cont.)



■ TYPICAL CHARACTERISTICS (Cont.)

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