



2N50Q-TA

Power MOSFET

2A, 500V N-CHANNEL POWER MOSFET

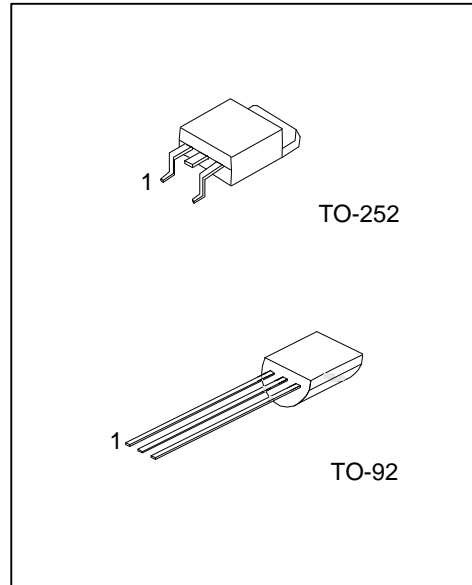
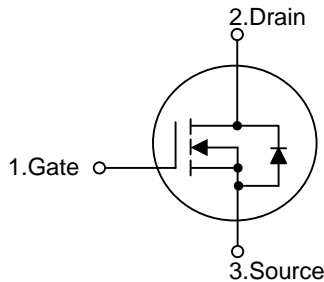
DESCRIPTION

The UTC 2N50Q-TA is a high voltage MOSFET and is designed to have better characteristics, such as fast switching time, low gate charge, low on-state resistance and have a high rugged avalanche characteristics. This power MOSFET is usually used at high speed switching applications in power supplies, PWM motor controls, high efficient AC to DC converters and bridge circuits.

FEATURES

- * $R_{DS(ON)} \leq 5.5\Omega$ @ $V_{GS}=10V, I_D=1.0A$
- * High Switching Speed
- * 100% Avalanche Tested

SYMBOL



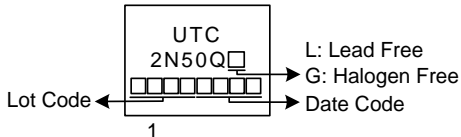
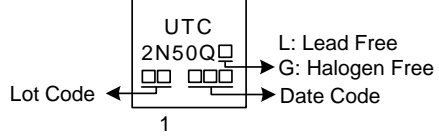
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
2N50QL-TN3-R	2N50QG-TN3-R	TO-252	G	D	S	Tape Reel
2N50QL-T92-B	2N50QG-T92-B	TO-92	G	D	S	Tape Box
2N50QL-T92-K	2N50QG-T92-K	TO-92	G	D	S	Bulk

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>2N50QG-TN3-R</p> <p>(1)Packing Type</p> <p>(2)Package Type</p> <p>(3)Green Package</p>	<p>(1) R: Tape Reel, B: Tape Box, K: Bulk</p> <p>(2) TN3: TO-252, T92: TO-92</p> <p>(3) G: Halogen Free and Lead Free, L: Lead Free</p>
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MARKING

TO-252	TO-92
 <p>Diagram showing the marking on a TO-252 package. The marking includes 'UTC', '2N50Q', a Lot Code (represented by a row of six boxes), and a Date Code (represented by a row of three boxes). The number '1' is located below the Lot Code. To the right of the package, there are three labels: 'L: Lead Free', 'G: Halogen Free', and 'Date Code', each with an arrow pointing to its corresponding marking area.</p>	 <p>Diagram showing the marking on a TO-92 package. The marking includes 'UTC', '2N50Q', a Lot Code (represented by a row of three boxes), and a Date Code (represented by a row of three boxes). The number '1' is located below the Lot Code. To the right of the package, there are three labels: 'L: Lead Free', 'G: Halogen Free', and 'Date Code', each with an arrow pointing to its corresponding marking area.</p>

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■ ABSOLUTE MAXIMUM RATINGS (T_C=25°C, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V _{DSS}	500	V
Gate-Source Voltage		V _{GSS}	±30	V
Drain Current	Continuous	I _D	2	A
	Pulsed (Note 2)	I _{DM}	4	A
Avalanche Current (Note 2)		I _{AR}	1.4	A
Avalanche Energy (Note 3)	Single Pulsed	E _{AS}	40	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	1.4	V/ns
Power Dissipation	TO-252	P _D	30	W
	TO-92		1.42	W
Junction Temperature		T _J	+150	°C
Storage Temperature		T _{STG}	-55 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. L=41mH, I_{AS}=1.4A, V_{DD}=50V, R_G=25 Ω, Starting T_J = 25°C

4. I_{SD}≤2.0A, di/dt≤200A/μs, V_{DD}≤BV_{DSS}, Starting T_J=25°C

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	TO-252	θ _{JA}	110	°C/W
	TO-92		60	°C/W
Junction to Case	TO-252	θ _{JC}	4.17 (Note)	°C/W
	TO-92		88	°C/W

Note: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

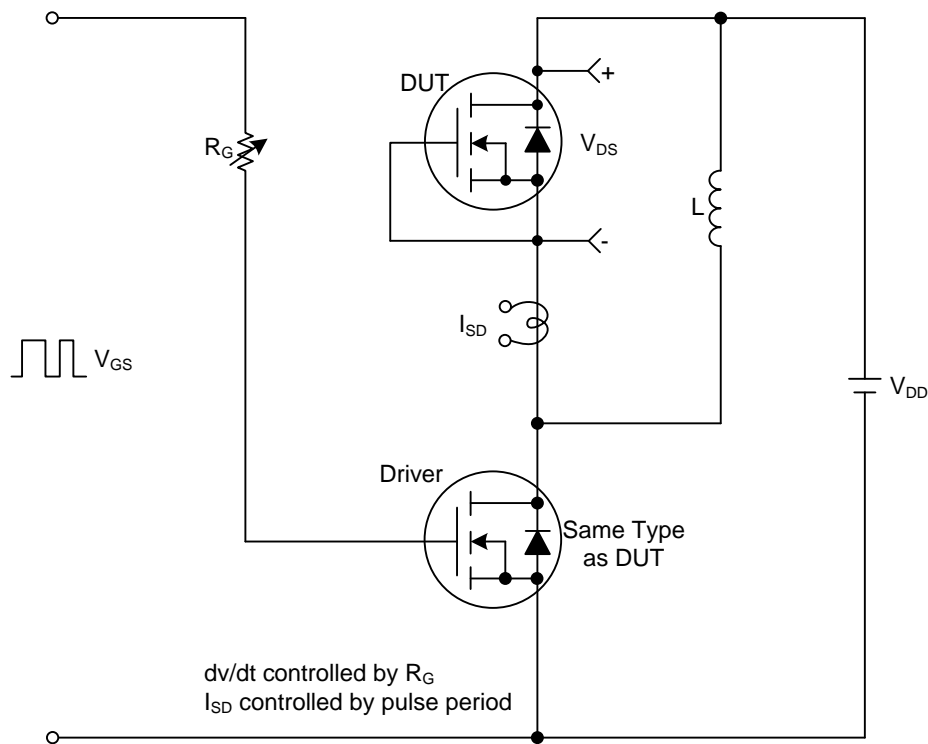
■ **ELECTRICAL CHARACTERISTICS** ($T_C=25^\circ\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	500			V
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=500\text{V}$, $V_{GS}=0\text{V}$			10	μA
Gate- Source Leakage Current	Forward	I_{GSS} $V_{GS}=+30\text{V}$, $V_{DS}=0\text{V}$			+100	nA
	Reverse				-100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	2.0		4.0	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=1.0\text{A}$			5.5	Ω
DYNAMIC PARAMETERS						
Input Capacitance	C_{ISS}	$V_{GS}=0\text{V}$, $V_{DS}=25\text{V}$, $f=1.0\text{MHz}$		140		pF
Output Capacitance	C_{OSS}			22		pF
Reverse Transfer Capacitance	C_{RSS}			3		pF
SWITCHING PARAMETERS						
Total Gate Charge	Q_G	$V_{DS}=400\text{V}$, $V_{GS}=10\text{V}$, $I_D=2\text{A}$, $I_G=1\text{mA}$ (Note 1, 2)		4.9		nC
Gate to Source Charge	Q_{GS}			2.3		nC
Gate to Drain Charge	Q_{GD}			0.8		nC
Turn-ON Delay Time	$t_{D(ON)}$	$V_{DD}=100\text{V}$, $V_{GS}=1.0\text{V}$, $I_D=2\text{A}$, $R_G=25\Omega$ (Note 1, 2)		4		ns
Rise Time	t_R			15		ns
Turn-OFF Delay Time	$t_{D(OFF)}$			12		ns
Fall-Time	t_F			24		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Body-Diode Continuous Current	I_S				2	A
Maximum Body-Diode Pulsed Current	I_{SM}				4	A
Drain-Source Diode Forward Voltage	V_{SD}	$I_S=2.0\text{A}$, $V_{GS}=0\text{V}$			1.2	V
Reverse Recovery Time	t_{RR}	$V_{GS}=0\text{V}$, $I_{SD}=2.0\text{A}$, $di/dt=100\text{A}/\mu\text{s}$		280		ns
Reverse Recovery Charge	Q_{RR}			0.58		μC

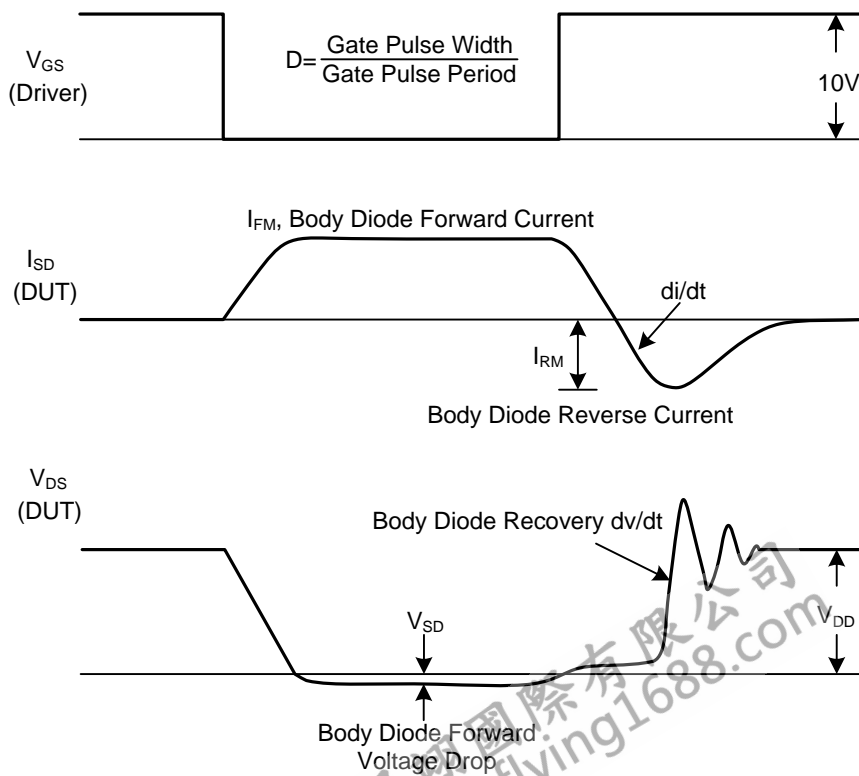
Notes: 1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating temperature.

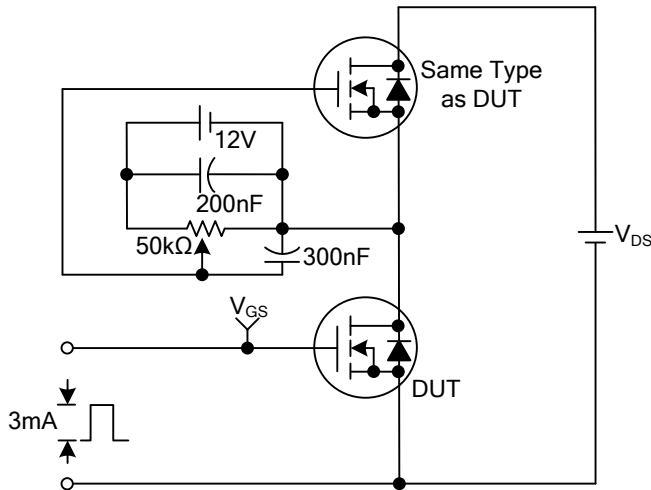
TEST CIRCUITS AND WAVEFORMS



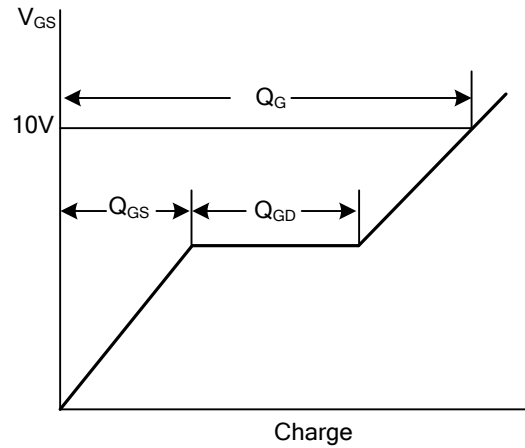
Peak Diode Recovery dv/dt Test Circuit & Waveforms



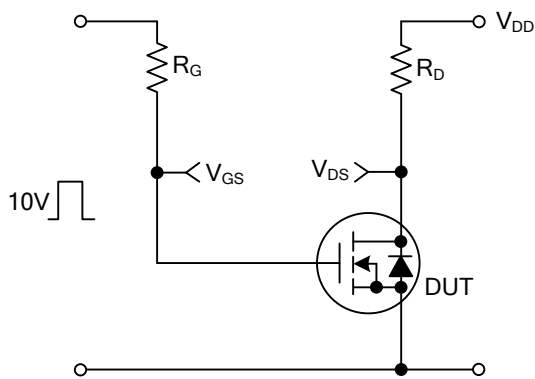
TEST CIRCUITS AND WAVEFORMS



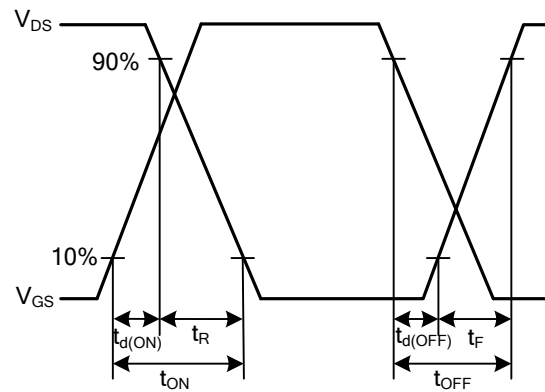
Gate Charge Test Circuit



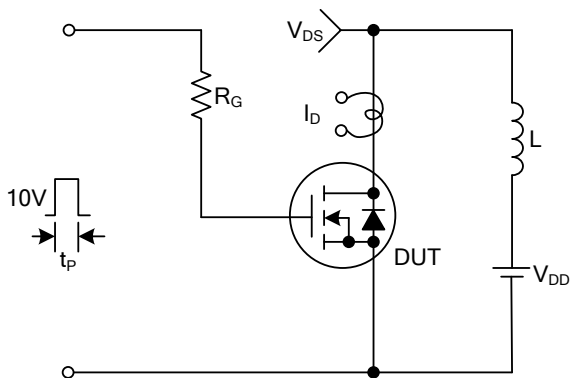
Gate Charge Waveforms



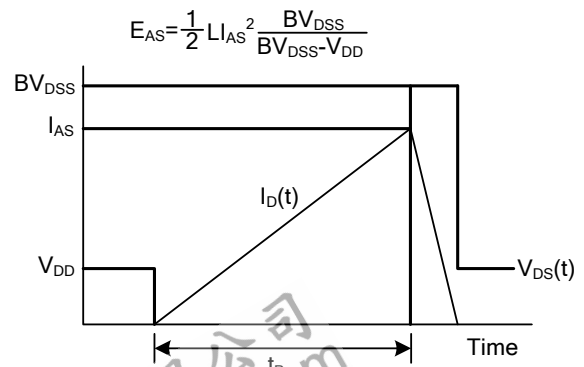
Resistive Switching Test Circuit



Resistive Switching Waveforms



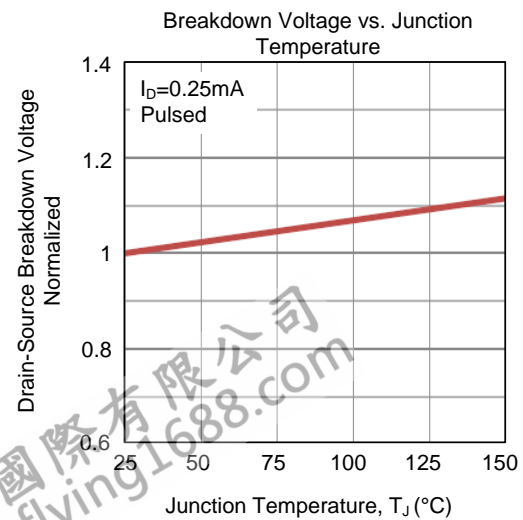
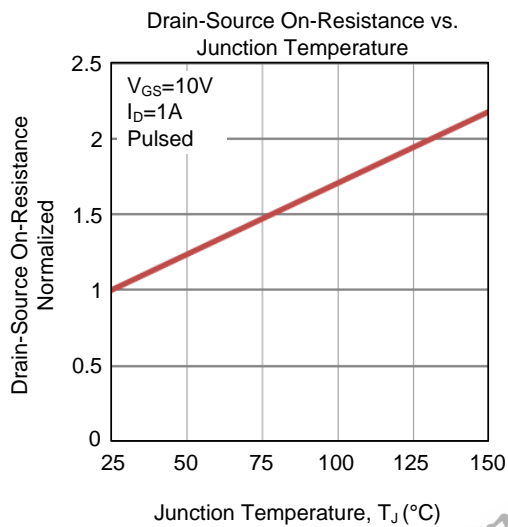
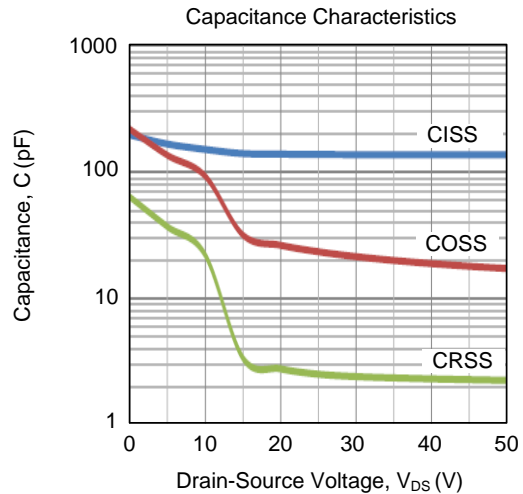
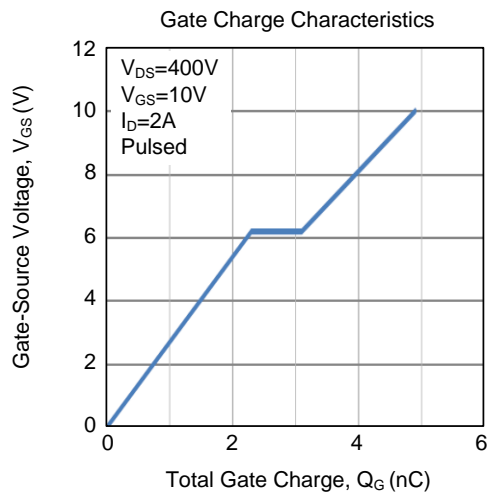
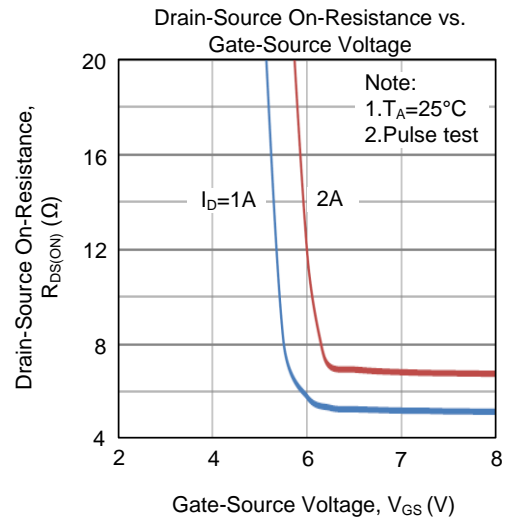
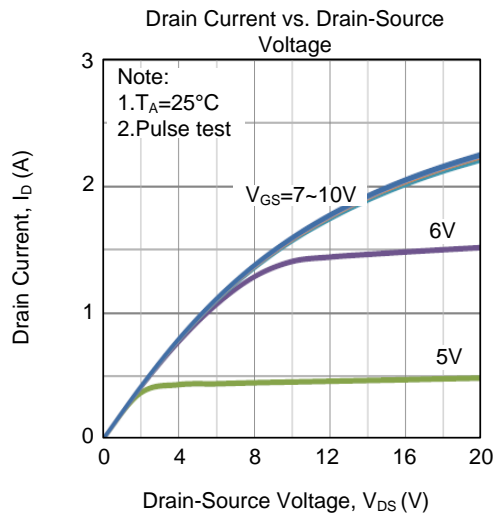
Unclamped Inductive Switching Test Circuit



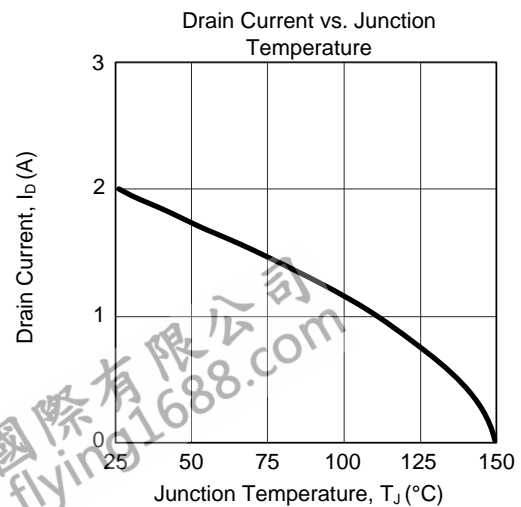
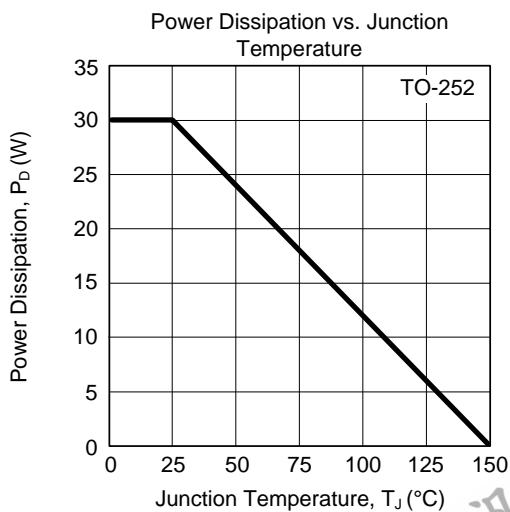
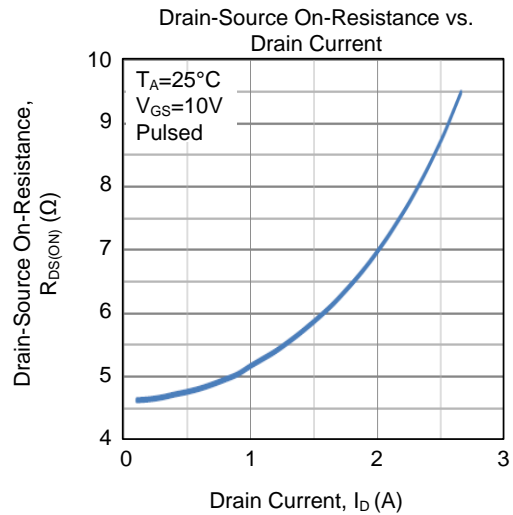
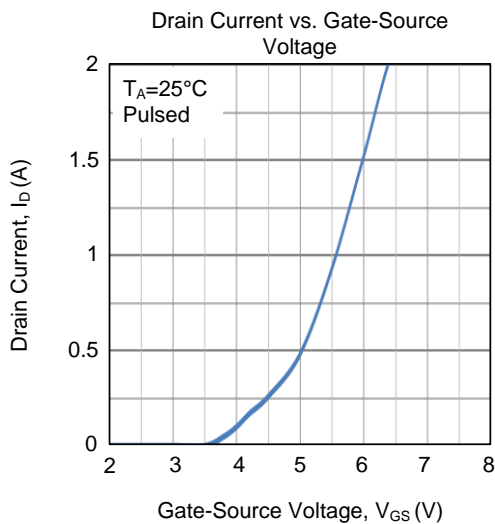
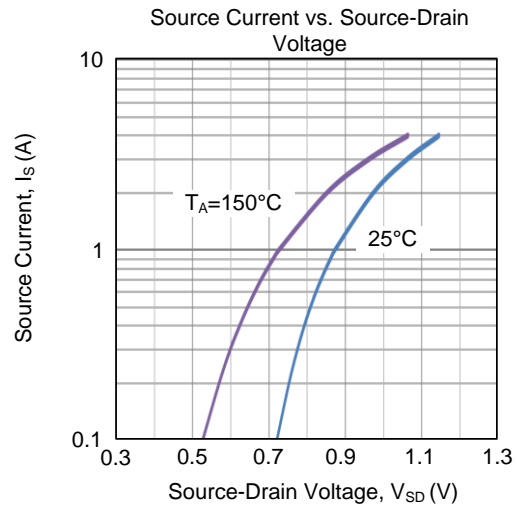
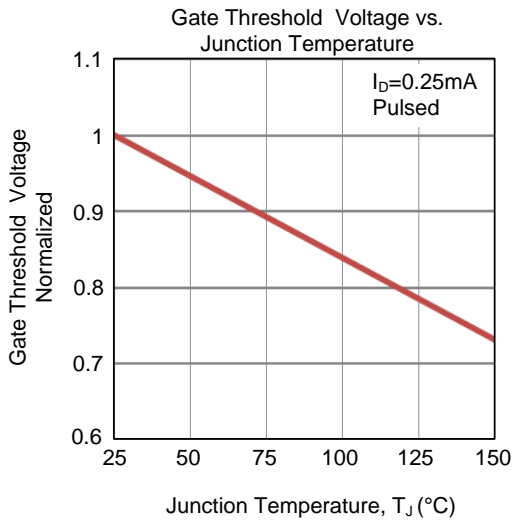
Unclamped Inductive Switching Waveforms

$$E_{AS} = \frac{1}{2} L I_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$

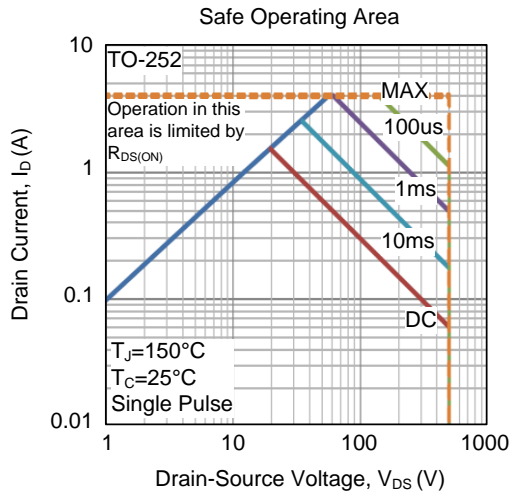
TYPICAL CHARACTERISTICS



■ TYPICAL CHARACTERISTICS (Cont.)



■ **TYPICAL CHARACTERISTICS (Cont.)**



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