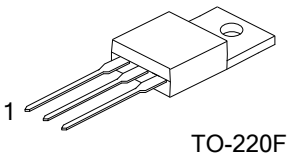
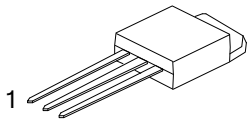
2 Amps, 700 Volts N-CHANNEL POWER MOSFET



TO-220F



TO-251

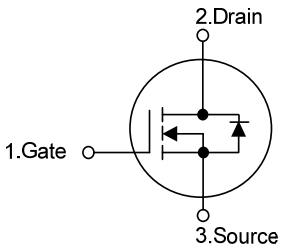
■ DESCRIPTION

The UTC **2N70-M** is a high voltage MOSFET designed to have better characteristics, such as fast switching time, low gate charge, low on-state resistance and high rugged avalanche characteristics. This power MOSFET is usually used at high speed switching applications in power supplies, PWM motor controls, high efficient DC to DC converters and bridge circuits.

■ FEATURES

* $R_{DS(ON)}$ < 6.3Ω @ V_{GS} = 10V
* Ultra Low gate charge (typical 17.2nC)
* Low reverse transfer capacitance (C_{RSS} = typical 5.0 pF)
* Fast switching capability
* Avalanche energy specified
* Improved dv/dt capability, high ruggedness

■ SYMBOL



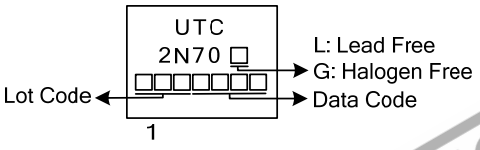
■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
2N70L-TF3-T	2N70G-TF3-T	TO-220F	G	D	S	Tube
2N70L-TM3-T	2N70G-TM3-T	TO-251	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

2N70L-TA3-T (1)Packing Type (2)Package Type (3)Green Package	(1) T: Tube (2) TF3: TO-220F, TM3: TO-251 (3) L: Lead Free, G: Halogen Free and Lead Free

■ MARKING



■ ABSOLUTE MAXIMUM RATINGS (T_C = 25°C, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	700	V
Gate-Source Voltage		V_{GSS}	±30	V
Avalanche Current (Note 2)		I_{AR}	2.0	A
Drain Current	Continuous	I_D	2.0	A
	Pulsed (Note 2)	I_{DM}	8.0	A
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	140	mJ
	Repetitive (Note 2)	E_{AR}	2.8	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	4.5	V/ns
Power Dissipation	TO-220F	P_D	48	W
	TO-251		30	W
Junction Temperature		T_J	+150	°C
Storage Temperature		T_{STG}	-55 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. Repetitive Rating : Pulse width limited by T_J
3. L=64mH, I_{AS}=2A, V_{DD}=50V, R_G=25 Ω, Starting T_J = 25°C
4. I_{SD}≤2.0A, di/dt≤200A/μs, V_{DD}≤ BV_{DSS}, Starting T_J = 25°C

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	TO-220F	θ_{JA}	62.5	°C/W
	TO-251		110	°C/W
Junction to Case	TO-220F	θ_{JC}	2.6	°C/W
	TO-251		4.24	°C/W

■ ELECTRICAL CHARACTERISTICS (T_J=25°C, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV_{DSS}	V_{GS} = 0V, I_D = 250μA	700			V
Drain-Source Leakage Current		I_{DSS}	V_{DS} = 700V, V_{GS} = 0V			10	μA
			V_{DS} = 560V, V_{GS} = 0V, T_J =125°C			100	μA
Gate-Source Leakage Current	Forward	I_{GSS}	V_{GS} = 30V, V_{DS} = 0V			100	nA
	Reverse		V_{GS} = -30V, V_{DS} = 0V			-100	nA
Breakdown Voltage Temperature Coefficient		$\triangle BV_{DSS}/\triangle T_J$	I_D = 250 μA, Referenced to 25°C		0.4		V/°C
ON CHARACTERISTICS							
Gate Threshold Voltage		$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0		4.0	V
Static Drain-Source On-State Resistance		$R_{DS(ON)}$	V_{GS} = 10V, I_D =1A		5.4	6.3	Ω
DYNAMIC CHARACTERISTICS							
Input Capacitance		C_{ISS}	V_{DS} =25V, V_{GS} =0V, f =1MHz		270	350	pF
Output Capacitance		C_{OSS}			38	50	pF
Reverse Transfer Capacitance		C_{RSS}			5	7	pF
SWITCHING CHARACTERISTICS							
Turn-On Delay Time		$t_{D\ (ON)}$	V_{DD} =30V, I_D =0.5A, R_G=25Ω (Note 1, 2)		35	40	ns
Turn-On Rise Time		t_R			65	70	ns
Turn-Off Delay Time		$t_{D(OFF)}$			105	115	ns
Turn-Off Fall Time		t_F			50	70	ns
Total Gate Charge		Q_G	V_{DS}=560V, V_{GS}=10V, I_D=2.0A (Note 1, 2)		17.2		nC
Gate-Source Charge		Q_{GS}			1.7		nC
Gate-Drain Charge		Q_{GD}			4.4		nC
DRAIN-SOURCE DIODE CHARACTERISTICS							
Drain-Source Diode Forward Voltage		V_{SD}	V_{GS} = 0 V, I_{SD} = 2.0 A			1.4	V
Continuous Drain-Source Current		I_{SD}				2.0	A
Pulsed Drain-Source Current		I_{SM}				8.0	A
Reverse Recovery Time		t_{RR}	V_{GS} = 0 V, I_{SD} = 2.0A di/dt = 100 A/μs (Note1)		260		ns
Reverse Recovery Charge		Q_{RR}			1.09		μC

Notes: 1. Pulse Test: Pulse width≤300μs, Duty cycle≤2%
2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

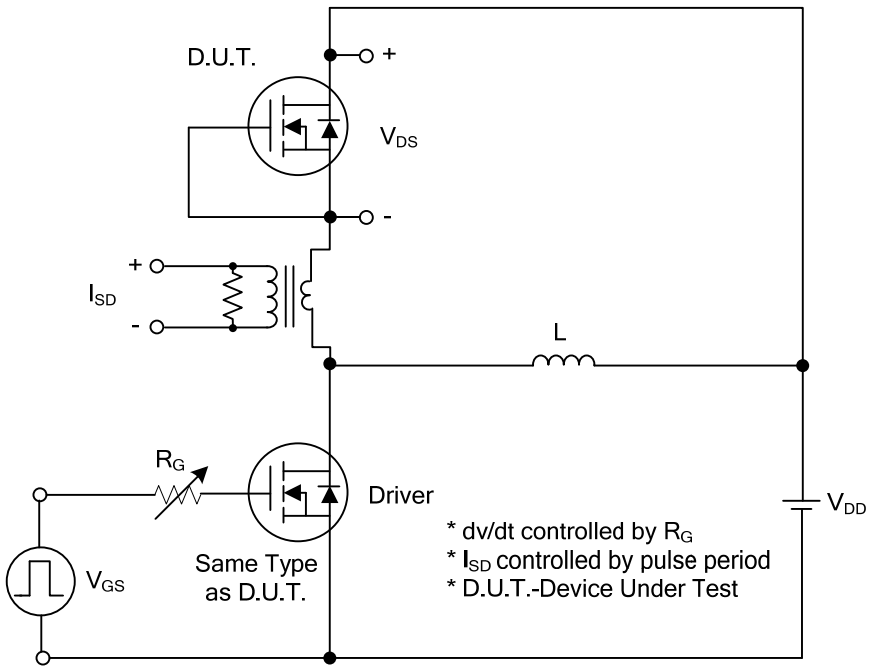


Fig. 1A Peak Diode Recovery dv/dt Test Circuit

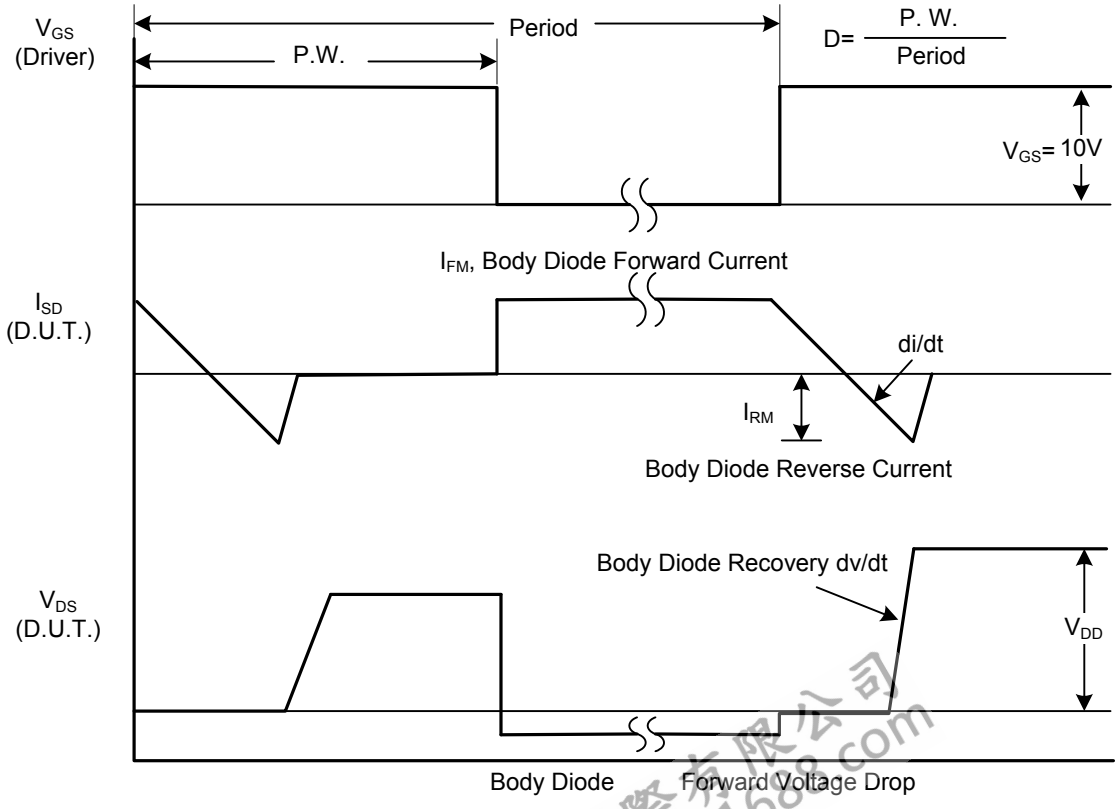


Fig. 1B Peak Diode Recovery dv/dt Waveforms

■ TEST CIRCUITS AND WAVEFORMS (Cont.)

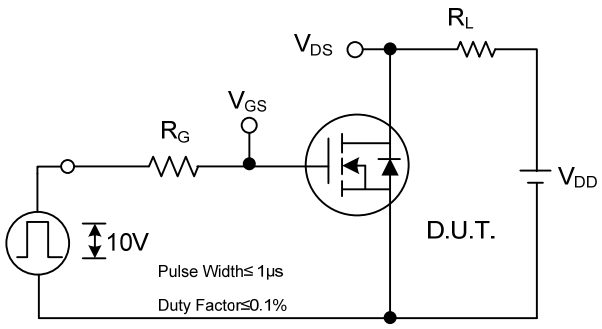


Fig. 2A Switching Test Circuit

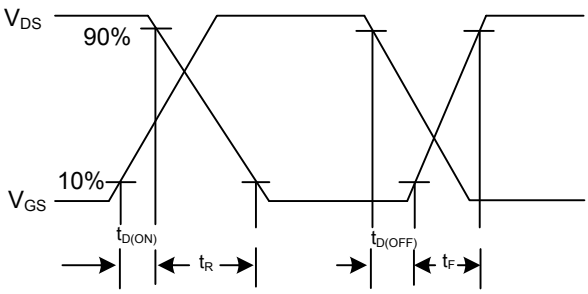


Fig. 2B Switching Waveforms

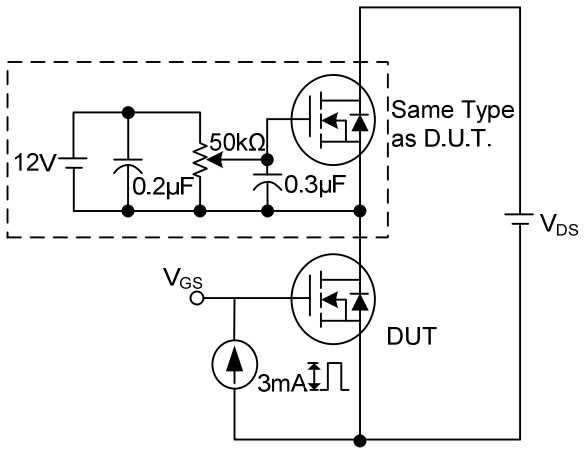


Fig. 3A Gate Charge Test Circuit

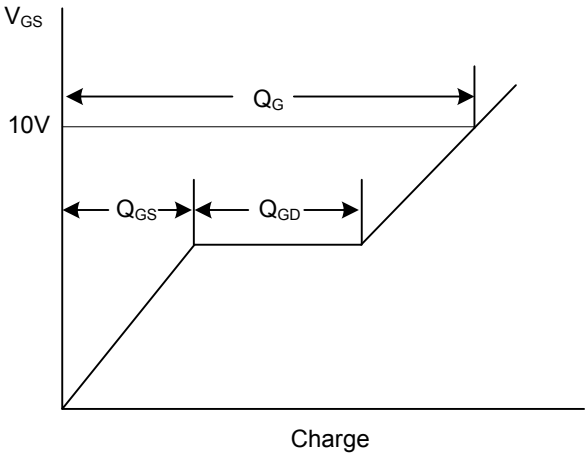


Fig. 3B Gate Charge Waveform

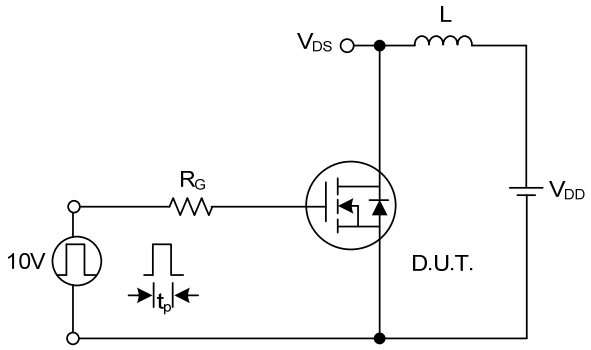


Fig. 4A Unclamped Inductive Switching Test Circuit

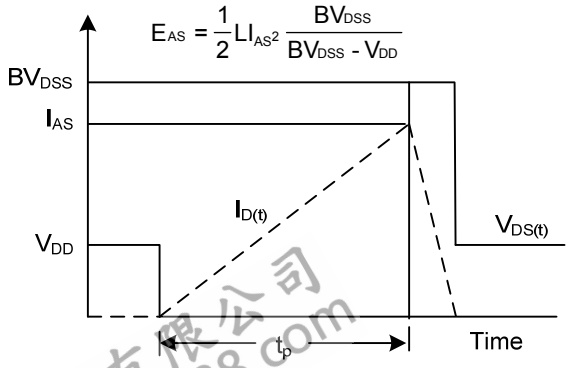


Fig. 4B Unclamped Inductive Switching Waveforms