



## 3N50-LC1

Power MOSFET

### 3A, 500V N-CHANNEL POWER MOSFET

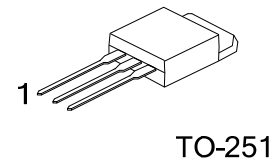
#### DESCRIPTION

The UTC **3N50-LC1** is an N-channel power MOSFET using UTC's advanced technology to provide customers with a minimum on-state resistance and superior switching performance.

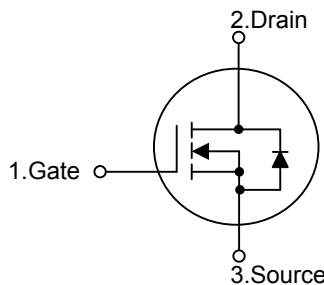
The UTC **3N50-LC1** is generally applied in low power switching mode power appliances and electronic ballast.

#### FEATURES

- \*  $R_{DS(ON)} \leq 3.1\Omega @ V_{GS}=10V, I_D=1.5A$
- \* High Switching Speed
- \* 100% Avalanche Tested



#### SYMBOL



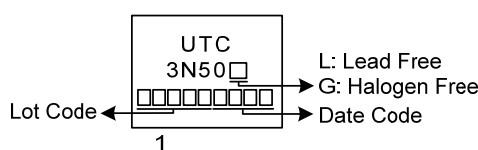
#### ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
3N50L-TM3-T	3N50G-TM3-T	TO-251	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>3N50G-TM3-T</p> <ul style="list-style-type: none"> <li>(1)Packing Type</li> <li>(2)Package Type</li> <li>(3)Green Package</li> </ul>	<ul style="list-style-type: none"> <li>(1) T: Tube</li> <li>(2) TM3: TO-251</li> <li>(3) G: Halogen Free and Lead Free, L: Lead Free</li> </ul>
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#### MARKING



■ ABSOLUTE MAXIMUM RATINGS ( $T_c=25^\circ\text{C}$ , unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		$V_{DSS}$	500	V
Gate-Source Voltage		$V_{GSS}$	$\pm 30$	V
Drain Current	Continuous	$I_D$	3	A
	Pulsed (Note 2)	$I_{DM}$	6	A
Avalanche Energy	Single Pulsed (Note 3)	$E_{AS}$	54.5	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	1.65	V/ns
Power Dissipation		$P_D$	45	W
Junction Temperature		$T_J$	+150	$^\circ\text{C}$
Storage Temperature		$T_{STG}$	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3.  $L = 10\text{mH}$ ,  $I_{AS} = 3.3\text{A}$ ,  $V_{DD} = 50\text{V}$ ,  $R_G = 25\Omega$ , Starting  $T_J = 25^\circ\text{C}$

4.  $I_{SD} \leq 3.0\text{A}$ ,  $di/dt \leq 200\text{A}/\mu\text{s}$ ,  $V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^\circ\text{C}$

■ THERMAL CHARACTERISTICS

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	$\theta_{JA}$	100	$^\circ\text{C}/\text{W}$
Junction to Case	$\theta_{JC}$	2.77 (Note)	$^\circ\text{C}/\text{W}$

Note: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

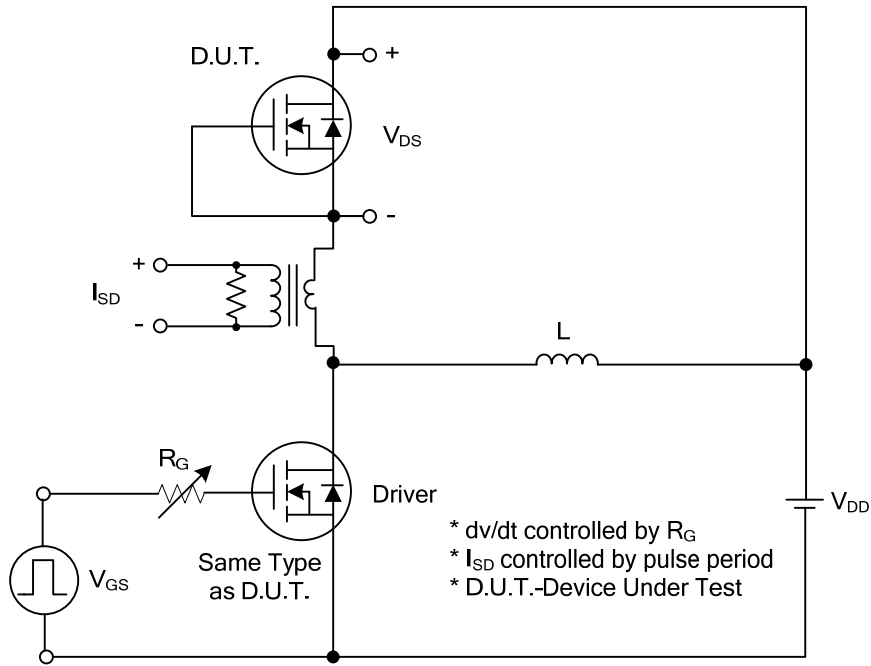
■ ELECTRICAL CHARACTERISTICS ( $T_J=25^\circ\text{C}$ , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>OFF CHARACTERISTICS</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$I_D=250\mu\text{A}$ , $V_{GS}=0\text{V}$	500			V
Drain-Source Leakage Current	$I_{DSS}$	$V_{DS}=500\text{V}$ , $V_{GS}=0\text{V}$			10	$\mu\text{A}$
Gate- Source Leakage Current	Forward	$I_{GSS}$			+100	nA
	Reverse				-100	nA
<b>ON CHARACTERISTICS</b>						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}$ , $I_D=250\mu\text{A}$	2.0		4.0	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$ , $I_D=1.5\text{A}$			3.1	$\Omega$
<b>DYNAMIC PARAMETERS</b>						
Input Capacitance	$C_{ISS}$	$V_{GS}=0\text{V}$ , $V_{DS}=25\text{V}$ , $f=1.0\text{MHz}$		261		pF
Output Capacitance	$C_{OSS}$			34		pF
Reverse Transfer Capacitance	$C_{RSS}$			3		pF
<b>SWITCHING PARAMETERS</b>						
Total Gate Charge (Note 1)	$Q_G$	$V_{DS}=400\text{V}$ , $V_{GS}=10\text{V}$ , $I_D=3\text{A}$ $I_G=1\text{mA}$ (Note 1, 2)		7.3		nC
Gate to Source Charge	$Q_{GS}$			2.9		nC
Gate to Drain Charge	$Q_{GD}$			1		nC
Turn-ON Delay Time (Note 1)	$t_{D(ON)}$	$V_{DD}=100\text{V}$ , $V_{GS}=10\text{V}$ , $I_D=3\text{A}$ , $R_G=25\Omega$ (Note 1, 2)		4		ns
Rise Time	$t_R$			15.5		ns
Turn-OFF Delay Time	$t_{D(OFF)}$			19.3		ns
Fall-Time	$t_F$			22		ns
<b>SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS</b>						
Maximum Body-Diode Continuous Current	$I_S$				2	A
Maximum Body-Diode Pulsed Current (Note 1)	$I_{SM}$				4	A
Drain-Source Diode Forward Voltage (Note 1)	$V_{SD}$	$I_S=3\text{A}$ , $V_{GS}=0\text{V}$			1.4	V
Body Diode Reverse Recovery Time	$t_{rr}$	$I_S=3\text{A}$ , $V_{GS}=0\text{V}$ ,		260		ns
Body Diode Reverse Recovery Charge	$Q_{rr}$	$di/dt=100\text{A}/\mu\text{s}$		1		$\mu\text{C}$

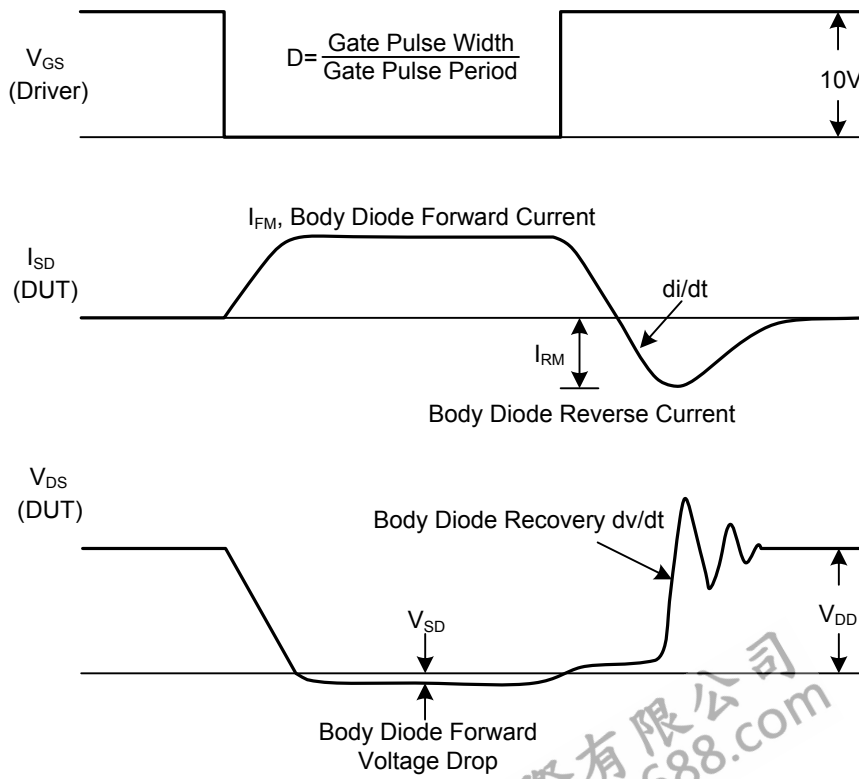
Notes: 1. Pulse Test: Pulse width  $\leq 300\mu\text{s}$ , Duty cycle  $\leq 2\%$ .

2. Essentially independent of operating temperature.

## TEST CIRCUITS AND WAVEFORMS

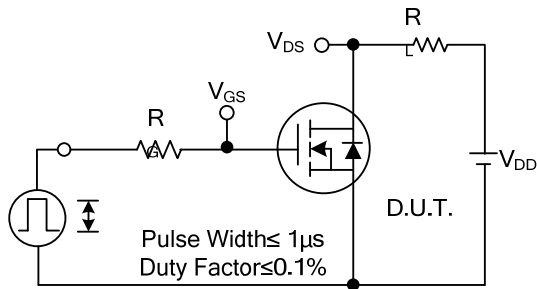


**Peak Diode Recovery dv/dt Test Circuit**

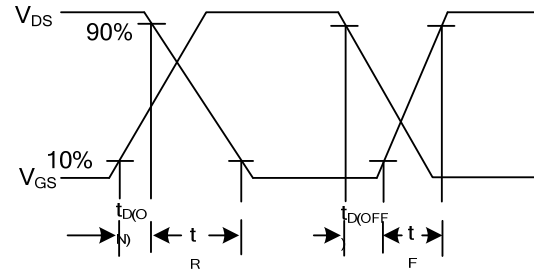


**Peak Diode Recovery dv/dt Waveforms**

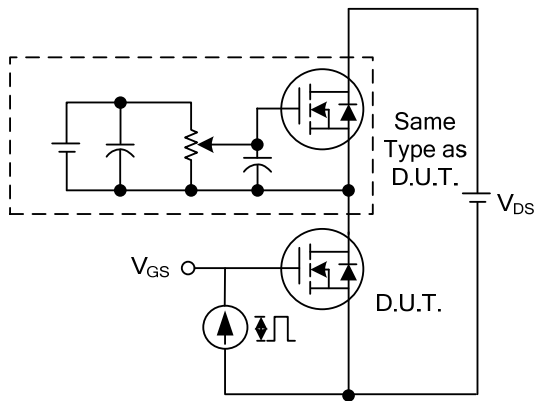
## TEST CIRCUITS AND WAVEFORMS



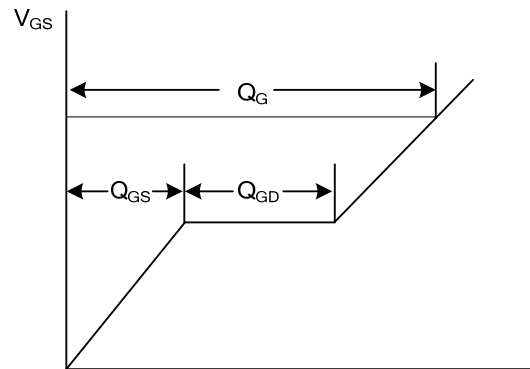
Switching Test Circuit



Switching Waveforms

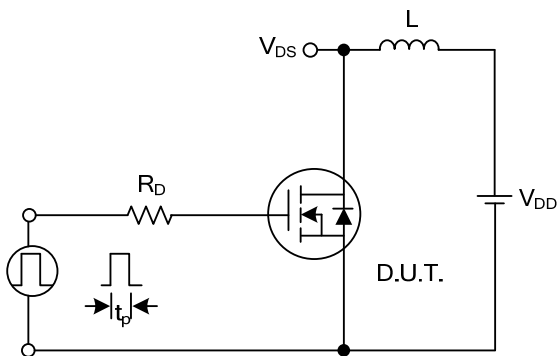


Gate Charge Test Circuit

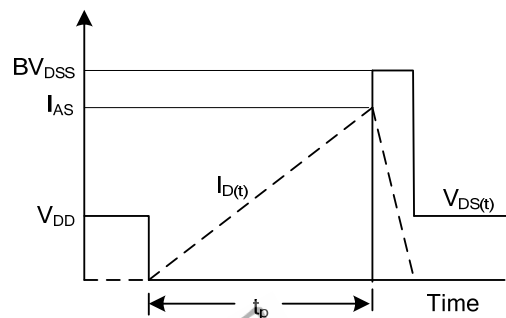


Charge

Gate Charge Waveform

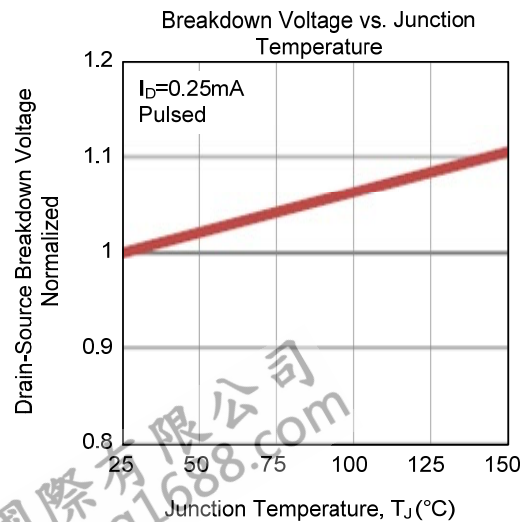
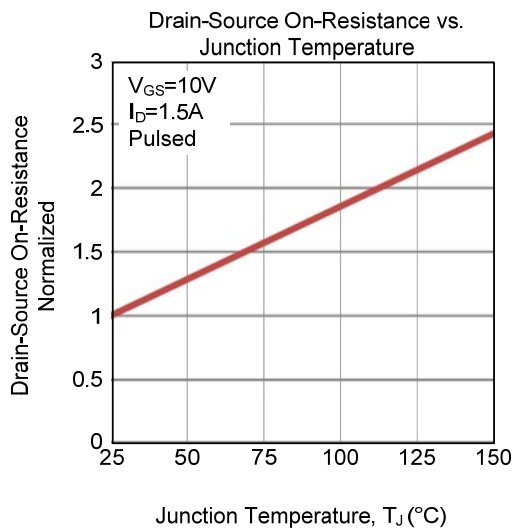
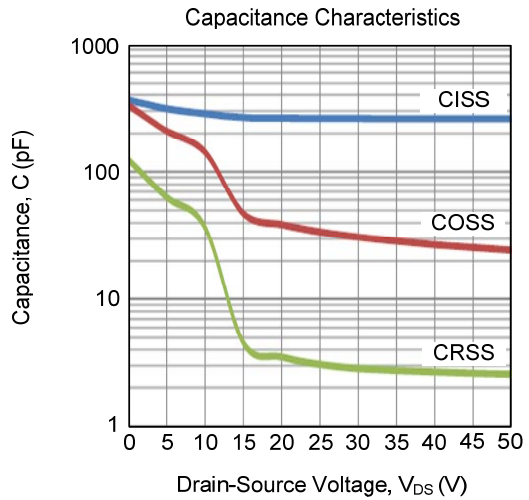
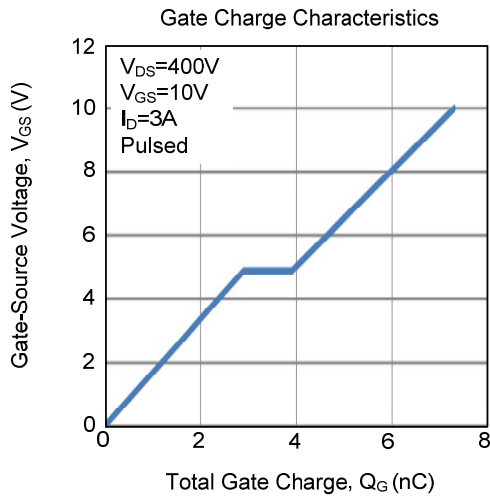
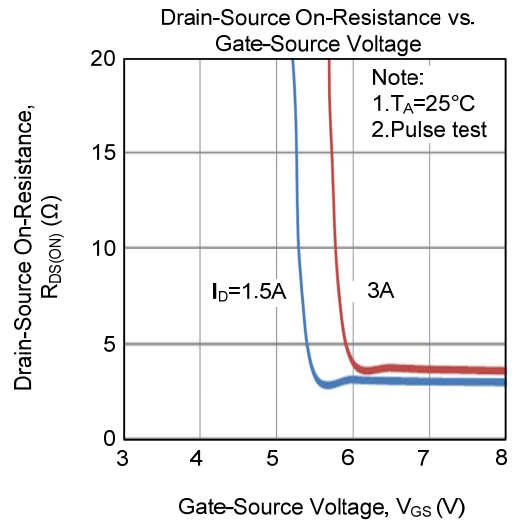
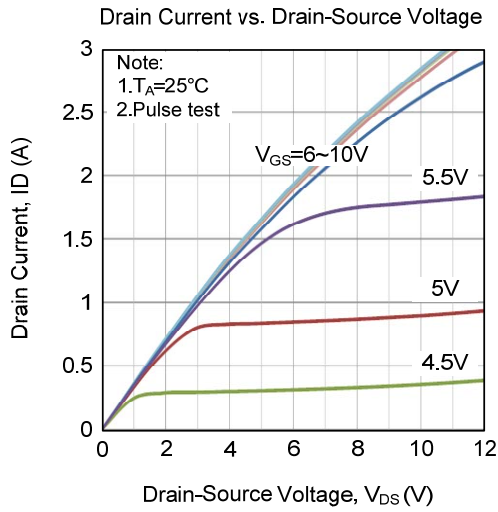


Unclamped Inductive Switching Test Circuit

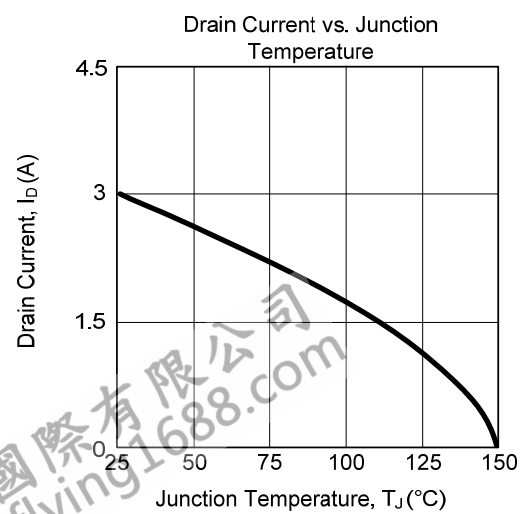
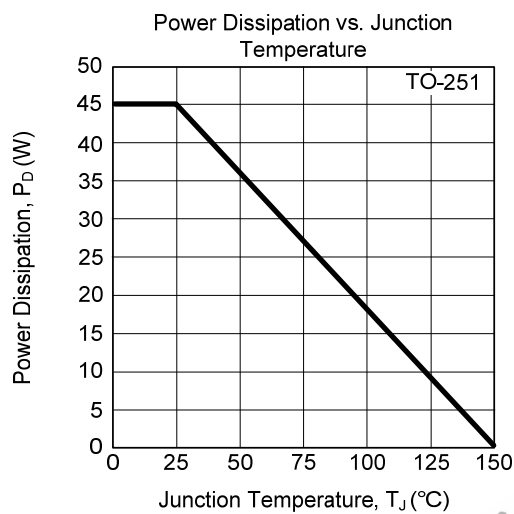
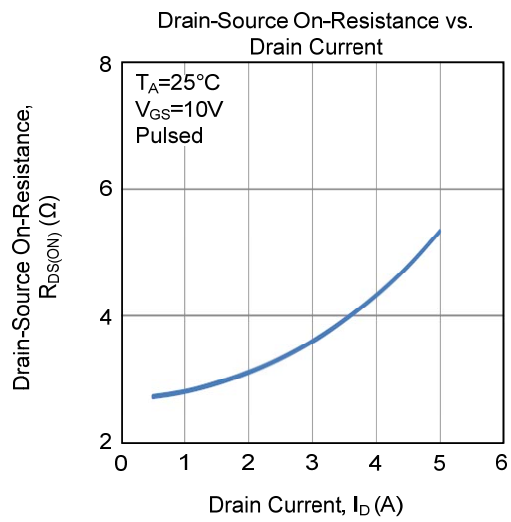
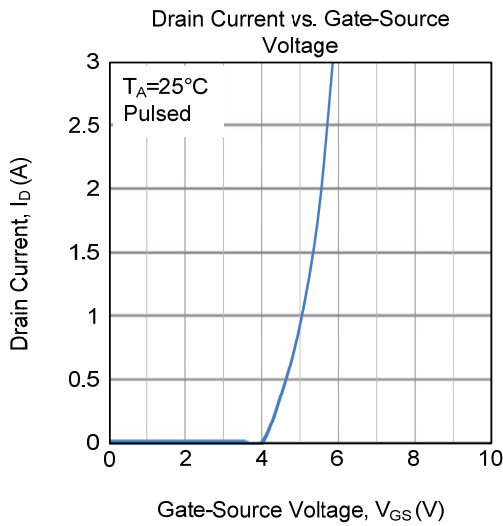
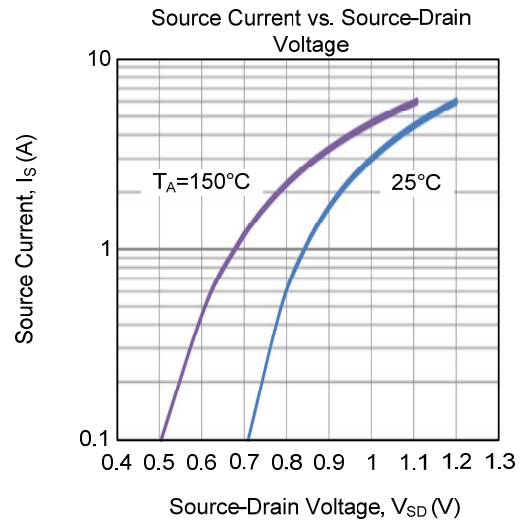
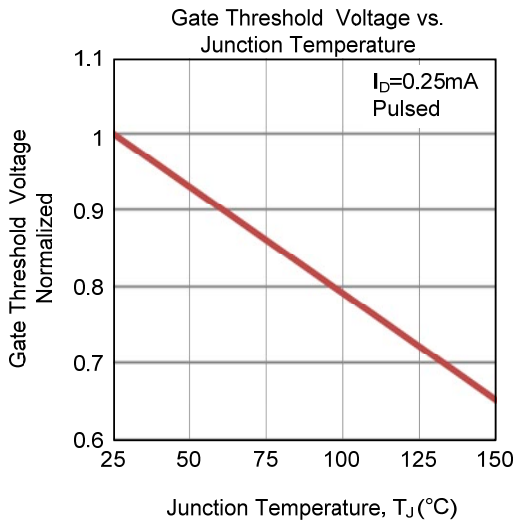


Unclamped Inductive Switching Waveforms

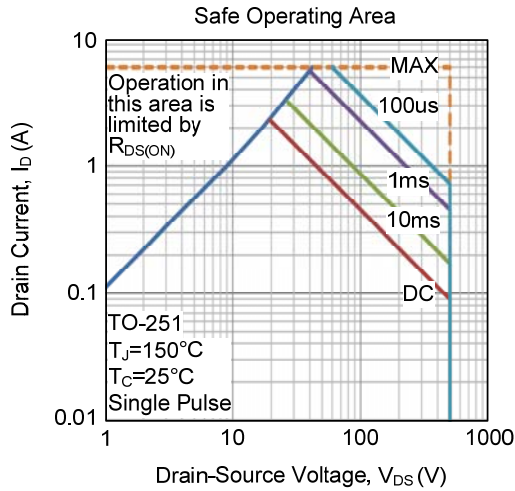
## TYPICAL CHARACTERISTICS



## TYPICAL CHARACTERISTICS (Cont.)



### ■ TYPICAL CHARACTERISTICS (Cont.)



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