



4N65-TA5

Preliminary

Power MOSFET

4.0A, 650V N-CHANNEL POWER MOSFET

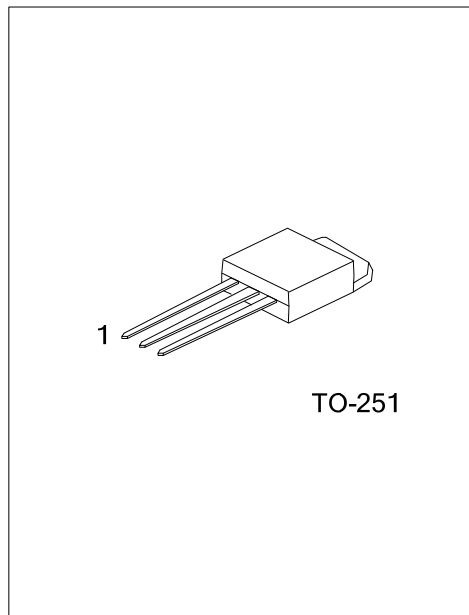
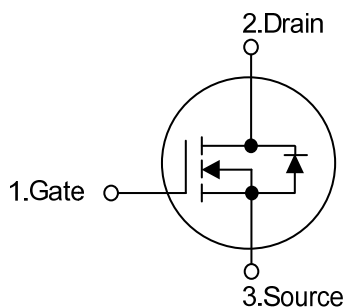
DESCRIPTION

The UTC **4N65-TA5** is a high voltage and high current power MOSFET, designed to have better characteristics, such as fast switching time, low gate charge, low on-state resistance and have a high rugged avalanche characteristics. This power MOSFET is usually used at high speed switching applications in power supplies, PWM motor controls, high efficient DC to DC converters and bridge circuits.

FEATURES

- * $R_{DS(ON)} < 2.8\Omega @ V_{GS} = 10V, I_D = 2.0A$
- * Fast switching capability
- * Avalanche energy specified
- * Improved dv/dt capability, high ruggedness

SYMBOL



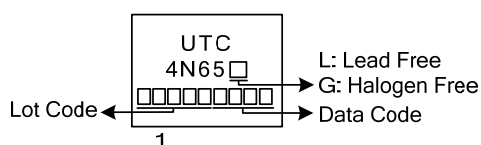
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
4N65L-TM3-T	4N65G-TM3-T	TO-251	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>4N65L-TM3-T</p> <p>(1)Packing Type</p> <p>(2)Package Type</p> <p>(3)Green Package</p>	<p>(1) T: Tube</p> <p>(2) TM3: TO-251</p> <p>(3) L: Lead Free, G: Halogen Free and Lead Free</p>
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MARKING



■ ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Drain-Source Voltage	V_{DSS}	650	V
Gate-Source Voltage	V_{GSS}	± 30	V
Avalanche Current (Note 2)	I_{AR}	4.0	A
Continuous Drain Current	I_D	4.0	A
Pulsed Drain Current (Note 2)	I_{DM}	12	A
Avalanche Energy	Single Pulsed (Note 3) E_{AS}	67	mJ
Peak Diode Recovery dv/dt (Note 4)	dv/dt	1.56	V/ns
Power Dissipation ($T_C=25^\circ\text{C}$)	P_D	50	W
Junction Temperature	T_J	+150	$^\circ\text{C}$
Operating Temperature	T_{OPR}	-55 ~ +150	$^\circ\text{C}$
Storage Temperature	T_{STG}	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating : Pulse width limited by T_J .

3. $L=15\text{mH}$, $I_{AS}=3.0\text{A}$, $V_{DD}=50\text{V}$, $R_G=25\ \Omega$, Starting $T_J = 25^\circ\text{C}$

4. $I_{SD}\leq 4.0\text{A}$, $di/dt \leq 100\text{A}/\mu\text{s}$, $V_{DD}\leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	110	$^\circ\text{C}/\text{W}$
Junction to Case	θ_{JC}	2.5	$^\circ\text{C}/\text{W}$

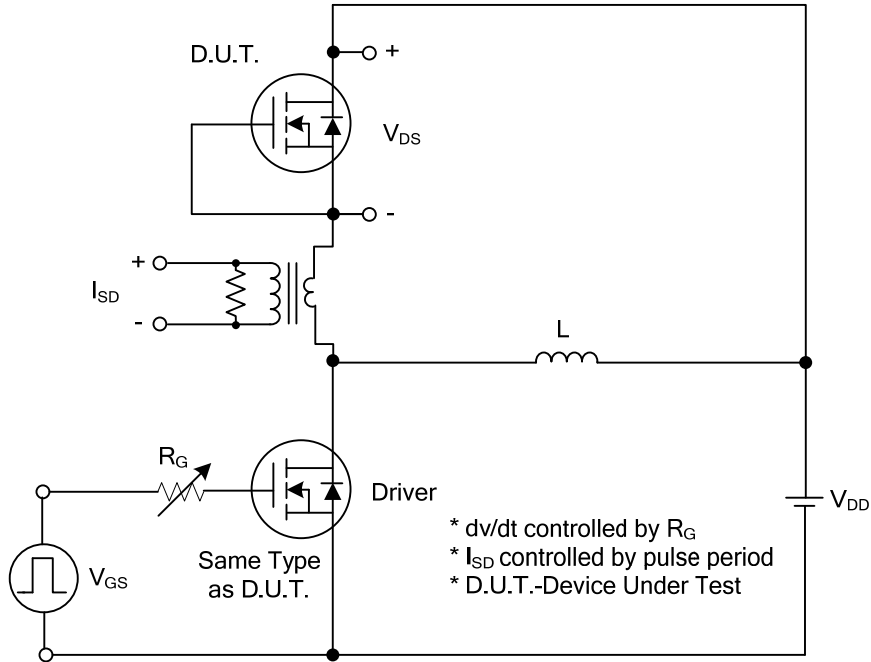
■ ELECTRICAL CHARACTERISTICS ($T_C=25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	650			V
Drain-Source Leakage Current	I_{DSS}	$V_{DS} = 650\text{ V}, V_{GS} = 0\text{ V}$			10	μA
Gate-Source Leakage Current	Forward	I_{GSS}			100	nA
	Reverse					
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	2.0		4.0	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS} = 10\text{ V}, I_D = 2.0\text{A}$			2.8	Ω
DYNAMIC CHARACTERISTICS						
Input Capacitance	C_{ISS}	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1\text{MHz}$		520		pF
Output Capacitance	C_{OSS}			52		pF
Reverse Transfer Capacitance	C_{RSS}			6		pF
SWITCHING CHARACTERISTICS						
Total Gate Charge	Q_G	$V_{DS}=50\text{V}, V_{GS}=10\text{V}, I_D=1.3\text{A},$ $I_G=100\mu\text{A}$ (Note 1, 2)		33		nC
Gate-Source Charge	Q_{GS}			4.5		nC
Gate-Drain Charge	Q_{GD}			4.8		nC
Turn-On Delay Time	$t_{D(ON)}$	$V_{DD}=30\text{V}, V_{GS}=10\text{V}, I_D=0.5\text{A},$ $R_G=25\Omega$ (Note 1, 2)		48		ns
Turn-On Rise Time	t_R			30		ns
Turn-Off Delay Time	$t_{D(OFF)}$			120		ns
Turn-Off Fall Time	t_F			30		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Continuous Drain-Source Diode Forward Current	I_S				4.0	A
Maximum Pulsed Drain-Source Diode Forward Current	I_{SM}				12	A
Drain-Source Diode Forward Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = 4.0\text{ A}$			1.4	V
Reverse Recovery Time	t_{rr}	$V_{GS}=0\text{V}, I_S=4.0\text{A}$ $di_F/dt=100\text{A}/\mu\text{s}$ (Note 1)		400		ns
Reverse Recovery Charge	Q_{RR}			2.13		μC

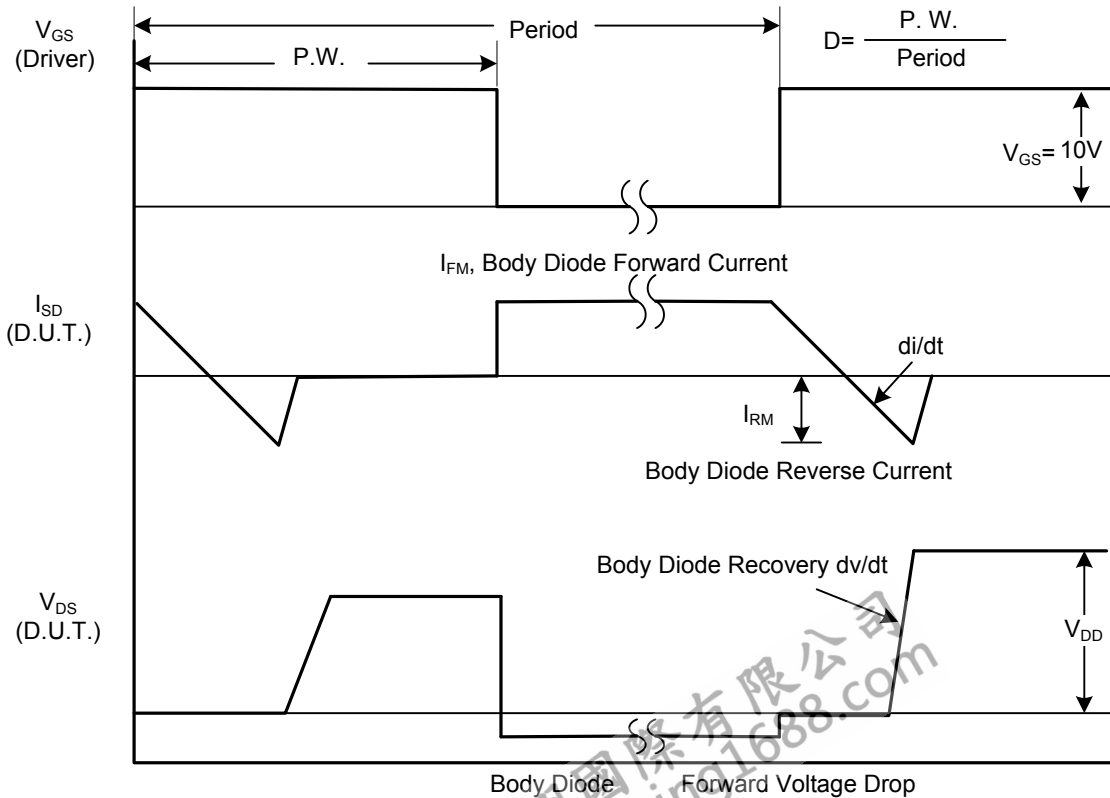
Notes: 1. Pulse Test: Pulse width $\leq 300\ \mu\text{s}$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

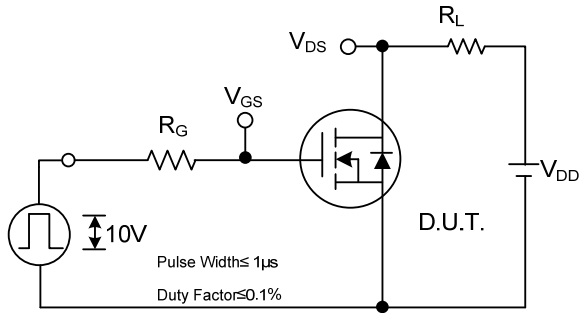


Peak Diode Recovery dv/dt Test Circuit

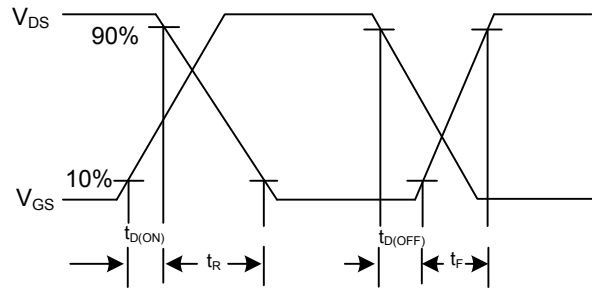


Peak Diode Recovery dv/dt Waveforms

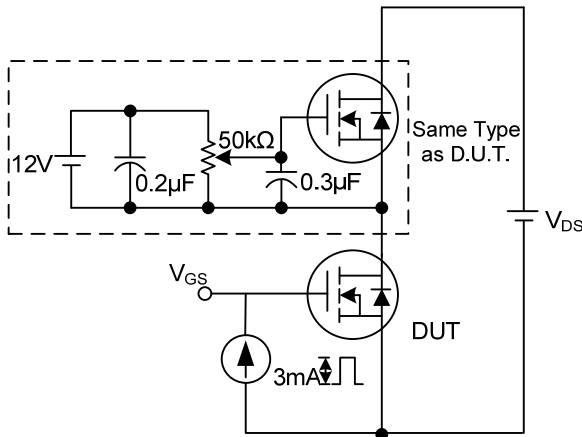
■ TEST CIRCUITS AND WAVEFORMS (Cont.)



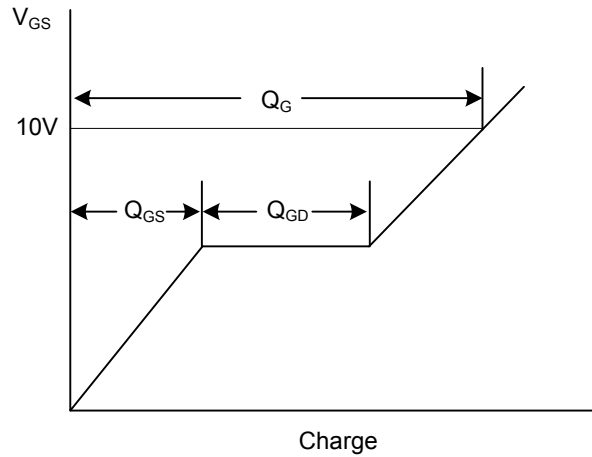
Switching Test Circuit



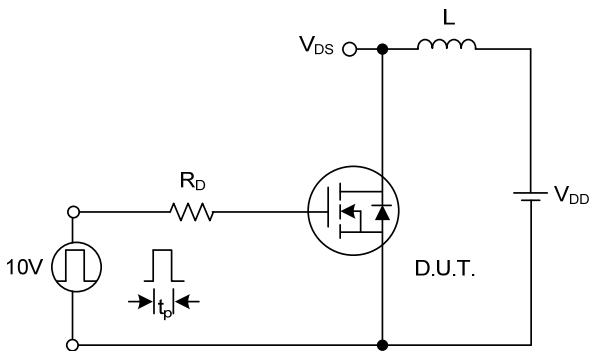
Switching Waveforms



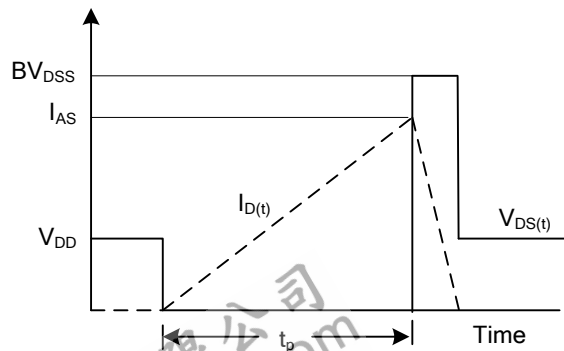
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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