



## 4N80-N

Power MOSFET

### 4.0A, 800V N-CHANNEL POWER MOSFET

#### DESCRIPTION

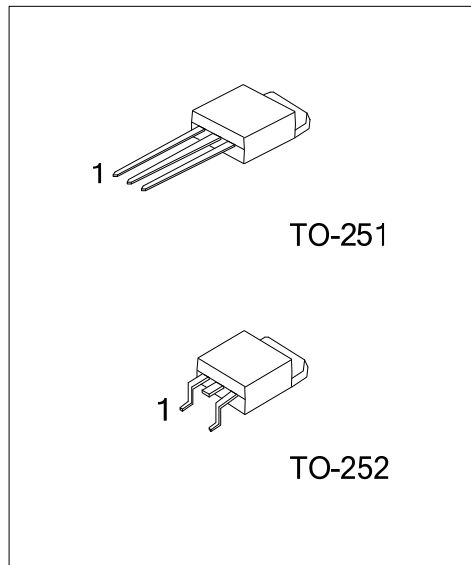
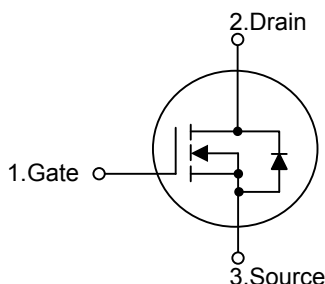
The UTC **4N80-N** is a N-channel mode power MOSFET using UTC's advanced technology to provide customers planar stripe and DMOS technology. This technology is specialized in allowing a minimum on-state resistance, and superior switching performance. It also can withstand high energy pulse in the avalanche and commutation mode.

The UTC **4N80-N** is universally applied in high efficiency switch mode power supply.

#### FEATURES

- \*  $R_{DS(on)} < 3.0\Omega @ V_{GS} = 10V$
- \* High switching speed
- \* Improved dv/dt capability
- \* 100% avalanche tested

#### SYMBOL



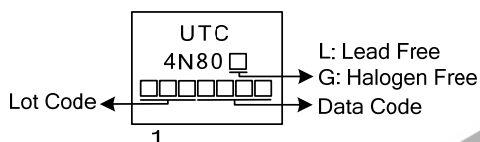
#### ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
4N80L-TM3-T	4N80G-TM3-T	TO-251	G	D	S	Tube
4N80L-TN3-R	4N80G-TN3-R	TO-252	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>4N80L-TM3-T</p>	<p>(1) T: Tube, R: Tape Reel</p> <p>(2) TM3: TO-251, TN3: TO-252</p> <p>(3) L: Lead Free, G: Halogen Free</p>
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#### MARKING



■ ABSOLUTE MAXIMUM RATINGS ( $T_c=25^\circ\text{C}$ , unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Drain-Source Voltage	$V_{DSS}$	800	V
Gate-Source Voltage	$V_{GSS}$	$\pm 30$	V
Drain Current	Continuous	$I_D$	4.0
	Pulsed (Note 2)	$I_{DM}$	16
Avalanche Energy	Single Pulsed (Note 3)	$E_{AS}$	250
Peak Diode Recovery dv/dt (Note 4)	dv/dt	4.0	V/ns
Power Dissipation	$P_D$	50	W
Junction Temperature	$T_J$	+150	$^\circ\text{C}$
Storage Temperature	$T_{STG}$	-55~+150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature

3.  $L=31.25\text{mH}$ ,  $I_{AS}=4\text{A}$ ,  $V_{DD}=50\text{V}$ ,  $R_G=25\Omega$ , Starting  $T_J=25^\circ\text{C}$

4.  $I_{SD} \leq 4\text{A}$ ,  $di/dt \leq 200\text{A}/\mu\text{s}$ ,  $V_{DD} \leq BV_{DSS}$ , Starting  $T_J=25^\circ\text{C}$

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	$\theta_{JA}$	110	$^\circ\text{C}/\text{W}$
Junction to Case	$\theta_{JC}$	2.5	$^\circ\text{C}/\text{W}$

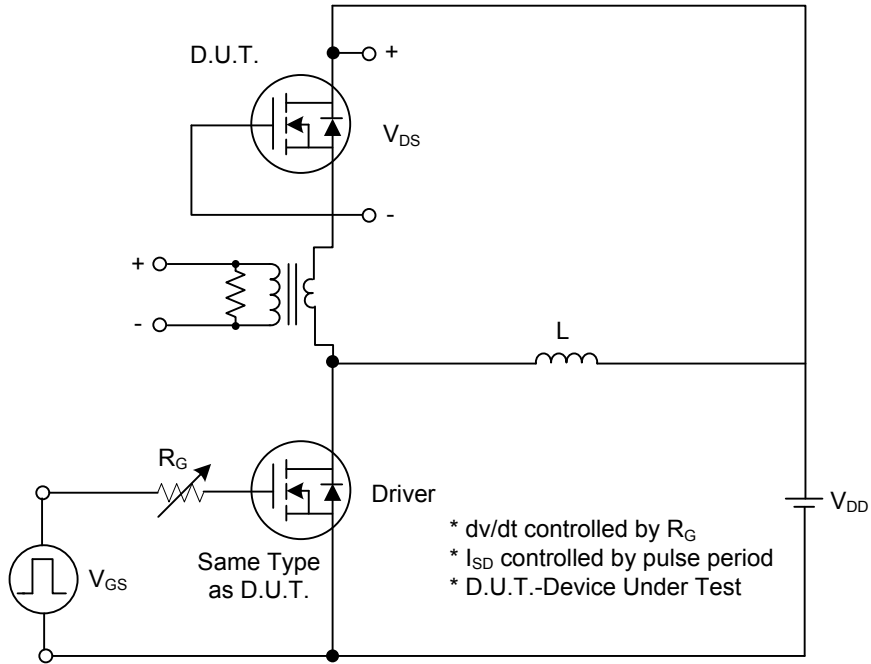
■ ELECTRICAL CHARACTERISTICS (T<sub>c</sub>=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>OFF CHARACTERISTICS</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	800			V
Breakdown Voltage Temperature Coefficient	ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	I <sub>D</sub> =250μA, Referenced to 25°C		950		mV/°C
Drain-Source Leakage Current	I <sub>DSS</sub>	V <sub>DS</sub> =800V, V <sub>GS</sub> =0V			10	μA
		V <sub>DS</sub> =640V, T <sub>C</sub> =125°C			100	μA
Gate-Source Leakage Current	Forward	I <sub>GSS</sub>			100	nA
	Reverse					
<b>ON CHARACTERISTICS</b>						
Gate Threshold Voltage	V <sub>GS(TH)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	3.0		5.0	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =2A		2.58	3.0	Ω
<b>DYNAMIC PARAMETERS</b>						
Input Capacitance	C <sub>ISS</sub>	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V, f=1.0MHz		570	880	pF
Output Capacitance	C <sub>OSS</sub>			65	100	pF
Reverse Transfer Capacitance	C <sub>RSS</sub>			9.5	12	pF
<b>SWITCHING PARAMETERS</b>						
Total Gate Charge	Q <sub>G</sub>	V <sub>DS</sub> =640V, V <sub>GS</sub> =10V, I <sub>D</sub> =4A (Note 1,2)		24	35	nC
Gate-Source Charge	Q <sub>GS</sub>			7.3		nC
Gate-Drain Charge	Q <sub>GD</sub>			7.25		nC
Turn-ON Delay Time	t <sub>D(ON)</sub>	V <sub>DD</sub> =400V, I <sub>D</sub> =4A, R <sub>G</sub> =25Ω (Note 1,2)		50	60	ns
Turn-ON Rise Time	t <sub>R</sub>			110	130	ns
Turn-OFF Delay Time	t <sub>D(OFF)</sub>			95	110	ns
Turn-OFF Fall Time	t <sub>F</sub>			70	90	ns
<b>SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS</b>						
Maximum Body-Diode Continuous Current	I <sub>S</sub>				4	A
Maximum Body-Diode Pulsed Current	I <sub>SM</sub>				16	A
Drain-Source Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =4A, V <sub>GS</sub> =0V			1.4	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =4A,		575		ns
Body Diode Reverse Recovery Charge	Q <sub>RR</sub>	di <sub>F</sub> /dt=100A/μs (Note 1)		3.65		μC

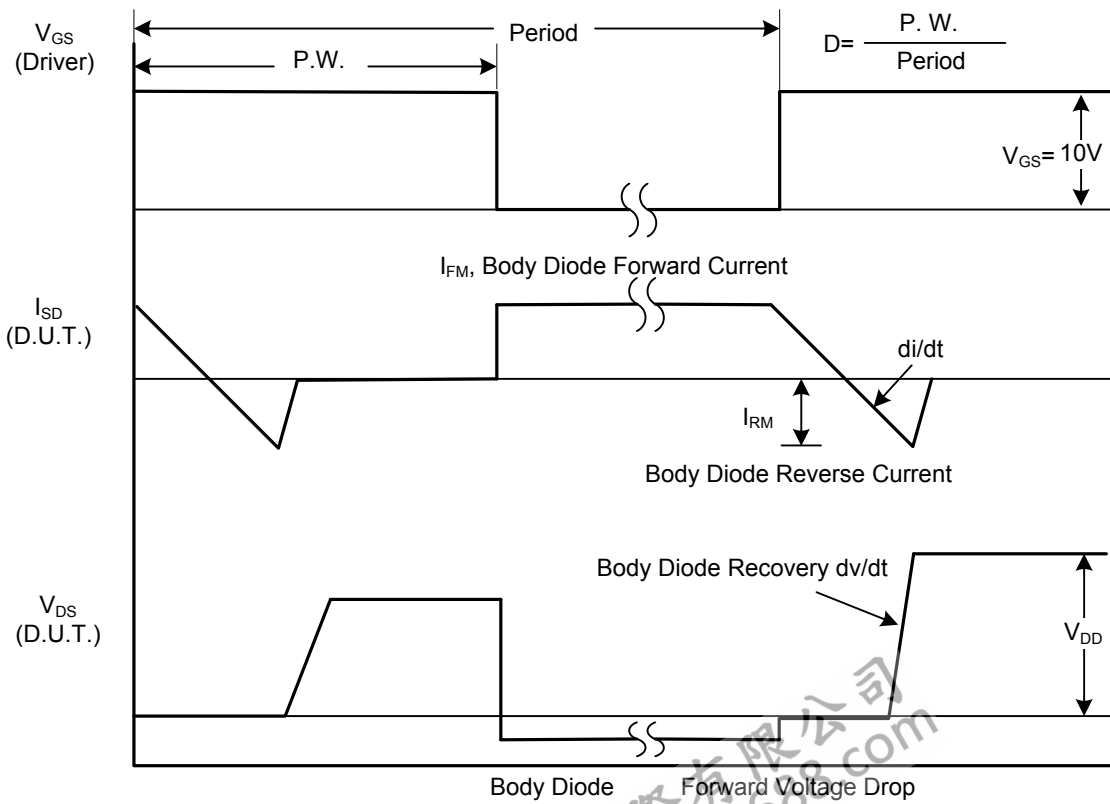
Notes: 1. Pulse Test: Pulse width ≤ 300μs, Duty cycle ≤ 2%

2. Essentially independent of operating temperature

■ TEST CIRCUITS AND WAVEFORMS

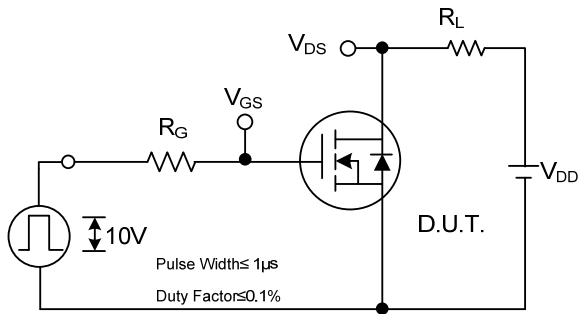


Peak Diode Recovery dv/dt Test Circuit

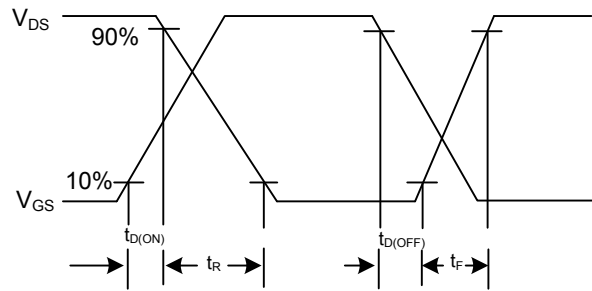


Peak Diode Recovery dv/dt Waveforms

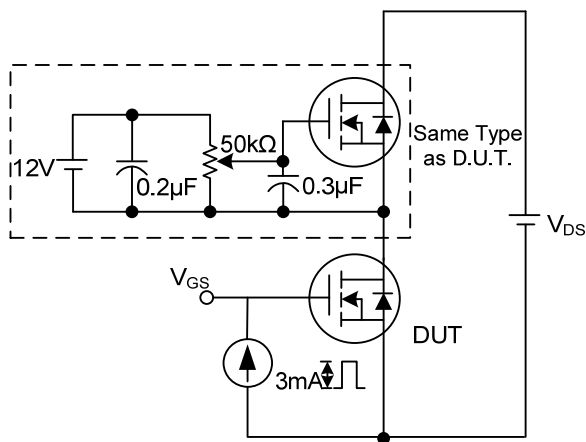
## TEST CIRCUITS AND WAVEFORMS(Cont.)



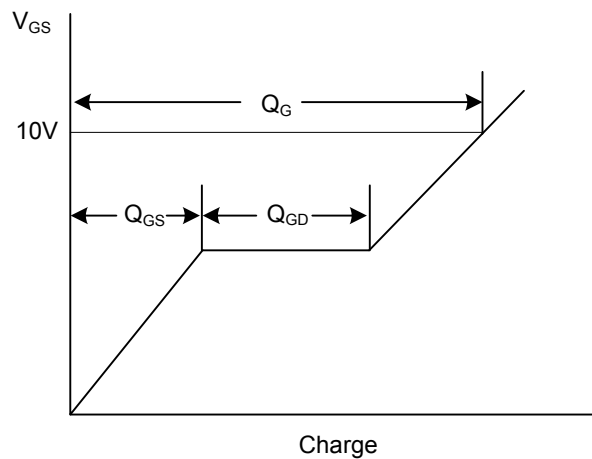
**Switching Test Circuit**



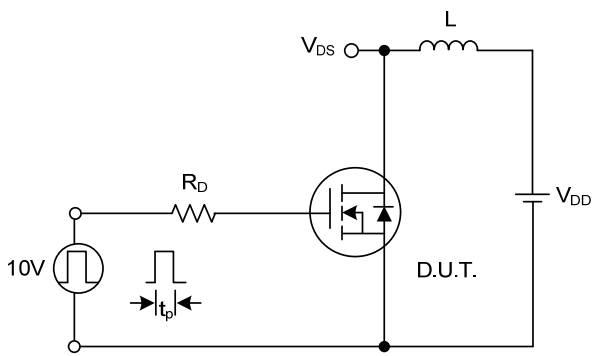
**Switching Waveforms**



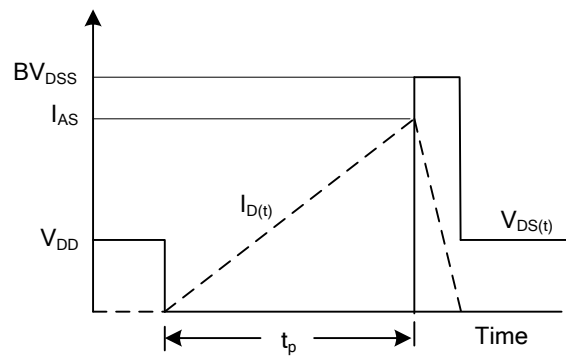
**Gate Charge Test Circuit**



**Gate Charge Waveform**

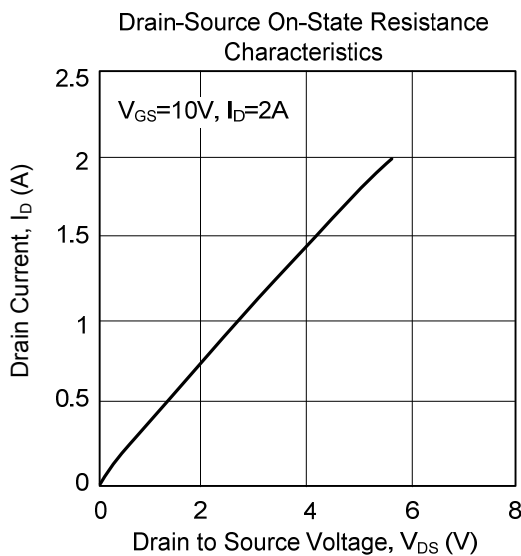
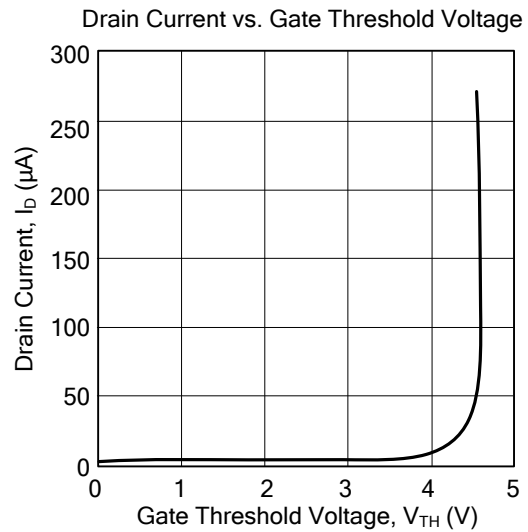
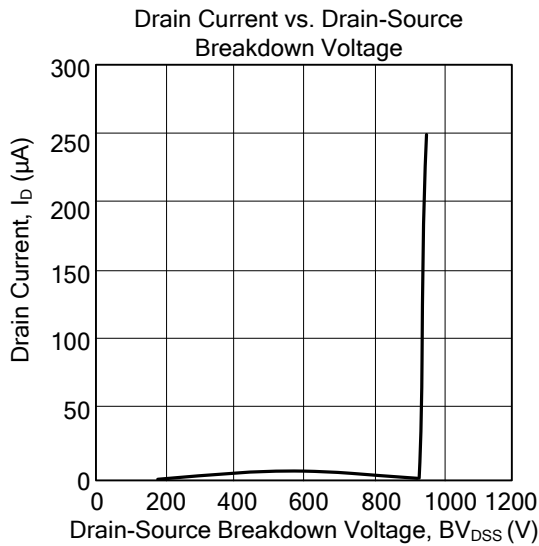


**Unclamped Inductive Switching Test Circuit**



**Unclamped Inductive Switching Waveforms**

### TYPICAL CHARACTERISTICS



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