

4P50

Power MOSFET

-4A, -500V P-CHANNEL POWER MOSFET

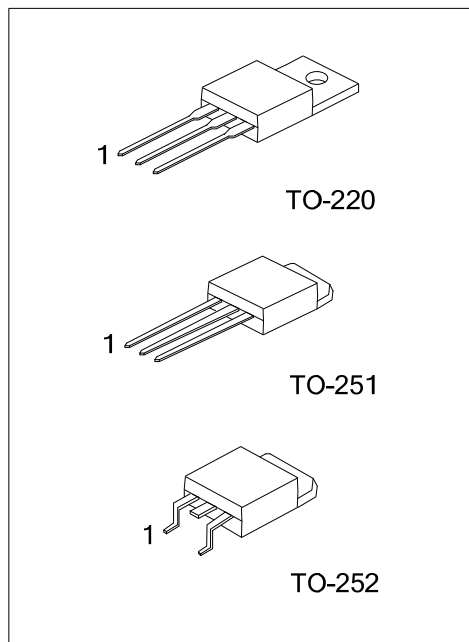
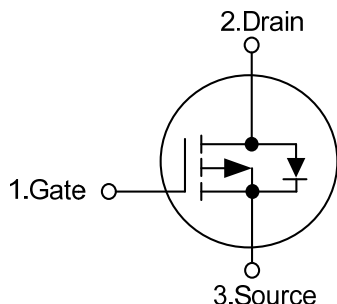
DESCRIPTION

The **4P50** uses advanced proprietary, planar stripe, DMOS technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with low gate voltages. This device is suitable to be used in low voltage applications such as audio amplifier, high efficiency switching DC/DC converters, and DC motor control.

FEATURES

- * $R_{DS(ON)} < 4.3\Omega$ @ $V_{GS}=-10V, I_D=-2.0A$
- * Low capacitance
- * Low gate charge
- * Fast switching capability
- * Avalanche energy specified

SYMBOL



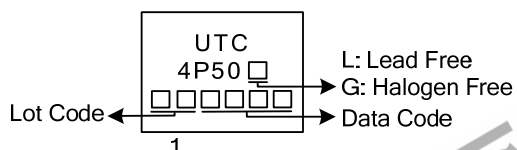
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
4P50L-TA3-T	4P50G-TA3-T	TO-220	G	D	S	Tube
4P50L-TM3-T	4P50G-TM3-T	TO-251	G	D	S	Tube
4P50L-TN3-R	4P50G-TN3-R	TO-252	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>4P50G-TA3-T</p> <p>(1)Packing Type</p> <p>(2)Package Type</p> <p>(3)Green Package</p>	<p>(1) T: Tube, R: Tape Reel</p> <p>(2) TA3: TO-220, TM3: TO-251, TN3: TO-252</p> <p>(3) G: Halogen Free and Lead Free, L: Lead Free</p>
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MARKING



■ ABSOLUTE MAXIMUM RATINGS ($T_C=25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	-500	V
Gate-Source Voltage		V_{GSS}	± 30	V
Continuous Drain Current	Continuous	I_D	-4	A
Pulsed Drain Current	Pulsed (Note 2)	I_{DM}	-16	A
Single Pulsed Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	192	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	10	V/ns
Power Dissipation	TO-220	P_D	73	W
	TO-251/TO-252		46	W
Junction Temperature		T_J	+150	$^\circ\text{C}$
Storage Temperature		T_{STG}	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $L=10\text{mH}$, $I_{AS}=-6.2\text{A}$, $V_{DD}=-150\text{V}$, $R_G=25\Omega$, Starting $T_J=25^\circ\text{C}$

4. $I_{SD} \leq -4.0\text{A}$, $di/dt \leq 200\mu\text{A/s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J=25^\circ\text{C}$

■ THERMAL DATA

PARAMETER		SYMBOL	RATING	UNIT
Junction to Ambient	TO-220	θ_{JA}	62.5	$^\circ\text{C/W}$
	TO-251/TO-252		110	$^\circ\text{C/W}$
Junction to Case	TO-220	θ_{JC}	1.71	$^\circ\text{C/W}$
	TO-251/TO-252		2.7	$^\circ\text{C/W}$

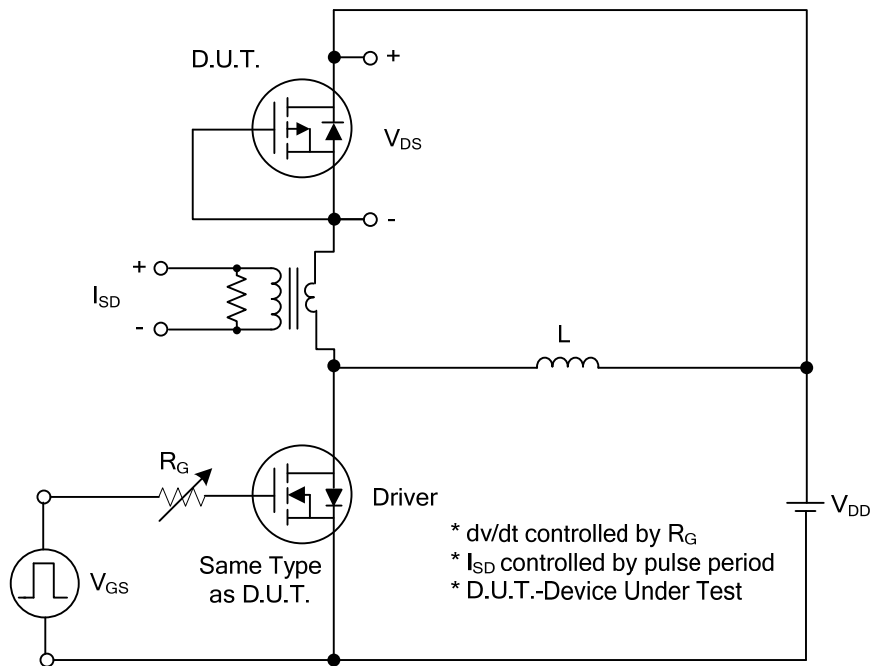
■ ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0\text{ V}, I_D=-250\mu\text{A}$	-500			V
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=-500\text{V}, V_{GS}=0\text{V}$			-1	μA
Gate-Source Leakage Current	Forward	$V_{DS}=0\text{V}, V_{GS}=+30\text{V}$			100	nA
	Reverse	$V_{DS}=0\text{V}, V_{GS}=-30\text{V}$			-100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}, I_D=-250\mu\text{A}$	-2.0		-4.0	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	$V_{GS}=-10\text{V}, I_D=-2.0\text{A}$			4.3	Ω
DYNAMIC PARAMETERS						
Input Capacitance	C_{ISS}	$V_{DS}=-25\text{V}, V_{GS}=0\text{V}, f=1.0\text{MHz}$		510		pF
Output Capacitance	C_{OSS}			85		pF
Reverse Transfer Capacitance	C_{RSS}			16		pF
SWITCHING PARAMETERS						
Total Gate Charge (Note 1)	Q_G	$V_{DS}=-50\text{V}, V_{GS}=-10\text{V}, I_D=-1.3\text{A}$ $I_G=-100\mu\text{A}$ (Note 1, 2)		52		nC
Gate Source Charge	Q_{GS}			5.2		nC
Gate Drain Charge	Q_{GD}			8.4		nC
Turn-ON Delay Time (Note 1)	$t_{D(ON)}$	$V_{DD}=-30\text{V}, V_{GS}=-10\text{V}, I_D=-0.5\text{A},$ $R_G=25\Omega$ (Note 1, 2)		85		ns
Turn-ON Rise Time	t_R			42		ns
Turn-OFF Delay Time	$t_{D(OFF)}$			176		ns
Turn-OFF Fall-Time	t_F			80		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Body-Diode Continuous Current	I_S				-4	A
Maximum Pulsed Drain-Source Diode Forward Current	I_{SM}				-16	A
Diode Forward Voltage (Note 1)	V_{SD}	$I_S=-2.0\text{A}, V_{GS}=0\text{V}$			-3.5	V
Body Diode Reverse Recovery Time(Note 1)	t_{rr}	$I_S=-4.0\text{A}, V_{GS}=0\text{V},$ $dI_F/dt=100\text{A}/\mu\text{s}$		230		ns
Body Diode Reverse Recovery Charge	Q_{rr}				2.2	

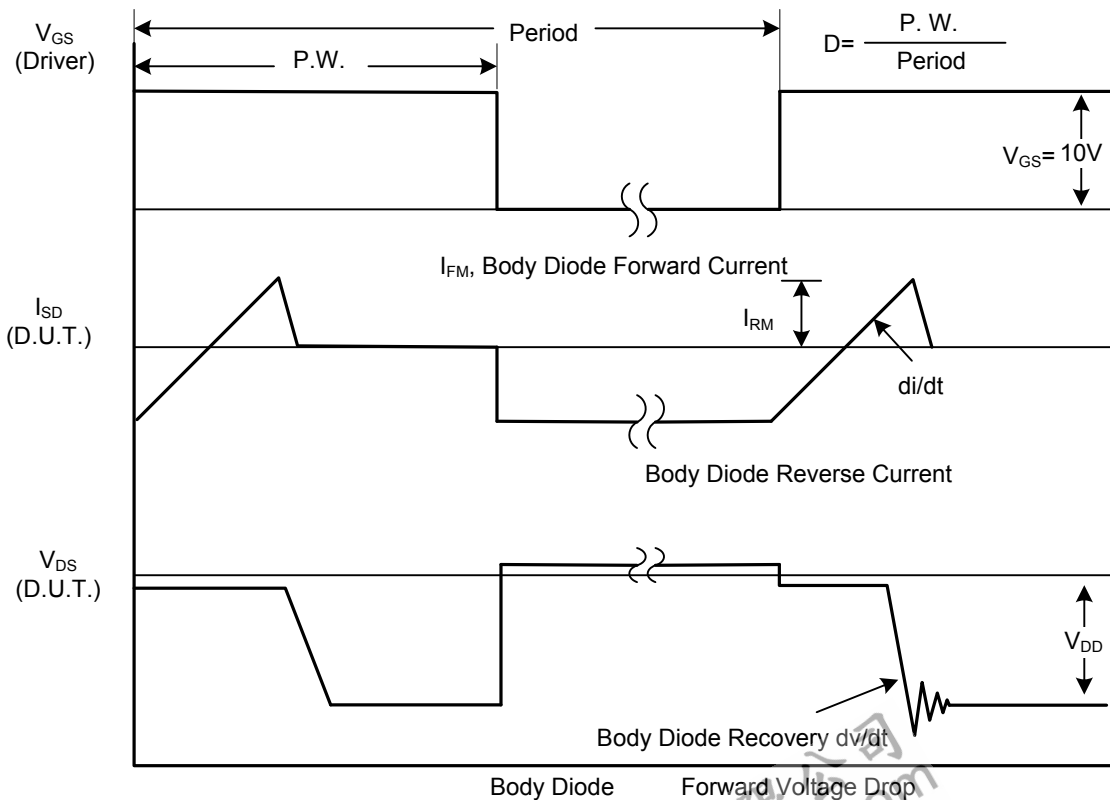
Notes: 1. Pulse Test : Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

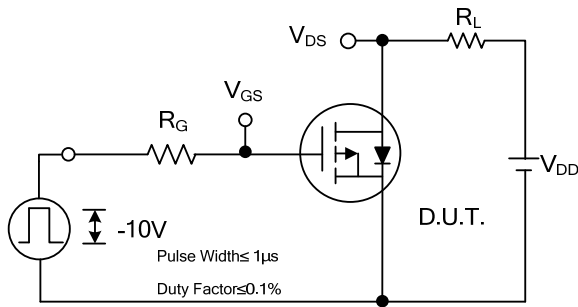


Peak Diode Recovery dv/dt Test Circuit

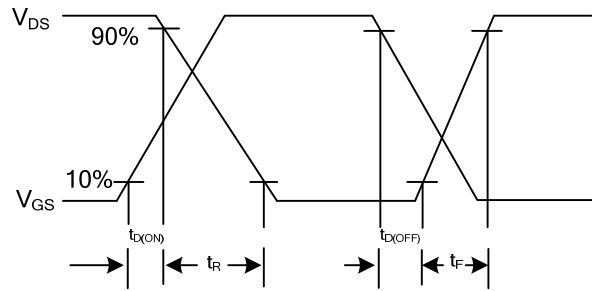


Peak Diode Recovery dv/dt Waveforms

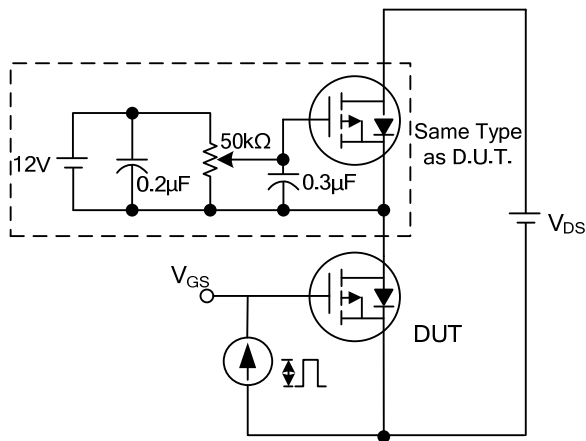
TEST CIRCUITS AND WAVEFORMS



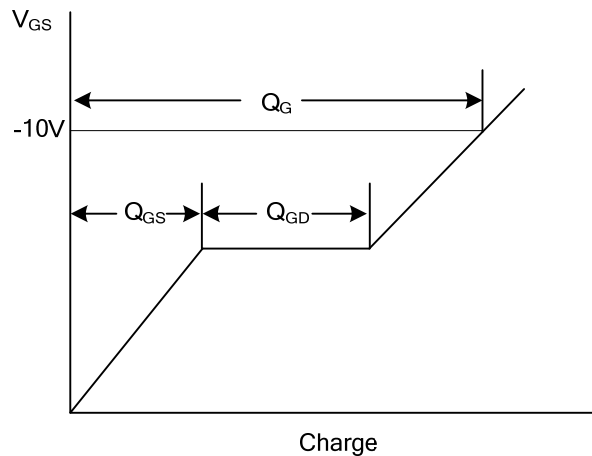
Switching Test Circuit



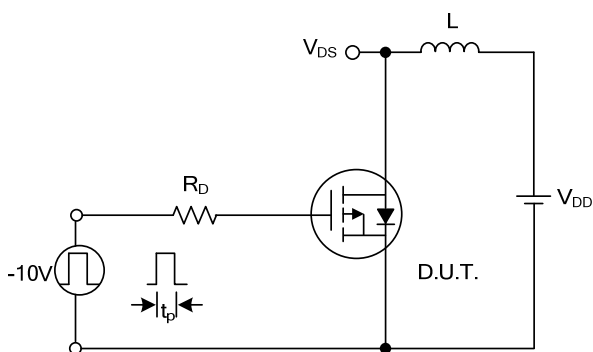
Switching Waveforms



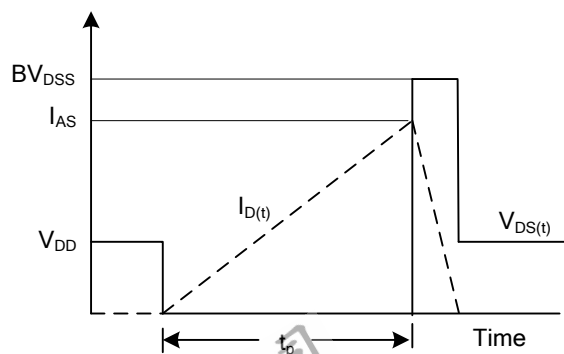
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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