



## 50NM70

Preliminary

Power MOSFET

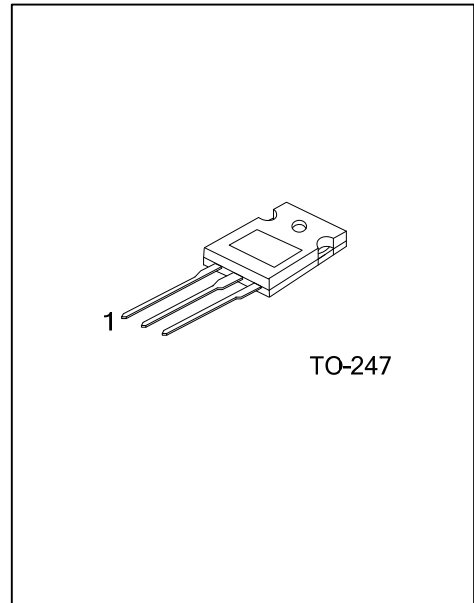
### 50A, 700V N-CHANNEL SUPER-JUNCTION MOSFET

#### DESCRIPTION

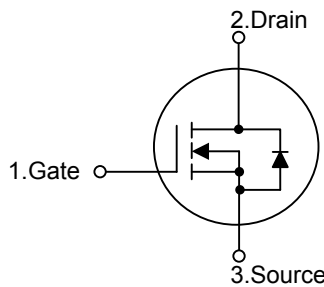
The **UTC 50NM70** is a Super Junction MOSFET Structure and is designed to have better characteristics, such as fast switching time, low gate charge, low on-state resistance and a high rugged avalanche characteristics. This power MOSFET is usually used at DC-DC, AC-DC converters for power applications.

#### FEATURES

- \*  $R_{DS(ON)} < 100m\Omega @ V_{GS}=10V, I_D=25A$
- \* High Switching Speed
- \* 100% Avalanche Tested



#### SYMBOL



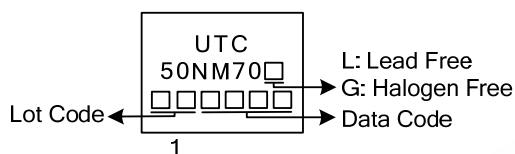
#### ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
50NM70L-T47-T	50NM70G-T47-T	TO-247	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>50NM70L-T47-T</p> <p>(1)Packing Type</p> <p>(2)Package Type</p> <p>(3)Green Package</p>	<p>(1) T: Tube</p> <p>(2) T47: TO-247</p> <p>(3) L: Lead Free, G: Halogen Free and Lead Free</p>
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#### MARKING



■ ABSOLUTE MAXIMUM RATINGS ( $T_C=25^{\circ}\text{C}$ , unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		$V_{DSS}$	700	V
Gate-Source Voltage		$V_{GSS}$	$\pm 30$	V
Drain Current	Continuous	$I_D$	50	A
	Pulsed (Note 2)	$I_{DM}$	200	A
Avalanche Energy	Single Pulsed (Note 3)	$E_{AS}$	1330	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	18	V/ns
Power Dissipation		$P_D$	310	W
Junction Temperature		$T_J$	+150	$^{\circ}\text{C}$
Storage Temperature		$T_{STG}$	-55 ~ +150	$^{\circ}\text{C}$

- Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.  
 2. Repetitive Rating: Pulse width limited by maximum junction temperature.  
 3.  $L = 36\text{mH}$ ,  $I_{AS} = 8.6\text{A}$ ,  $V_{DD} = 50\text{V}$ ,  $R_G = 25\Omega$ , Starting  $T_J = 25^{\circ}\text{C}$

■ THERMAL DATA

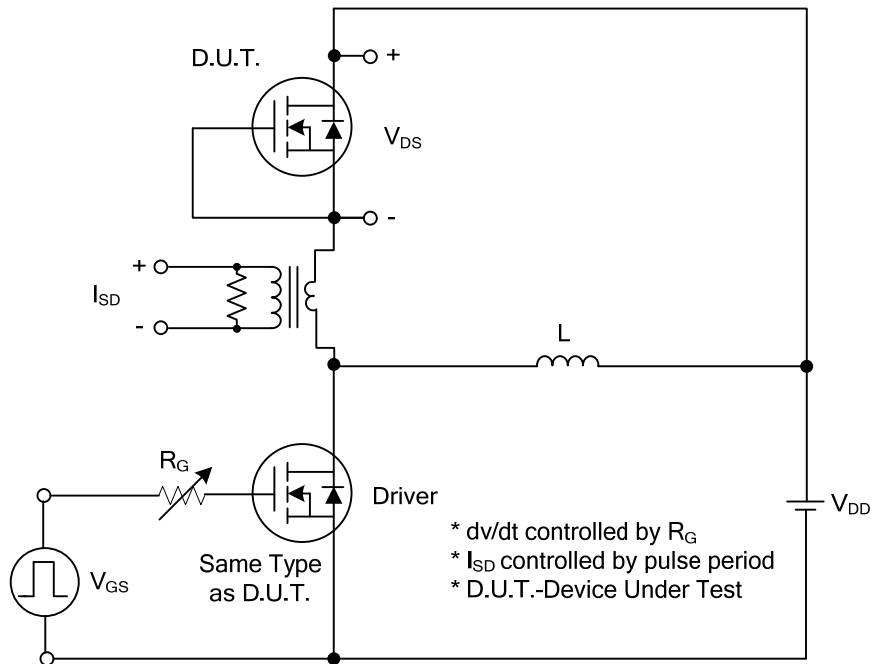
PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	$\theta_{JA}$	40	$^{\circ}\text{C/W}$
Junction to Case	$\theta_{JC}$	0.4	$^{\circ}\text{C/W}$

■ ELECTRICAL CHARACTERISTICS ( $T_C=25^{\circ}\text{C}$ , unless otherwise specified)

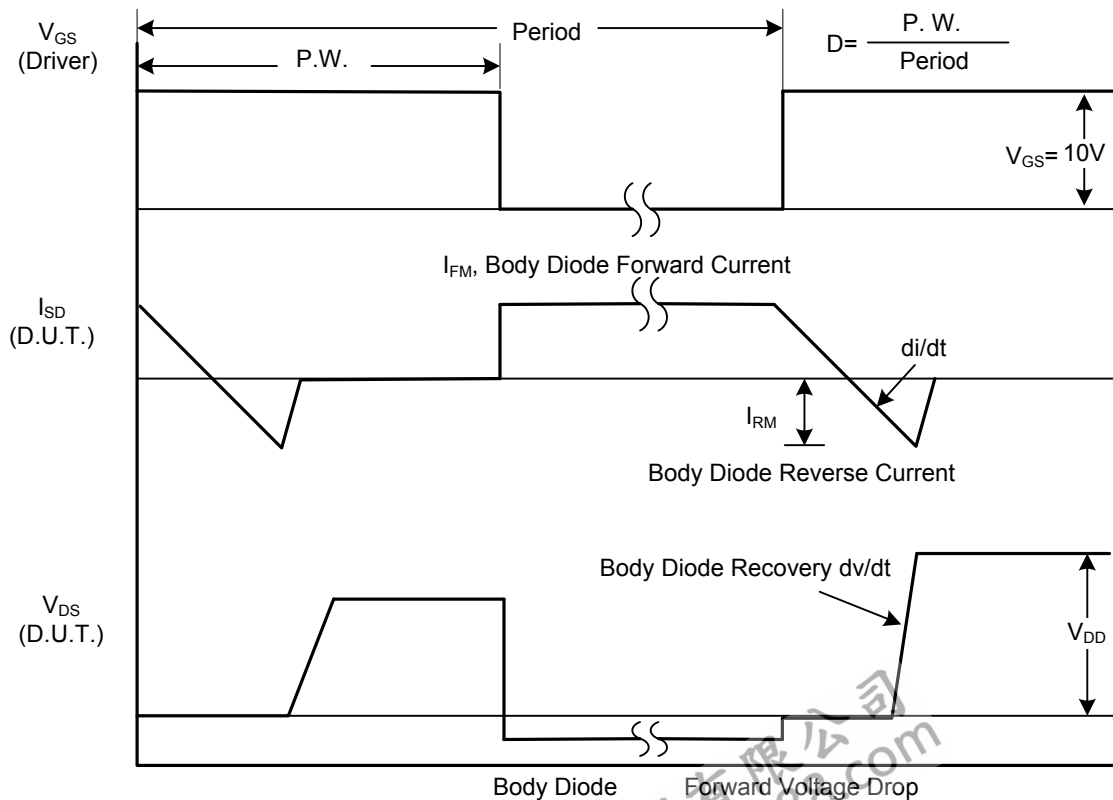
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>OFF CHARACTERISTICS</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$I_D=250\mu\text{A}$ , $V_{GS}=0\text{V}$	700			V
Drain-Source Leakage Current	$I_{DSS}$	$V_{DS}=700\text{V}$ , $V_{GS}=0\text{V}$			50	$\mu\text{A}$
Gate- Source Leakage Current	$I_{GSS}$	Forward			+100	nA
		Reverse	$V_{GS}=+30\text{V}$ , $V_{DS}=0\text{V}$			-100
<b>ON CHARACTERISTICS</b>						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}$ , $I_D=250\mu\text{A}$	2.5		4.5	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$ , $I_D=25\text{A}$			100	m $\Omega$
<b>DYNAMIC PARAMETERS</b>						
Input Capacitance	$C_{ISS}$	$V_{GS}=0\text{V}$ , $V_{DS}=25\text{V}$ , $f=1.0\text{MHz}$		3200		pF
Output Capacitance	$C_{OSS}$			1660		pF
Reverse Transfer Capacitance	$C_{RSS}$			20		pF
<b>SWITCHING PARAMETERS</b>						
Total Gate Charge	$Q_G$	$V_{DS}=50\text{V}$ , $V_{GS}=10\text{V}$ , $I_D=1.3\text{A}$ , (Note 1, 2)		300		nC
Gate to Source Charge	$Q_{GS}$			30		nC
Gate to Drain Charge	$Q_{GD}$			78		nC
Turn-ON Delay Time	$t_{D(ON)}$	$V_{DD}=30\text{V}$ , $V_{GS}=10\text{V}$ , $I_D=0.5\text{A}$ , $R_G=25\Omega$ (Note 1, 2)		180		ns
Rise Time	$t_R$			520		ns
Turn-OFF Delay Time	$t_{D(OFF)}$			1080		ns
Fall-Time	$t_F$			680		ns
<b>SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS</b>						
Maximum Body-Diode Continuous Current	$I_S$				50	A
Maximum Body-Diode Pulsed Current	$I_{SM}$				200	A
Drain-Source Diode Forward Voltage	$V_{SD}$	$I_S=50\text{A}$ , $V_{GS}=0\text{V}$			1.4	V
Body Diode Reverse Recovery Time	$t_{rr}$	$I_S=25\text{A}$ , $V_{GS}=0\text{V}$ , $V_R=200\text{V}$		630		ns
Body Diode Reverse Recovery Charge	$Q_{rr}$	$dI_F/dt=100\text{A}/\mu\text{s}$ (Note 1)		15		$\mu\text{C}$

- Notes: 1. Pulse Test : Pulse width  $\leq 300\mu\text{s}$ , Duty cycle  $\leq 2\%$ .  
 2. Essentially independent of operating ambient temperature.

■ TEST CIRCUITS AND WAVEFORMS



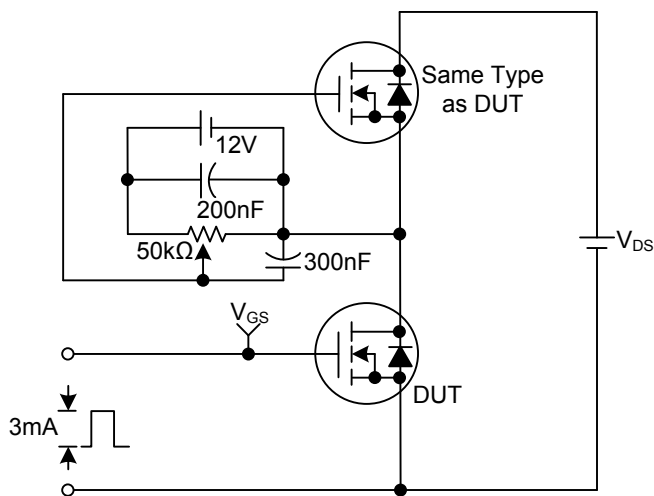
Peak Diode Recovery  $dv/dt$  Test Circuit



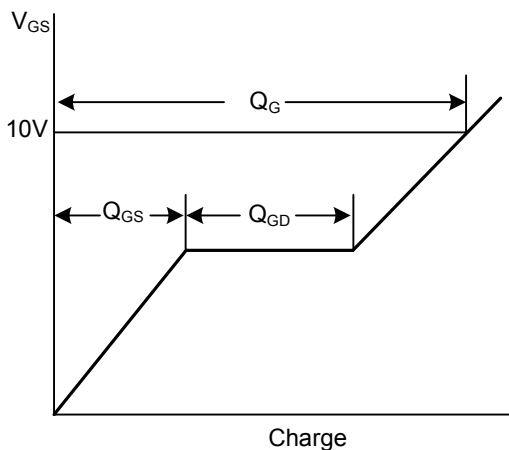
Peak Diode Recovery  $dv/dt$  Waveforms

■ TEST CIRCUITS AND WAVEFORMS (Cont.)

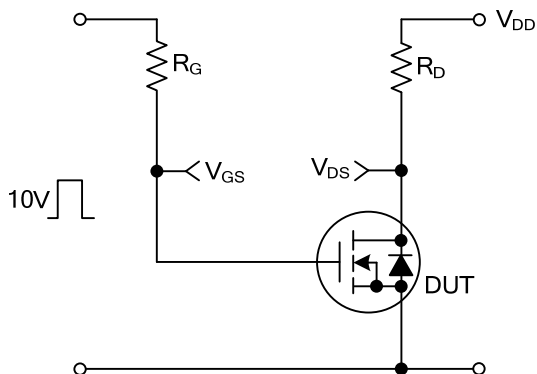
Gate Charge Test Circuit



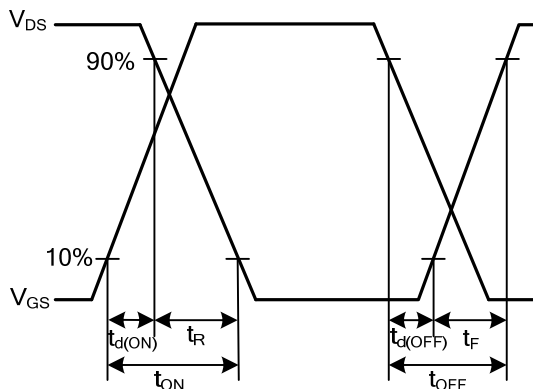
Gate Charge Waveforms



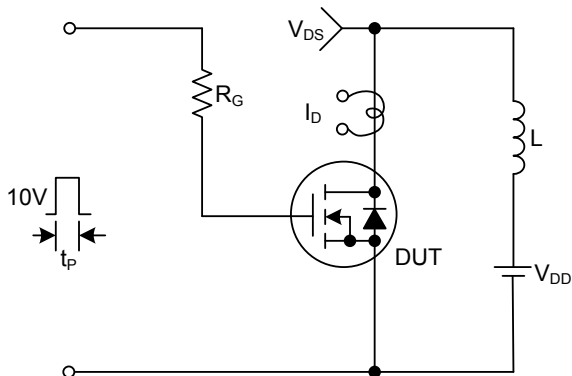
Resistive Switching Test Circuit



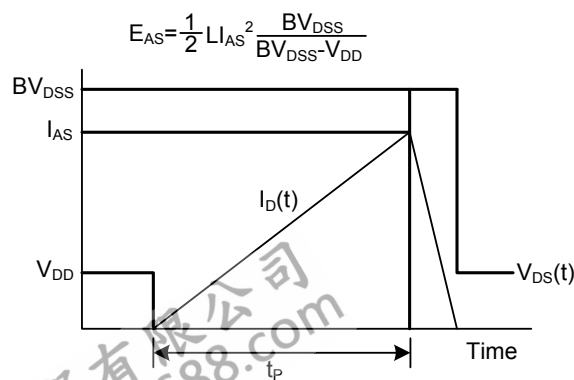
Resistive Switching Waveforms



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms



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