



5NL55

Power MOSFET

5A, 550V N-CHANNEL SUPER-JUNCTION MOSFET

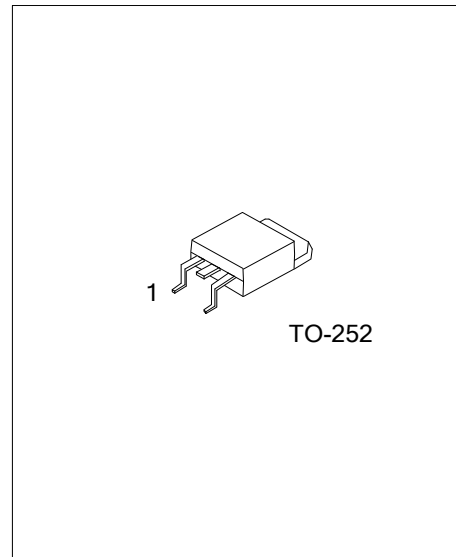
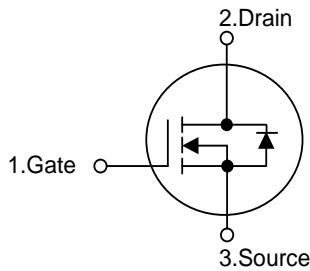
DESCRIPTION

The UTC 5NL55 is a Super Junction MOSFET Structure and is designed to have better characteristics, such as fast switching time, low gate charge, low on-state resistance and a high rugged avalanche characteristics. This power MOSFET is usually used at AC-DC converters for power applications.

FEATURES

- * $R_{DS(ON)} \leq 1.4 \Omega$ @ $V_{GS}=10V, I_D=2.5A$
- * Fast switching
- * 100% avalanche tested
- * Improved dv/dt capability

SYMBOL



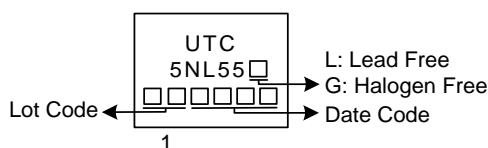
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
5NL55L-TN3-R	5NL55G-TN3-R	TO-252	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>5NL55G-TN3-R</p> <ul style="list-style-type: none"> (1) Packing Type (2) Package Type (3) Green Package 	<ul style="list-style-type: none"> (1) R: Tape Reel (2) TN3: TO-252 (3) G: Halogen Free and Lead Free, L: Lead Free
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MARKING



■ **ABSOLUTE MAXIMUM RATINGS** ($T_C = 25^\circ\text{C}$ unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	550	V
Gate-Source Voltage		V_{GSS}	± 30	V
Drain Current	Continuous	I_D	5	A
	Pulsed (Note 2)	I_{DM}	10	A
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	144	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	3.9	V/ns
Power Dissipation		P_D	50	W
Junction Temperature		T_J	+150	$^\circ\text{C}$
Storage Temperature		T_{STG}	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature
3. $L = 30\text{mH}$, $I_{AS} = 3.1\text{A}$, $V_{DD} = 100\text{V}$, $R_G = 25\ \Omega$ Starting $T_J = 25^\circ\text{C}$
4. $I_{SD} \leq 5.0\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$

■ **THERMAL DATA**

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient		θ_{JA}	110	$^\circ\text{C}/\text{W}$
Junction to Case		θ_{JC}	2.5 (Note)	$^\circ\text{C}/\text{W}$

Note: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

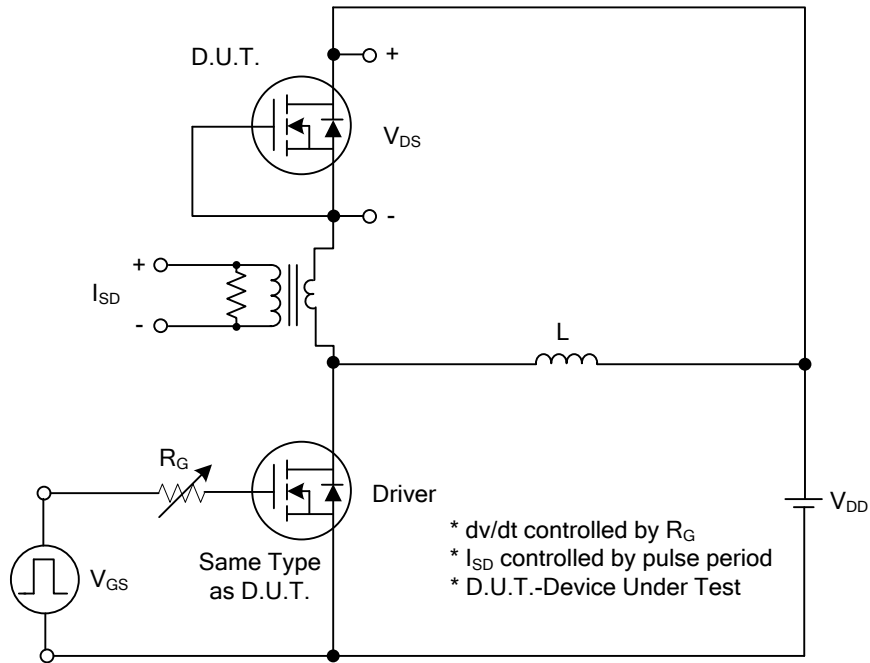
■ **ELECTRICAL CHARACTERISTICS** ($T_C=25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	550			V
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=550V, V_{GS}=0V$			10	μA
Gate-Source Leakage Current	Forward	$V_{GS}=30V, V_{DS}=0V$ $V_{GS}=-30V, V_{DS}=0V$			100	nA
	Reverse				-100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2.0		4.0	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=2.5A$			1.4	Ω
DYNAMIC CHARACTERISTICS						
Input Capacitance	C_{ISS}	$V_{DS}=25V, V_{GS}=0V, f=1.0\text{ MHz}$		358		pF
Output Capacitance	C_{OSS}			157		pF
Reverse Transfer Capacitance	C_{RSS}			17		pF
SWITCHING CHARACTERISTICS						
Total Gate Charge	Q_G	$V_{DS}=440V, V_{GS}=10V, I_D=5A$ $I_G=1\text{ mA (Note1, 2)}$		13.4		nC
Gate-Source Charge	Q_{GS}			3.4		nC
Gate-Drain Charge	Q_{GD}			3.4		nC
Turn-On Delay Time	$t_{D(ON)}$	$V_{DS}=100V, V_{GS}=10V, I_D=5A,$ $R_G=25\Omega$ (Note1, 2)		6		ns
Turn-On Rise Time	t_R			16		ns
Turn-Off Delay Time	$t_{D(OFF)}$			38		ns
Turn-Off Fall Time	t_F			23		ns
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
Maximum Continuous Drain-Source Diode Forward Current	I_S				5	A
Maximum Pulsed Drain-Source Diode Forward Current	I_{SM}				10	A
Drain-Source Diode Forward Voltage	V_{SD}	$V_{GS}=0V, I_S=5A$			1.4	V
Reverse Recovery Time	t_{rr}	$V_{GS}=0V, I_S=5A,$ $di_F/dt=100A/\mu s$ (Note1)		272		ns
Reverse Recovery Charge	Q_{rr}			4.9		μC

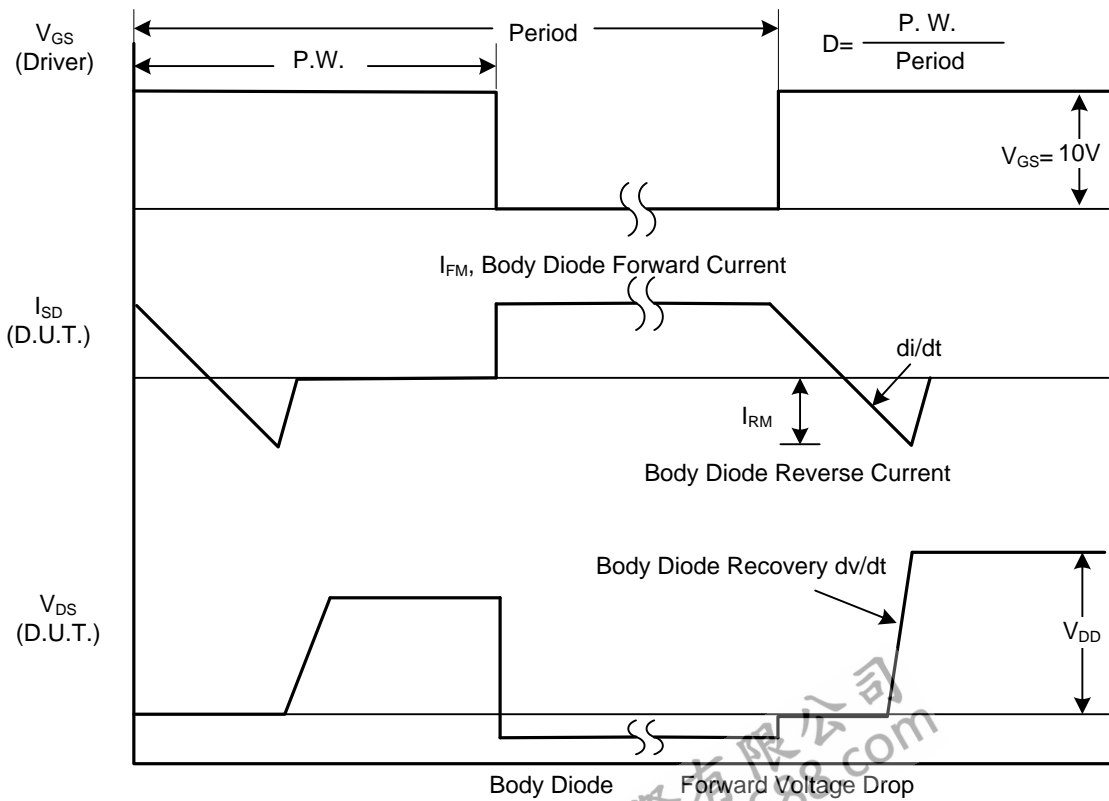
Notes: 1. Pulse Test : Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

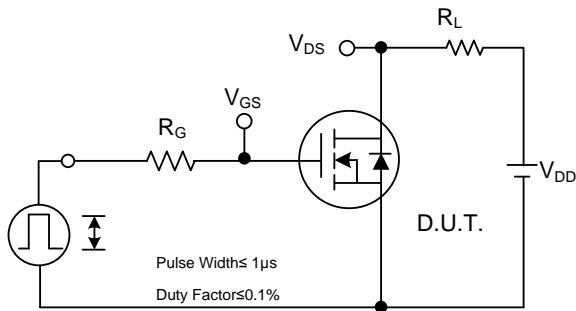


Peak Diode Recovery dv/dt Test Circuit

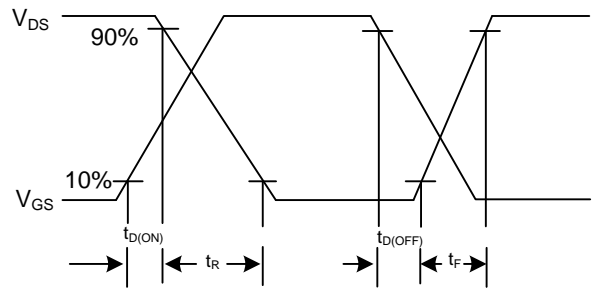


Peak Diode Recovery dv/dt Waveforms

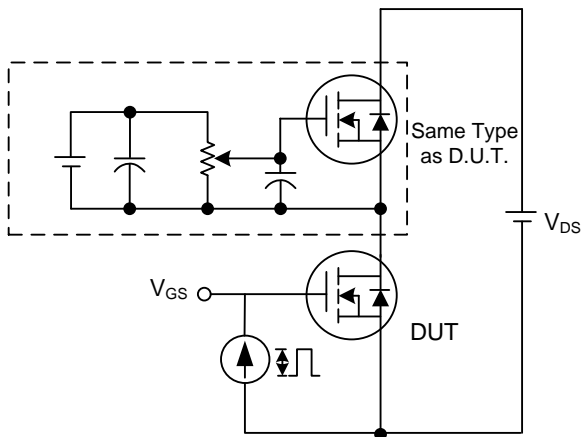
■ TEST CIRCUITS AND WAVEFORMS



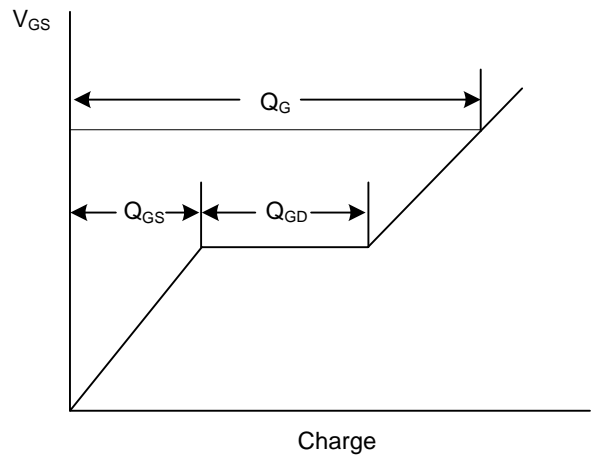
Switching Test Circuit



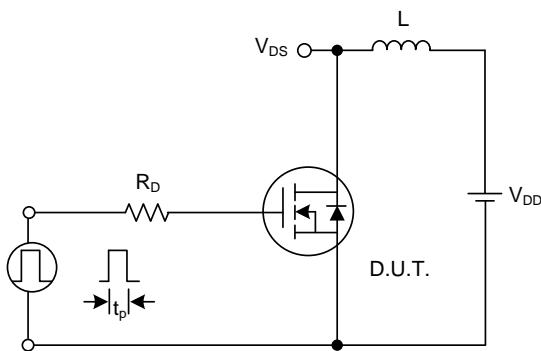
Switching Waveforms



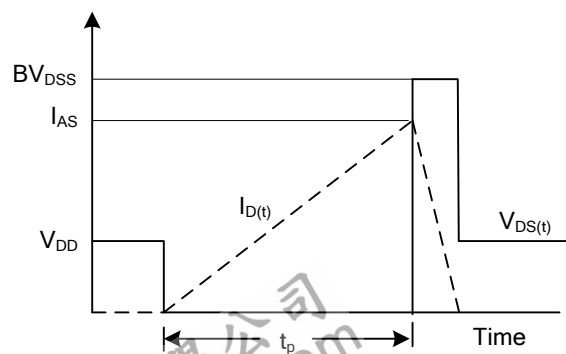
Gate Charge Test Circuit



Gate Charge Waveform

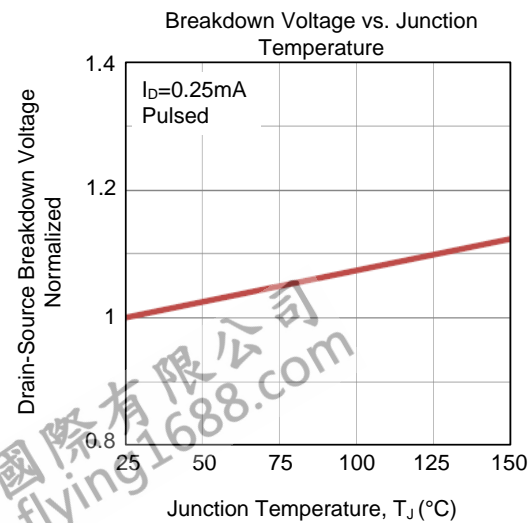
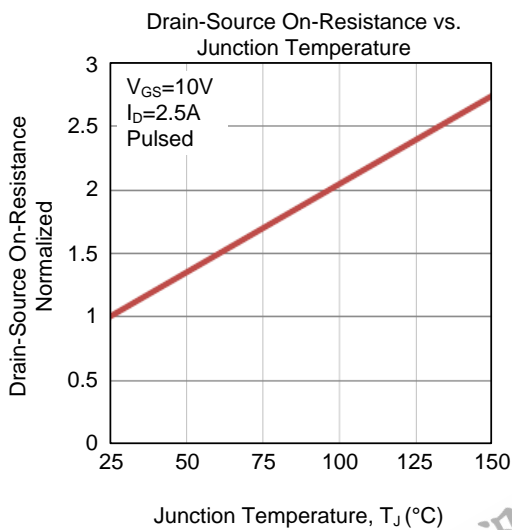
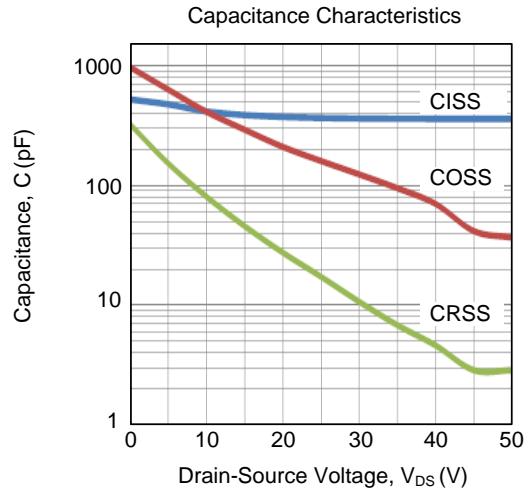
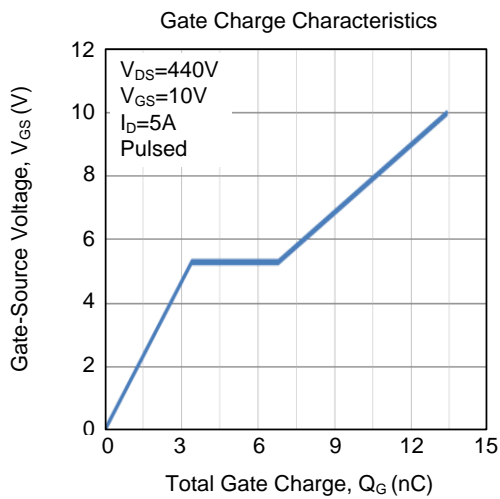
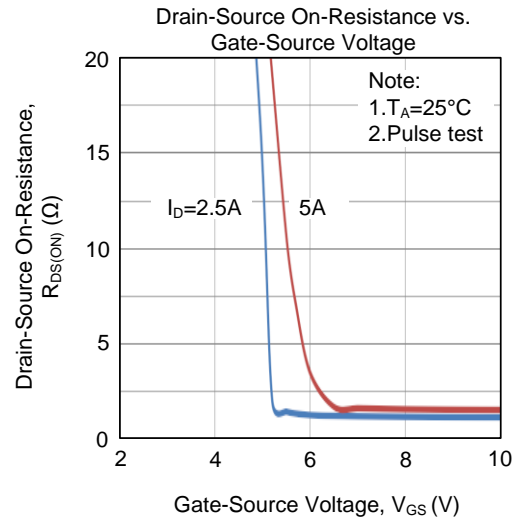
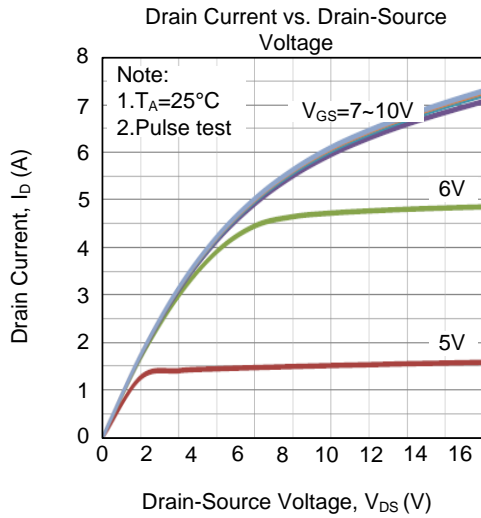


Unclamped Inductive Switching Test Circuit

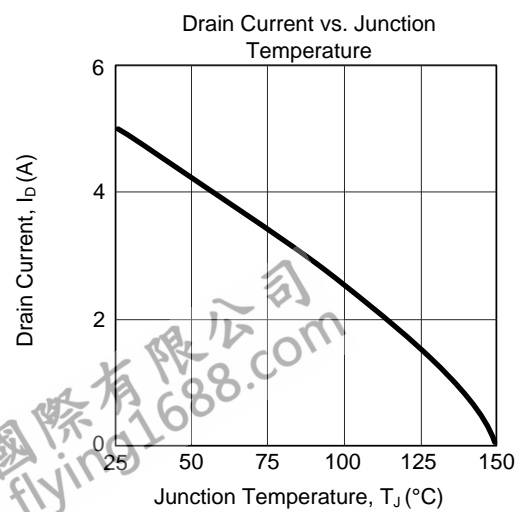
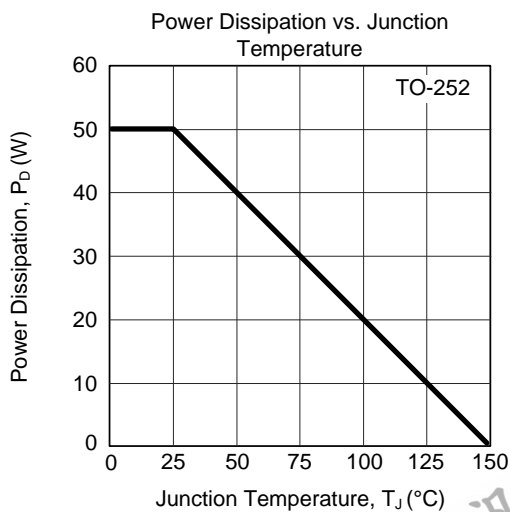
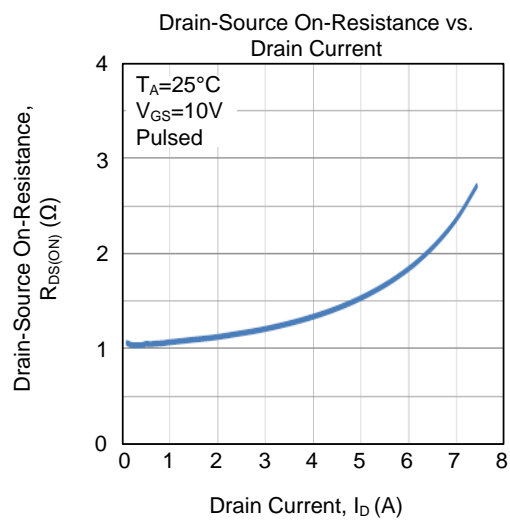
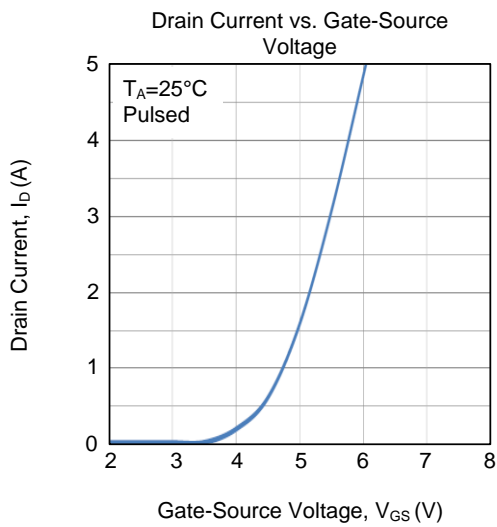
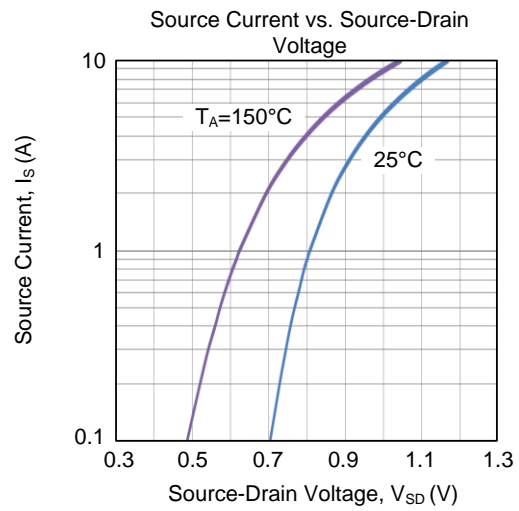
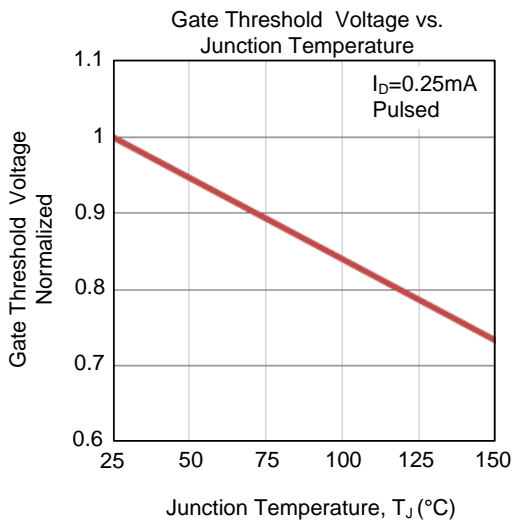


Unclamped Inductive Switching Waveforms

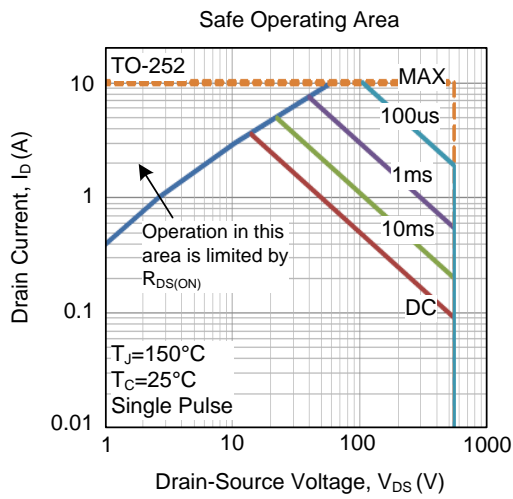
■ TYPICAL CHARACTERISTICS



■ TYPICAL CHARACTERISTICS (Cont.)



■ TYPICAL CHARACTERISTICS (Cont.)



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