



6N40-TC

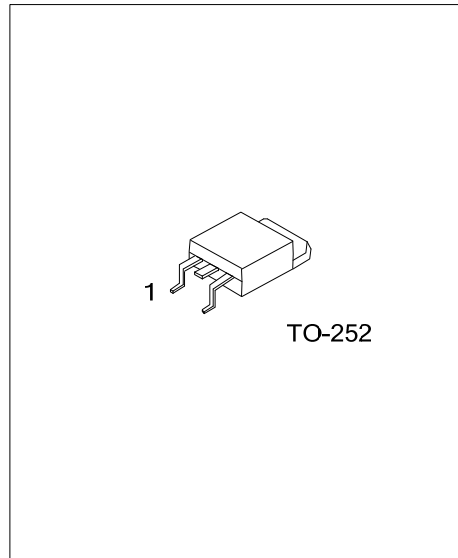
Preliminary

Power MOSFET

**6A, 400V N-CHANNEL
POWER MOSFET**

■ DESCRIPTION

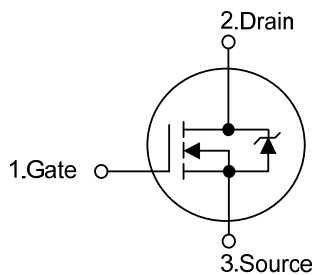
The N-Channel enhancement mode silicon gate power MOSFET is designed for high voltage, high speed power switching applications such as switching regulators, switching converters, solenoid, motor drivers, relay drivers.



■ FEATURES

- * $R_{DS(ON)} < 1.1\Omega @ V_{GS}=10V, I_D=3.0A$
- * Avalanche Energy Specified
- * Fast Switching Capability
- * Linear Transfer Characteristics
- * High Input Impedance

■ SYMBOL



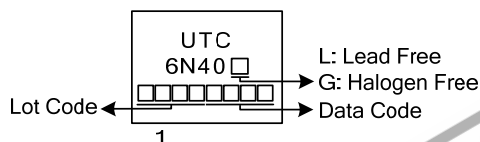
■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
6N40L-TN3-R	6N40G-TN3-R	TO-252	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>6N40G-TN3-R</p> <p>(1)Packing Type</p> <p>(2)Package Type</p> <p>(3)Green Package</p>	<p>(1) R: Tape Reel</p> <p>(2) TN3: TO-252</p> <p>(3) G: Halogen Free and Lead Free, L: Lead Free</p>
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■ MARKING



■ ABSOLUTE MAXIMUM RATINGS ($T_C=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	400	V
Gate-Source Voltage		V_{GSS}	± 20	V
Drain Current	Continuous	I_D	6.0	A
	Pulsed (Note 2)	I_{DM}	24	A
Avalanche Current (Note 2)		I_{AR}	4.6	A
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	106	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	2.0	V/ns
Power Dissipation		P_D	48	W
Junction Temperature		T_J	+150	$^{\circ}\text{C}$
Storage Temperature		T_{STG}	-55 ~ +150	$^{\circ}\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $L = 10\text{mH}$, $I_{AS} = 4.6\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 25\Omega$, Starting $T_J = 25^{\circ}\text{C}$

4. $I_{SD} \leq 5.5\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^{\circ}\text{C}$

■ THERMAL DATA

PARAMETER	SYMBOL	RATING	UNIT
Junction to Ambient	θ_{JA}	110	$^{\circ}\text{C}/\text{W}$
Junction to Case	θ_{JC}	2.6	$^{\circ}\text{C}/\text{W}$

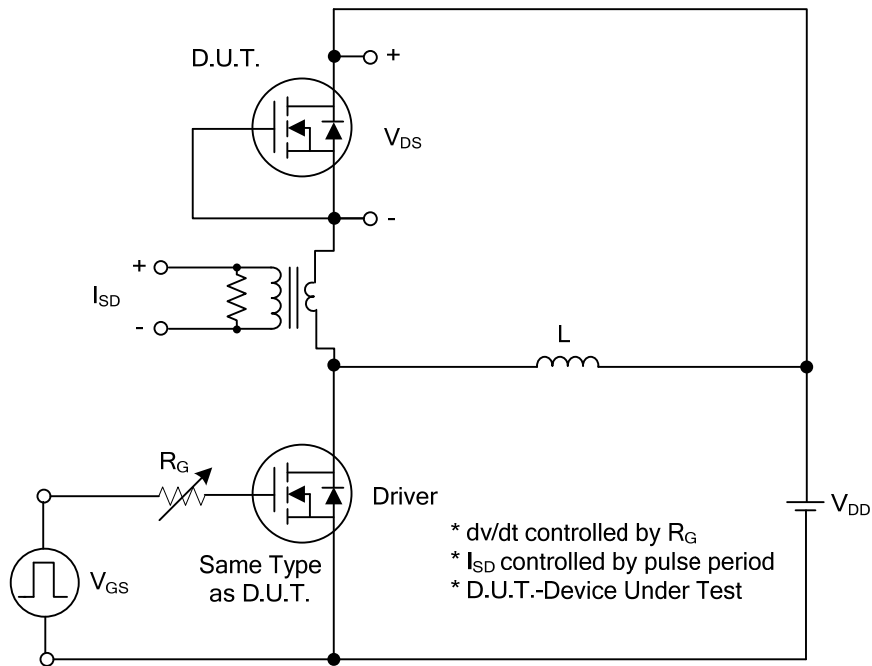
■ ELECTRICAL CHARACTERISTICS ($T_J=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0\text{V}$, $I_D=250\mu\text{A}$	400			V
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=\text{Rated } BV_{DSS}$, $V_{GS}=0\text{V}$			25	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 20\text{V}$			± 100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	2.0		4.0	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=3.0\text{A}$			1.1	Ω
DYNAMIC CHARACTERISTICS						
Input Capacitance	C_{ISS}	$V_{GS}=0\text{V}$, $V_{DS}=25\text{V}$, $f=1.0\text{MHz}$		485		pF
Output Capacitance	C_{OSS}			70		pF
Reverse Transfer Capacitance	C_{RSS}			7		pF
SWITCHING CHARACTERISTICS						
Total Gate Charge (Note 1)	Q_G	$V_{DS}=50\text{V}$, $V_{GS}=10\text{V}$, $I_D=1.3\text{A}$ $I_G=100\mu\text{A}$ (Note1, 2)		35.4		nC
Gate to Source Charge	Q_{GS}			3.6		nC
Gate to Drain Charge	Q_{GD}			5.8		nC
Turn-ON Delay Time (Note 1)	$t_{D(ON)}$	$V_{DS}=30\text{V}$, $V_{GS}=10\text{V}$, $I_D=0.5\text{A}$, $R_G=25\Omega$ (Note1, 2)		31		ns
Rise Time	t_R			40		ns
Turn-OFF Delay Time	$t_{D(OFF)}$			117		ns
Fall-Time	t_F			38		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Body-Diode Continuous Current	I_S				6	A
Maximum Body-Diode Pulsed Current	I_{SM}				24	A
Drain-Source Diode Forward Voltage (Note 1)	V_{SD}	$I_S=6.0\text{A}$, $V_{GS}=0\text{V}$			1.6	V
Body Diode Reverse Recovery Time (Note 1)	t_{rr}	$I_S=6.0\text{A}$, $V_{GS}=0\text{V}$		220		ns
Body Diode Reverse Recovery Charge	Q_{rr}	$di/dt=100\text{A}/\mu\text{s}$		1.0		μC

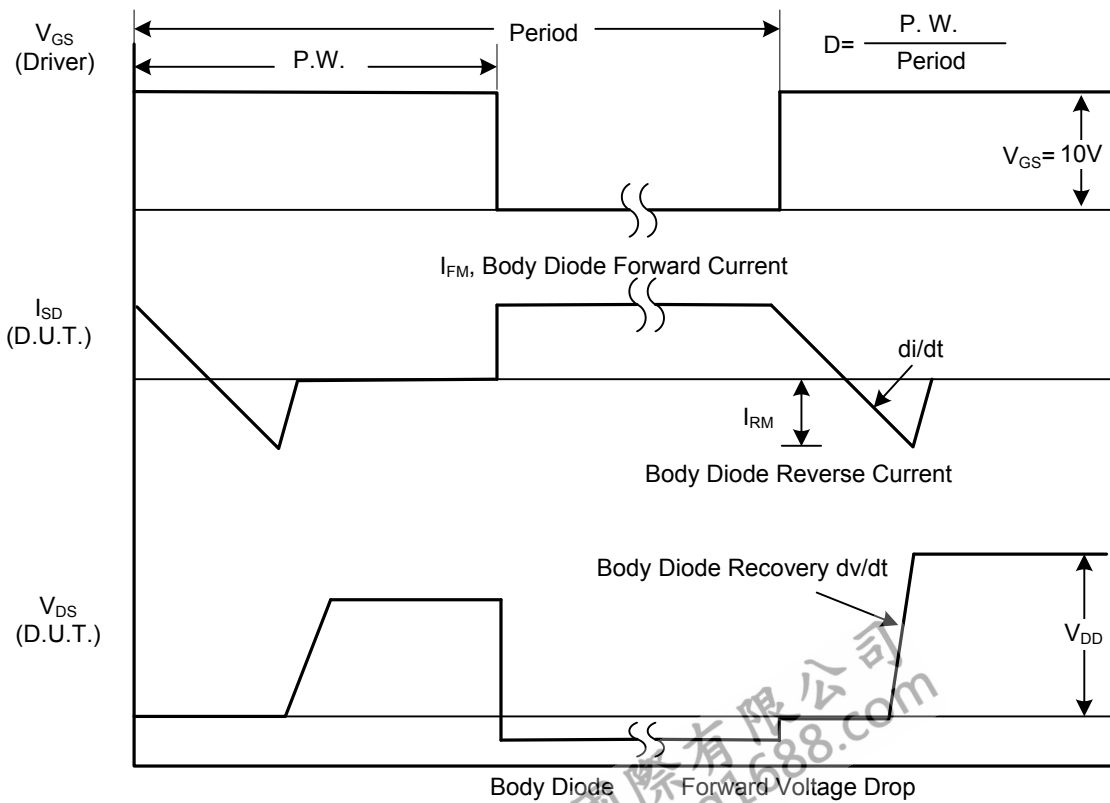
Notes: 1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS



Peak Diode Recovery dv/dt Test Circuit



Peak Diode Recovery dv/dt Waveforms

■ TEST CIRCUITS AND WAVEFORMS

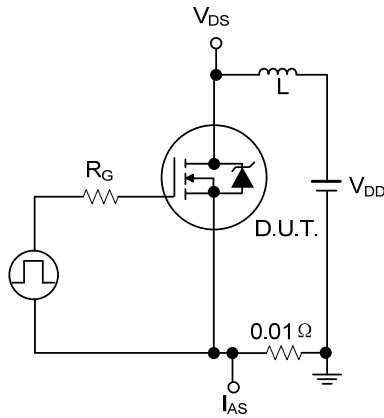


Figure 1A. Unclamped Energy Test Circuit

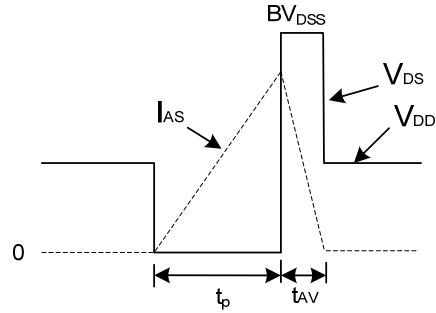


Figure 1B. Unclamped Energy Waveforms

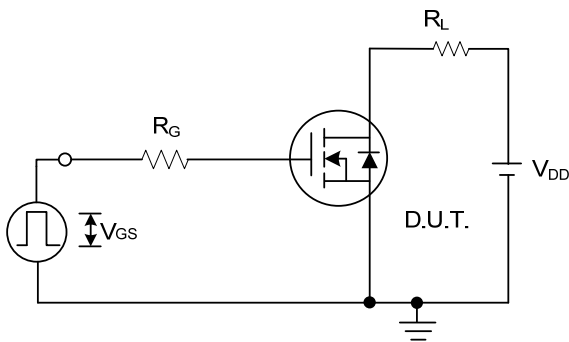


Figure 2A. Switching Time Test Circuit

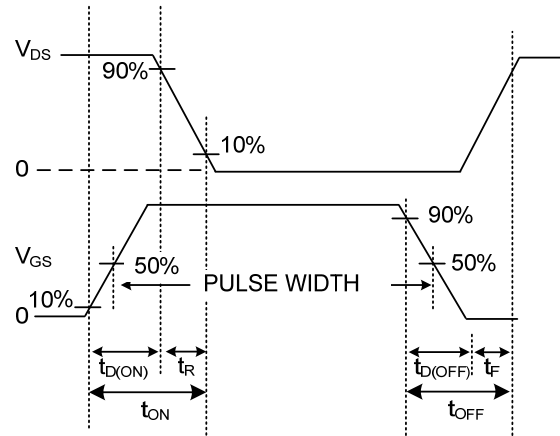


Figure 2B. Resistive Switching Waveforms

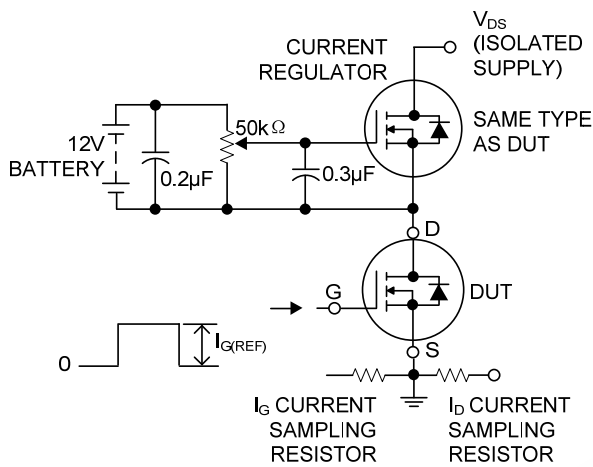


Figure 3A. Gate Charge Test Circuit

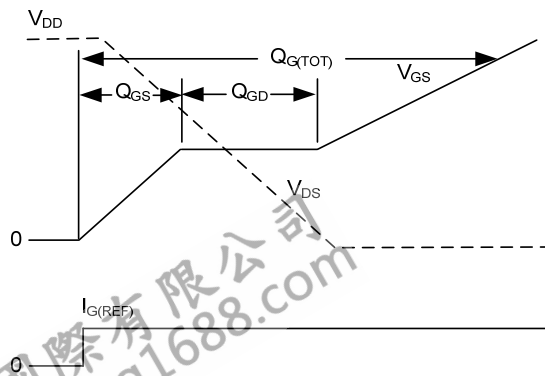


Figure 3B. Gate Charge Waveforms

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