



6N60-FTC

Power MOSFET

6A, 600V N-CHANNEL POWER MOSFET

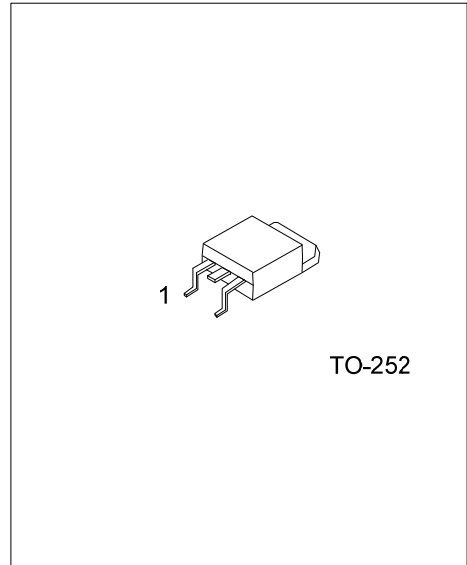
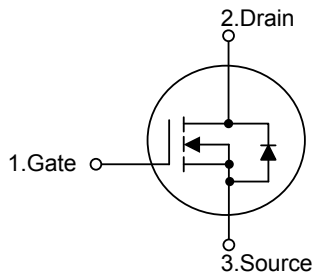
DESCRIPTION

The UTC **6N60-FTC** is a high voltage power MOSFET and is designed to have better characteristics, such as fast switching time, low gate charge, low on-state resistance and have a high rugged avalanche characteristics. This power MOSFET is usually used at high speed switching applications in switching power supplies and adaptors.

FEATURES

- * $R_{DS(ON)} \leq 1.8\Omega @ V_{GS}=10V, I_D=3.0A$
- * High Switching Speed

SYMBOL



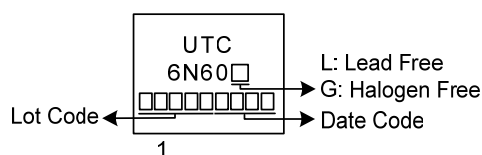
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
6N60L-TN3-R	6N60G-TN3-R	TO-252	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>6N60G-TN3-R</p> <p>(1)Packing Type</p> <p>(2)Package Type</p> <p>(3)Green Package</p>	<p>(1) R: Tape Reel</p> <p>(2) TN3: TO-252</p> <p>(3) G: Halogen Free and Lead Free, L: Lead Free</p>
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MARKING



■ ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Drain-Source Voltage	V_{DSS}	600	V
Gate-Source Voltage	V_{GSS}	± 30	V
Drain Current	Continuous	I_D	6
	Pulsed (Note 2)	I_{DM}	12
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	120
Peak Diode Recovery dv/dt (Note 4)	dv/dt	3.3	V/ns
Power Dissipation	P_D	55	W
Junction Temperature	T_J	+150	$^\circ\text{C}$
Storage Temperature	T_{STG}	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $L = 10\text{mH}$, $I_{AS} = 4.9\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 25\Omega$ Starting $T_J = 25^\circ\text{C}$

4. $I_{SD} \leq 6.0\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	62.5	$^\circ\text{C}/\text{W}$
Junction to Case	θ_{JC}	2.27	$^\circ\text{C}/\text{W}$

Note: The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.

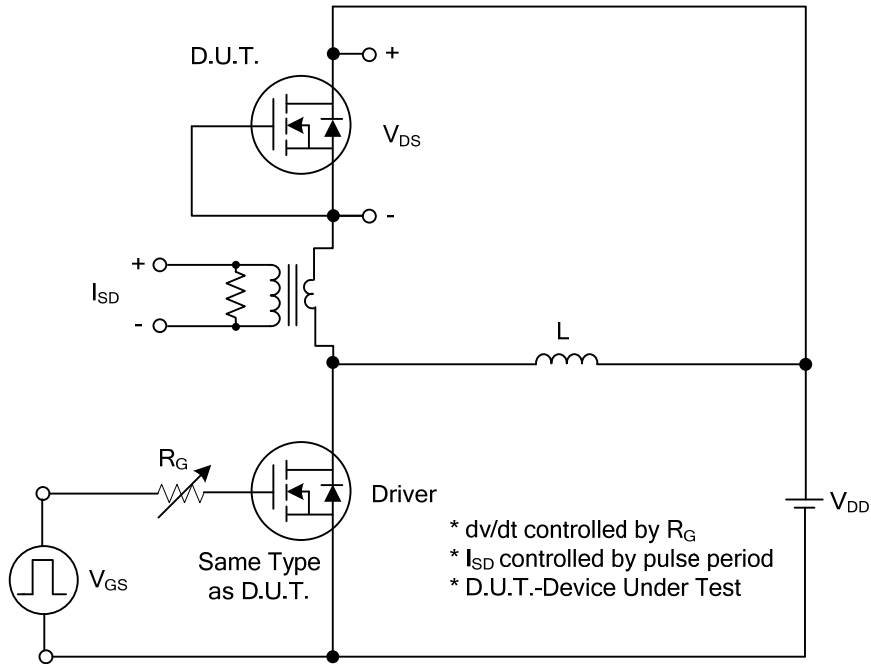
■ ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0\text{V}$, $I_D=250\mu\text{A}$	600			V
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=600\text{V}$, $V_{GS}=0\text{V}$			10	μA
Gate-Source Leakage Current	Forward	I_{GSS}			100	nA
	Reverse					
		$V_{GS}=-30\text{V}$, $V_{DS}=0\text{V}$			-100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	2.0		4.0	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=3.0\text{A}$			1.8	Ω
DYNAMIC CHARACTERISTICS						
Input Capacitance	C_{ISS}	$V_{GS}=0\text{V}$, $V_{DS}=25\text{V}$, $f=1.0\text{MHz}$		682		pF
Output Capacitance	C_{OSS}			80		pF
Reverse Transfer Capacitance	C_{RSS}			5.5		pF
SWITCHING CHARACTERISTICS						
Total Gate Charge (Note 1)	Q_G	$V_{DS}=480\text{V}$, $V_{GS}=10\text{V}$, $I_D=6.0\text{A}$ $I_G=1\text{mA}$ (Note 1, 2)		20		nC
Gate-source Charge	Q_{GS}			7.2		nC
Gate-drain Charge	Q_{GD}			4		nC
Turn-on Delay Time (Note 1)	$t_{D(ON)}$	$V_{DS}=100\text{V}$, $V_{GS}=10\text{V}$, $I_D=6.0\text{A}$, $R_G=25\Omega$ (Note 1, 2)		8		ns
Rise Time	t_R			16.8		ns
Turn-off Delay Time	$t_{D(OFF)}$			52		ns
Fall-Time	t_F			27.5		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Continuous Drain-Source Diode Forward Current	I_S				6	A
Maximum Pulsed Drain-Source Diode Forward Current	I_{SM}				12	A
Drain-Source Diode Forward Voltage (Note 1)	V_{SD}	$V_{GS}=0\text{V}$, $I_S=6.0\text{A}$			1.4	V
Reverse Recovery Time (Note 1)	t_{rr}	$V_{GS}=0\text{V}$, $I_S=6.0\text{A}$,		137		ns
Reverse Recovery Charge	Q_{rr}	$di/dt=100\text{A}/\mu\text{s}$ (Note1)		0.5		μC

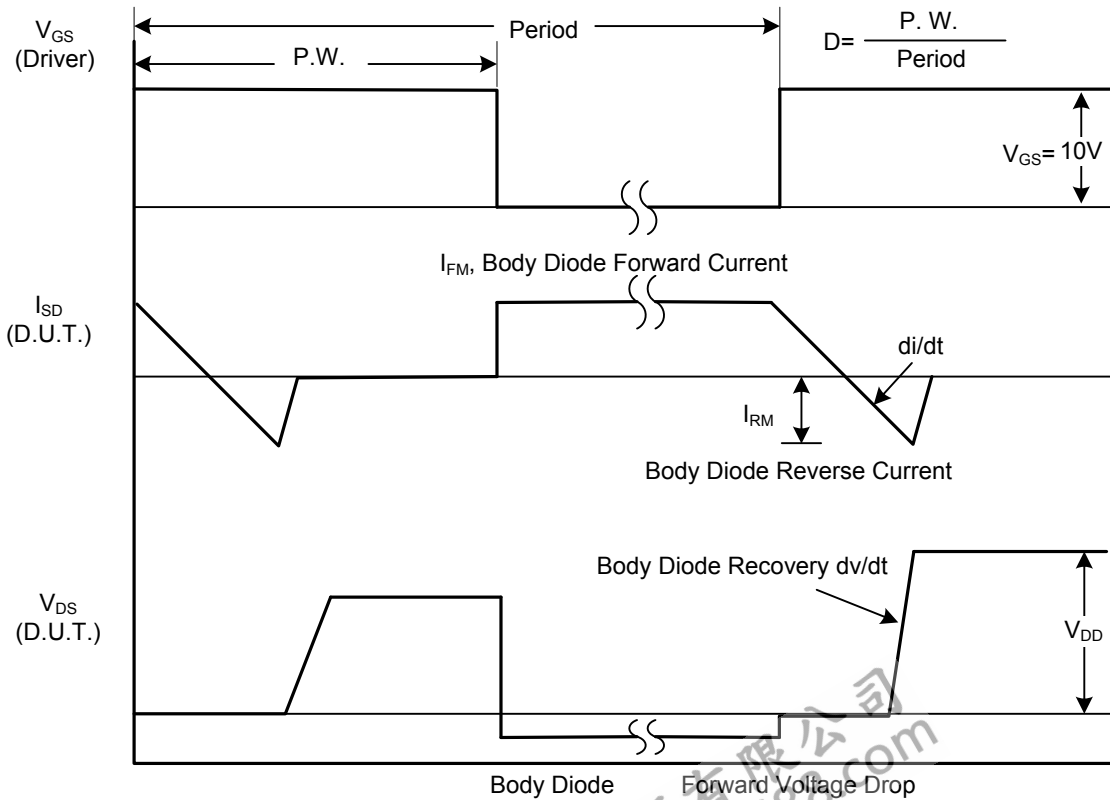
Notes: 1. Pulse Test : Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

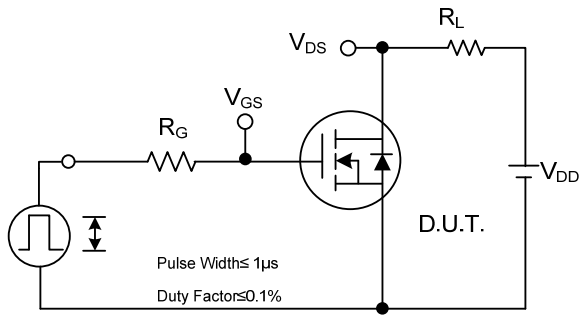


Peak Diode Recovery dv/dt Test Circuit

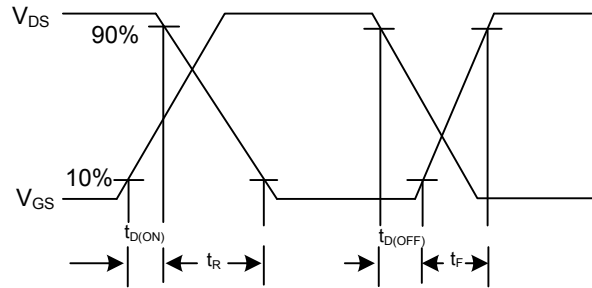


Peak Diode Recovery dv/dt Waveforms

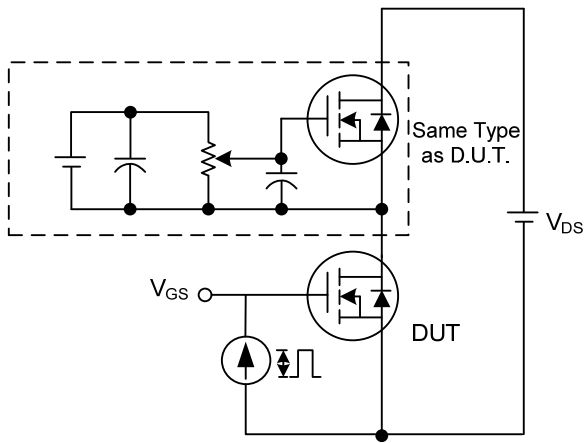
■ TEST CIRCUITS AND WAVEFORMS



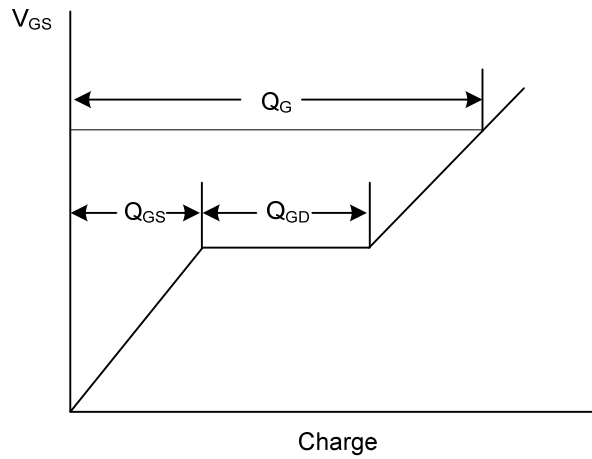
Switching Test Circuit



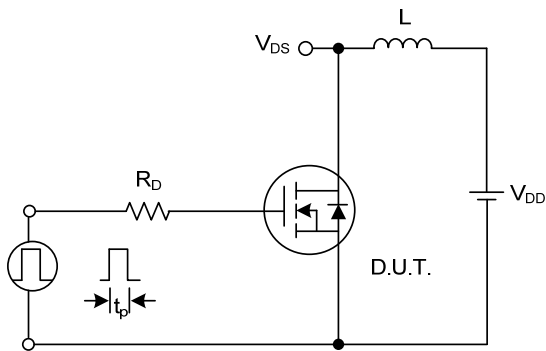
Switching Waveforms



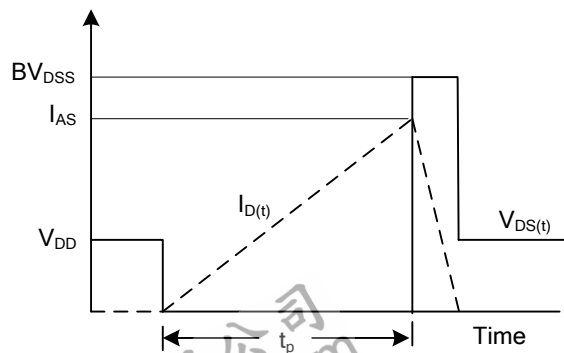
Gate Charge Test Circuit



Gate Charge Waveform

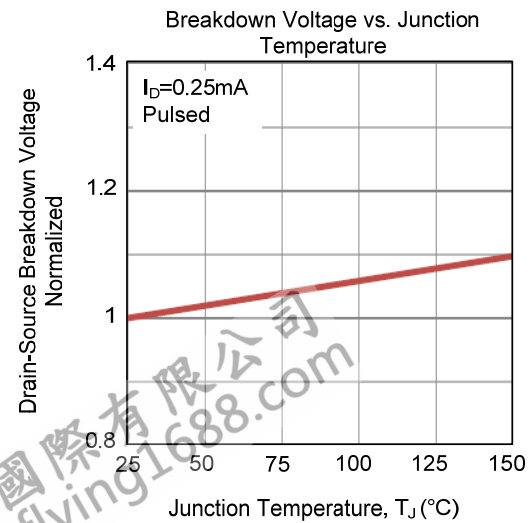
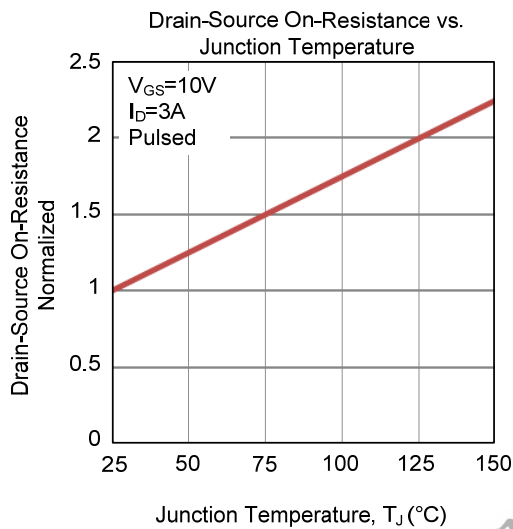
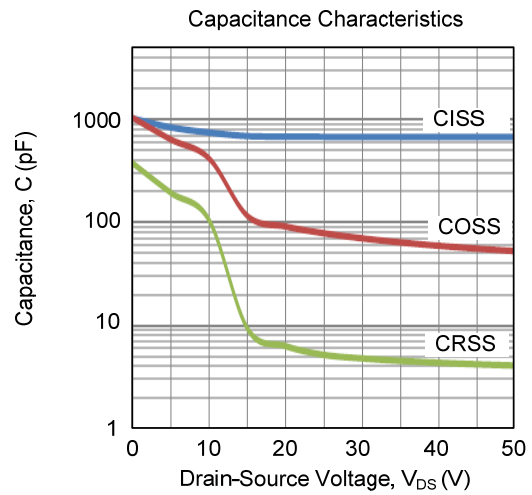
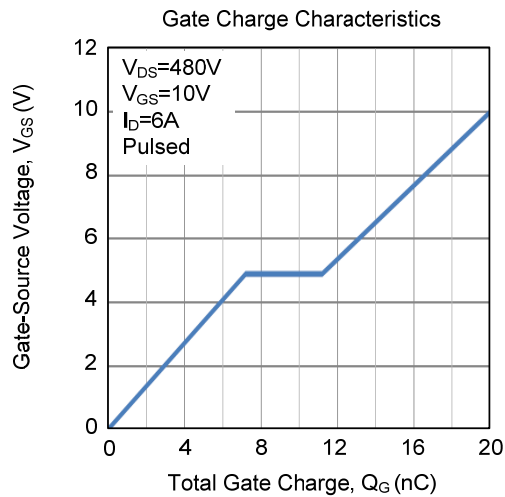
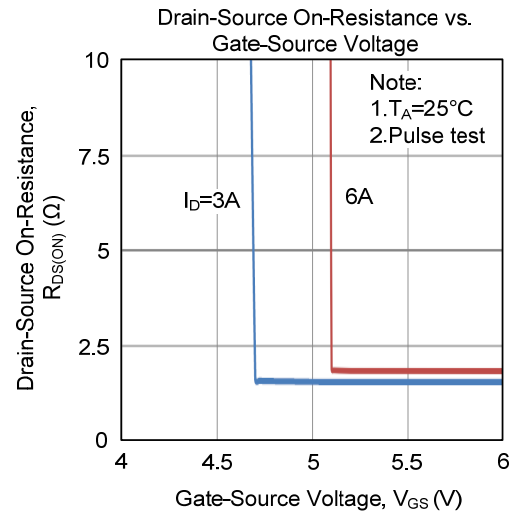
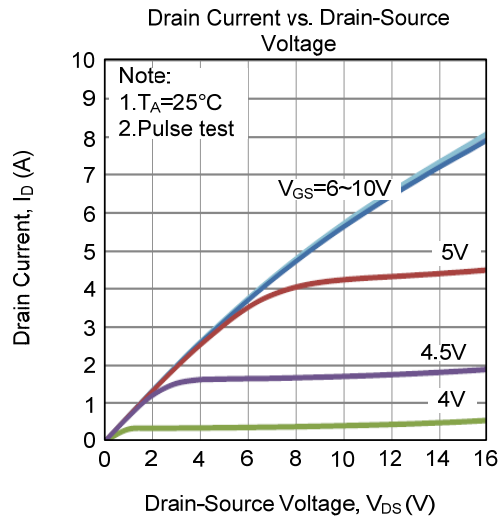


Unclamped Inductive Switching Test Circuit

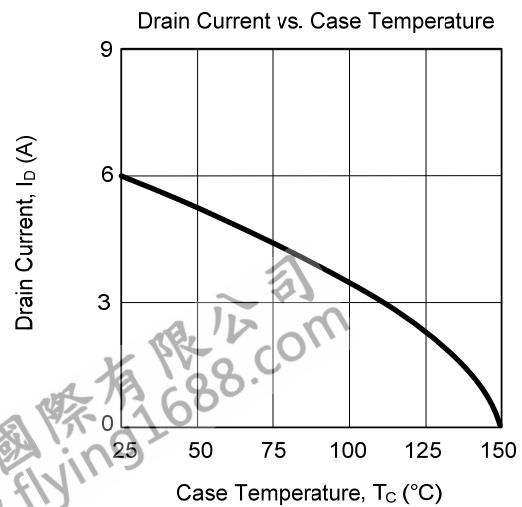
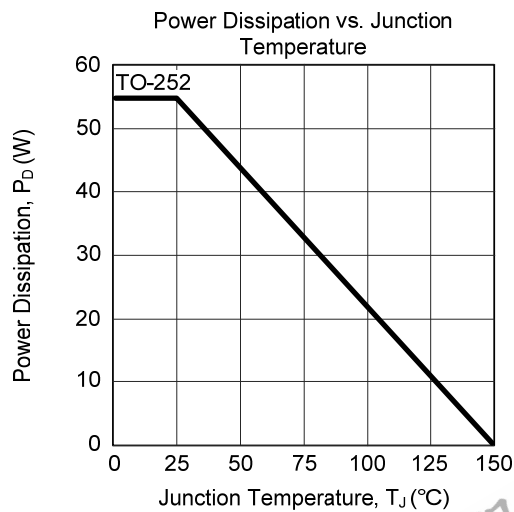
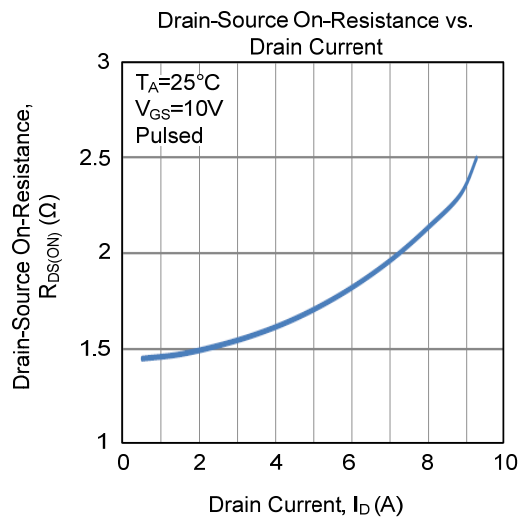
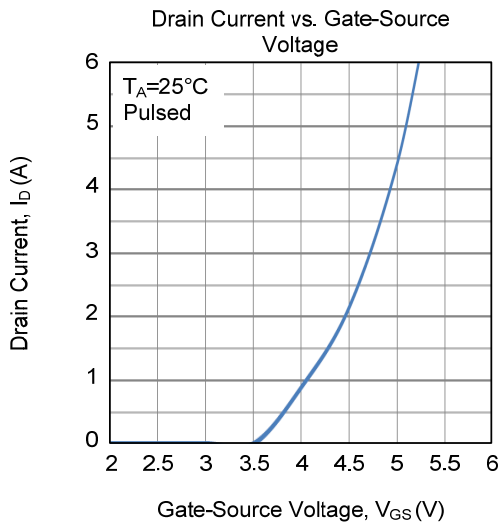
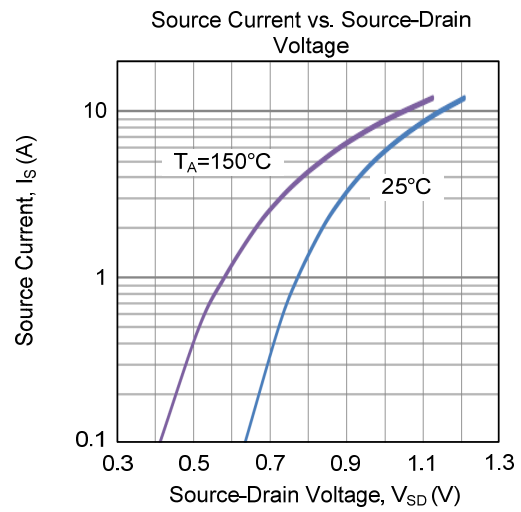
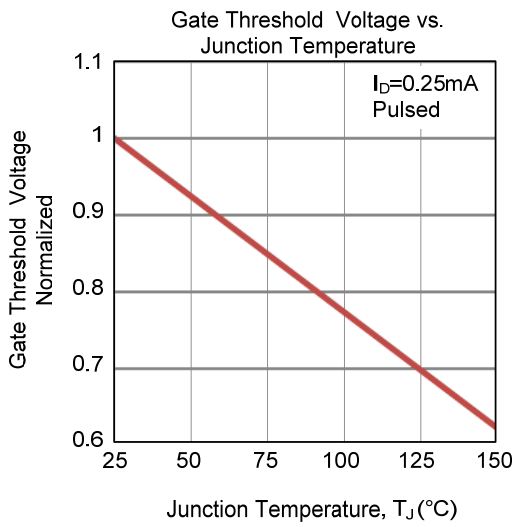


Unclamped Inductive Switching Waveforms

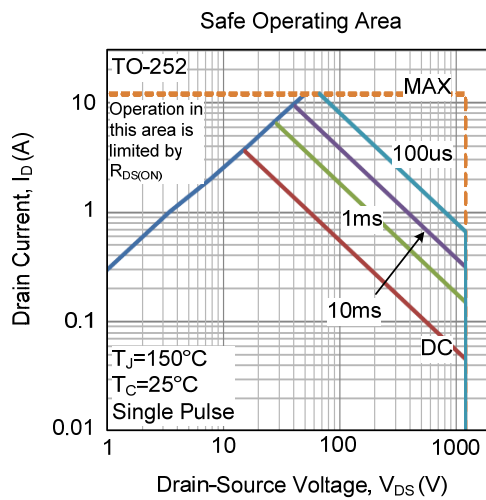
TYPICAL CHARACTERISTICS



■ TYPICAL CHARACTERISTICS (Cont.)



■ TYPICAL CHARACTERISTICS (Cont.)



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