



75NM65

Power MOSFET

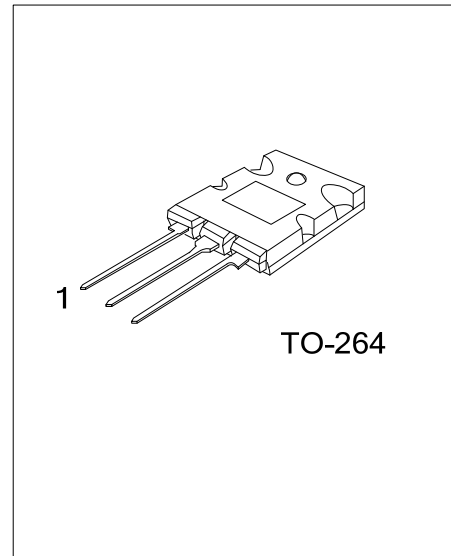
75A, 650V N-CHANNEL SUPER-JUNCTION MOSFET

DESCRIPTION

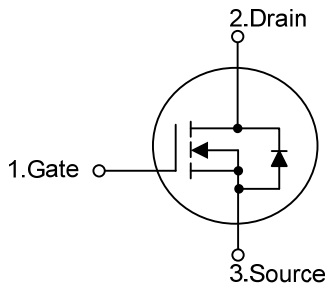
The **UTC 75NM65** is a Super Junction MOSFET Structure and is designed to have better characteristics, such as fast switching time, low gate charge, low on-state resistance and a high rugged avalanche characteristics. This power MOSFET is usually used at AC-DC converters for power applications.

FEATURES

- * $R_{DS(ON)} \leq 48m\Omega$ @ $V_{GS}=10V, I_D=37.5A$
- * Fast switching capability
- * Avalanche energy tested
- * Improved dv/dt capability, high ruggedness



SYMBOL



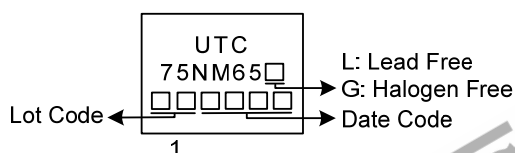
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
75NM65L-T64-T	75NM65G-T64-T	TO-264	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>75NM65G-T64-T</p> <p>(1)Packing Type</p> <p>(2)Package Type</p> <p>(3)Green Package</p>	<p>(1) T: Tube</p> <p>(2) T64: TO-264</p> <p>(3) G: Halogen Free and Lead Free, L: Lead Free</p>
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MARKING



■ ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	650	V
Gate-Source Voltage		V_{GSS}	± 30	V
Drain Current	Continuous	I_D	75	A
	Pulsed (Note 2)	I_{DM}	150	A
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	1711	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	6	V/ns
Power Dissipation		P_D	446	W
Junction Temperature		T_J	+150	$^\circ\text{C}$
Storage Temperature Range		T_{STG}	-55 ~ +150	$^\circ\text{C}$

- Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
 2. Repetitive Rating: Pulse width limited by maximum junction temperature.
 3. $L=10\text{mH}$, $I_{AS}=18.5\text{A}$, $V_{DD}=50\text{V}$, $R_G=25\Omega$, Starting $T_J = 25^\circ\text{C}$.
 4. $I_{SD} \leq 30\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_J = 25^\circ\text{C}$.

■ THERMAL DATA

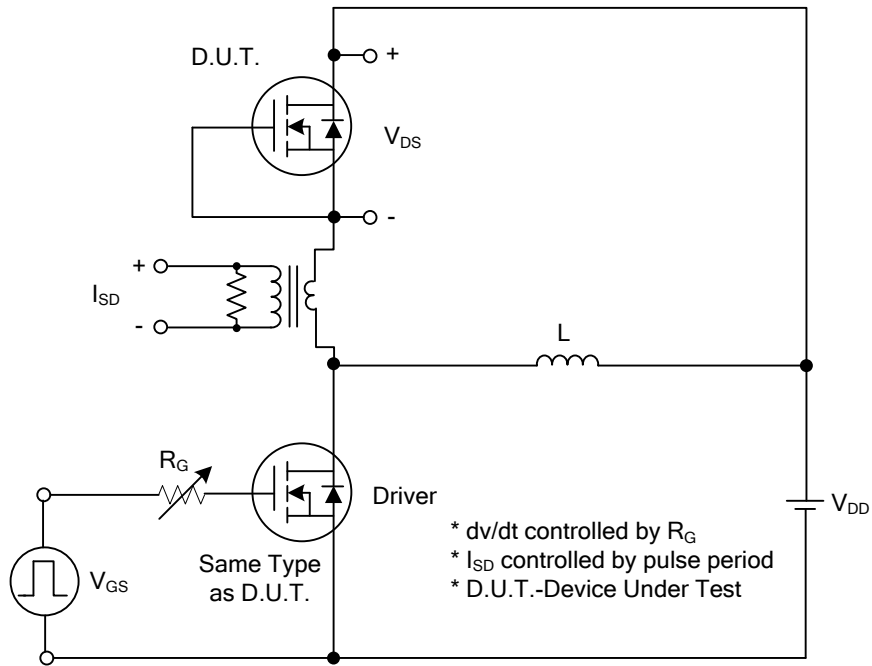
PARAMETER	SYMBOL	RATING	UNIT
Junction to Ambient	θ_{JA}	40	$^\circ\text{C}/\text{W}$
Junction to Case	θ_{JC}	0.28	$^\circ\text{C}/\text{W}$

■ ELECTRICAL CHARACTERISTICS ($T_J=25^\circ\text{C}$, unless otherwise specified)

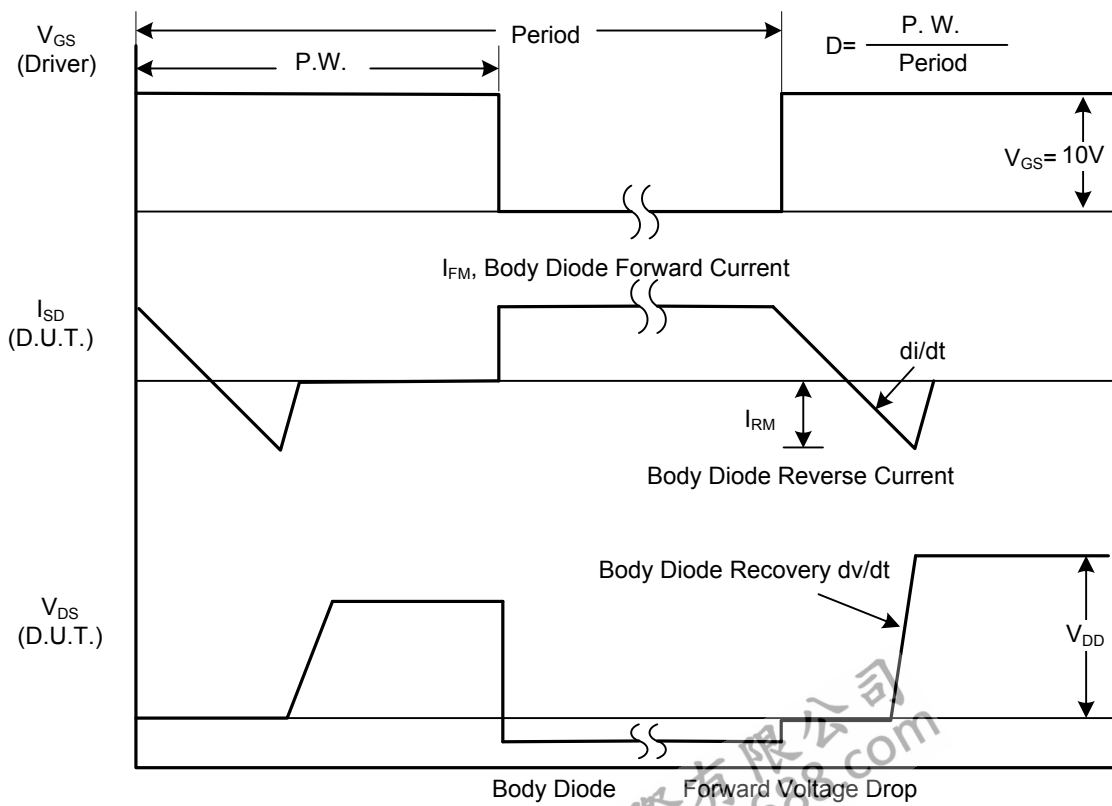
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0\text{V}$, $I_D=250\mu\text{A}$	650			V
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=650\text{V}$, $V_{GS}=0\text{V}$			10	μA
Gate-Source Leakage Current	I_{GSS}	$V_{DS}=0\text{V}$, $V_{GS}=\pm 30\text{V}$			± 100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	2.5		4.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=37.5\text{A}$			48	m Ω
DYNAMIC PARAMETERS						
Input Capacitance	C_{ISS}	$V_{GS}=0\text{V}$, $V_{DS}=25\text{V}$, $f=1.0\text{MHz}$		6400		pF
Output Capacitance	C_{OSS}			4400		pF
Reverse Transfer Capacitance	C_{RSS}			280		pF
SWITCHING PARAMETERS						
Total Gate Charge (Note 1)	Q_G	$V_{DS}=520\text{V}$, $V_{GS}=10\text{V}$, $I_D=75\text{A}$, $I_G=1\text{mA}$ (Note 1, 2)		220		nC
Gate to Source Charge	Q_{GS}			29		nC
Gate to Drain Charge	Q_{GD}			89		nC
Turn-ON Delay Time (Note 1)	$t_{D(ON)}$	$V_{DD}=100\text{V}$, $V_{GS}=10\text{V}$, $I_D=75\text{A}$, $R_G=3.3\Omega$ (Note 1, 2)		30		ns
Rise Time	t_R			28		ns
Turn-OFF Delay Time	$t_{D(OFF)}$			130		ns
Fall-Time	t_F			29		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Body-Diode Continuous Current	I_S				75	A
Maximum Body-Diode Pulsed Current	I_{SM}				150	A
Drain-Source Diode Forward Voltage (Note 1)	V_{SD}	$I_S=75\text{A}$, $V_{GS}=0\text{V}$			1.4	V
Body Diode Reverse Recovery Time (Note 1)	t_{rr}	$I_S=75\text{A}$, $V_{GS}=0\text{V}$		710		ns
Body Diode Reverse Recovery Charge	Q_{rr}	$di/dt=100\text{A}/\mu\text{s}$		16.4		μC

- Notes: 1. Pulse Test : Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.
 2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

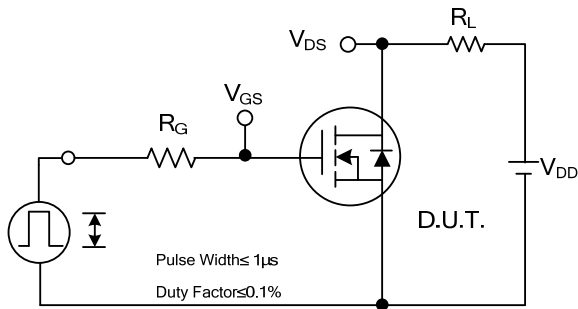


Peak Diode Recovery dv/dt Test Circuit

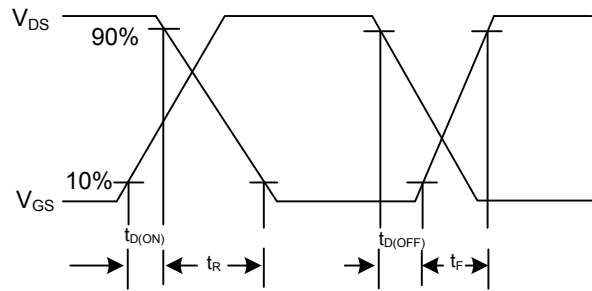


Peak Diode Recovery dv/dt Waveforms

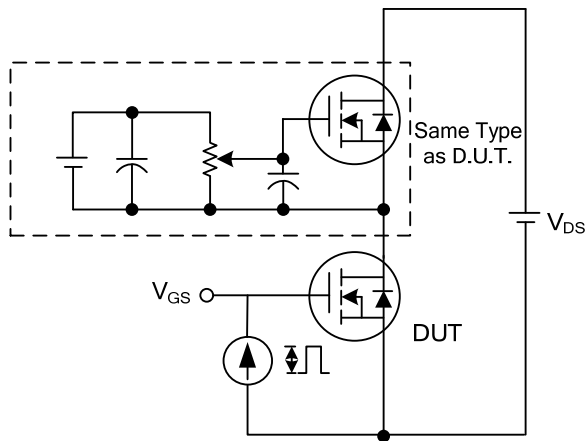
■ TEST CIRCUITS AND WAVEFORMS



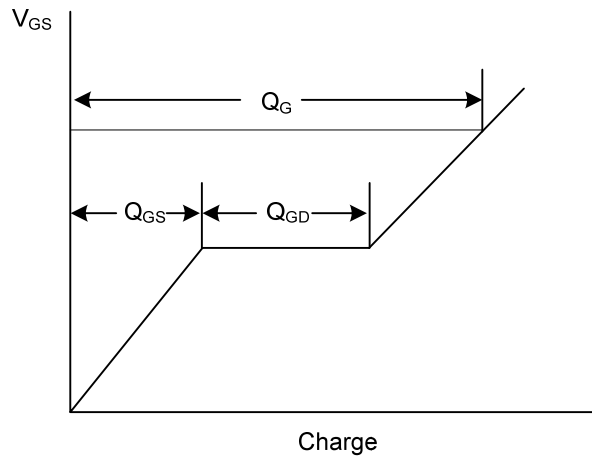
Switching Test Circuit



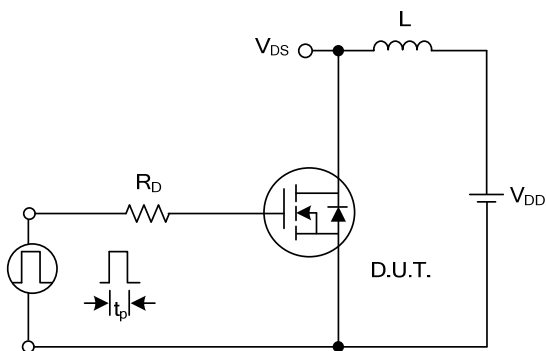
Switching Waveforms



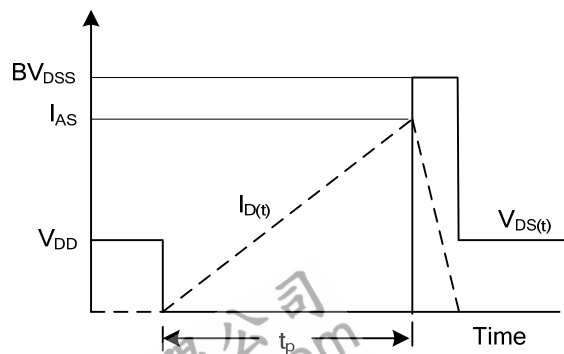
Gate Charge Test Circuit



Gate Charge Waveform

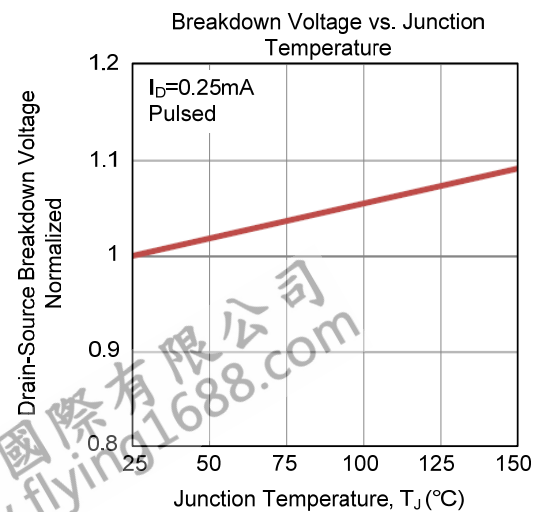
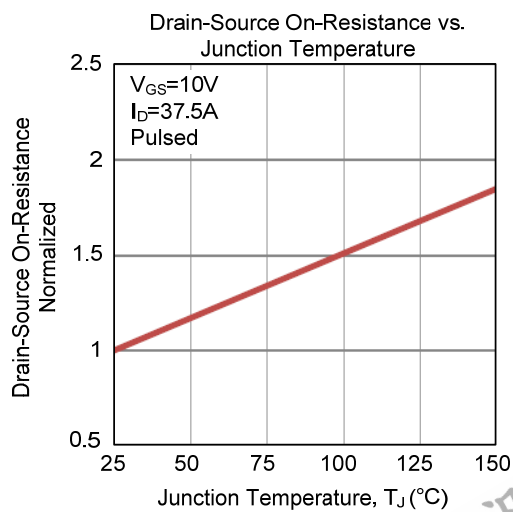
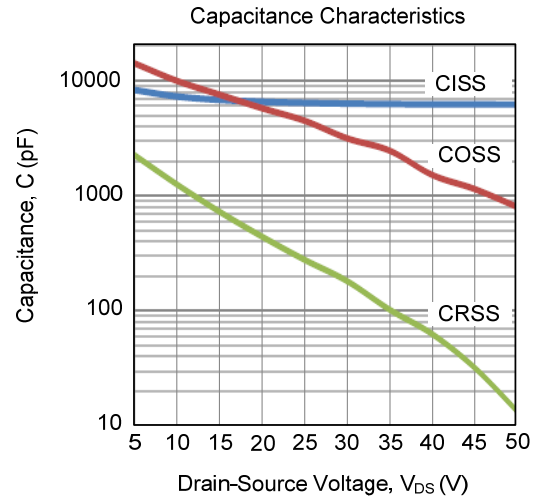
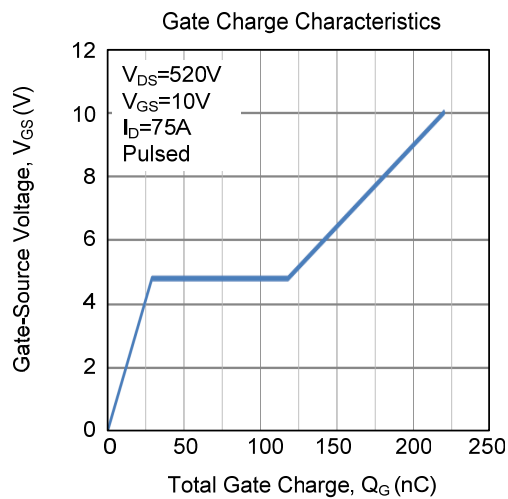
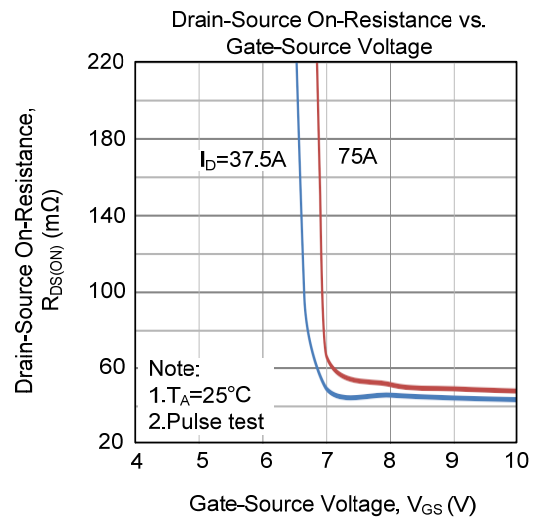
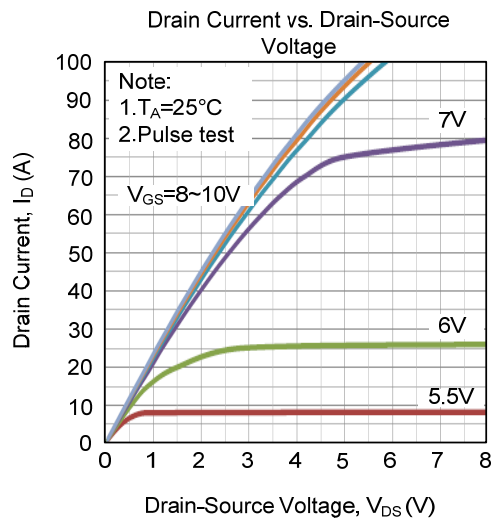


Unclamped Inductive Switching Test Circuit

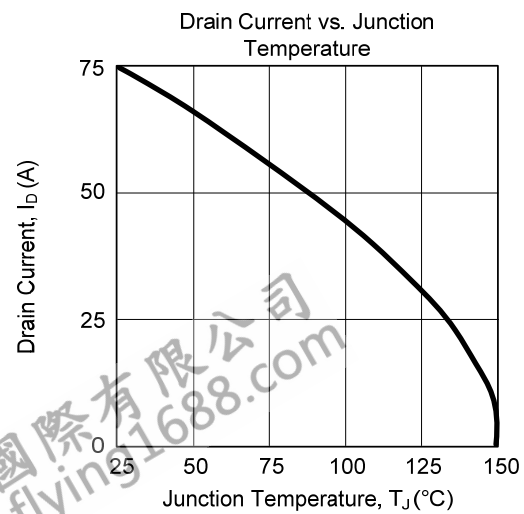
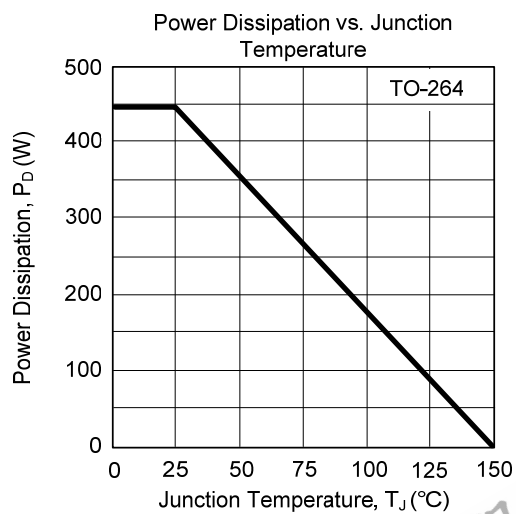
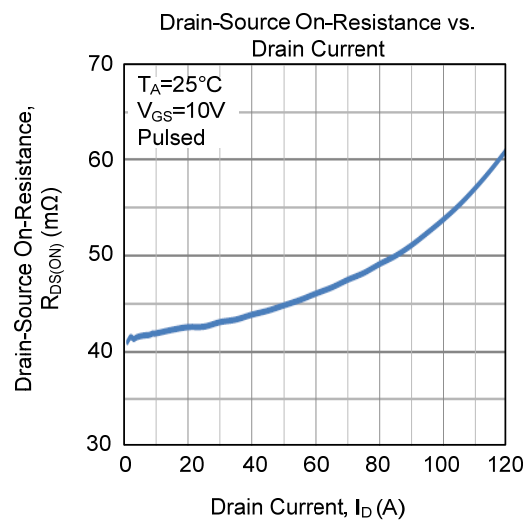
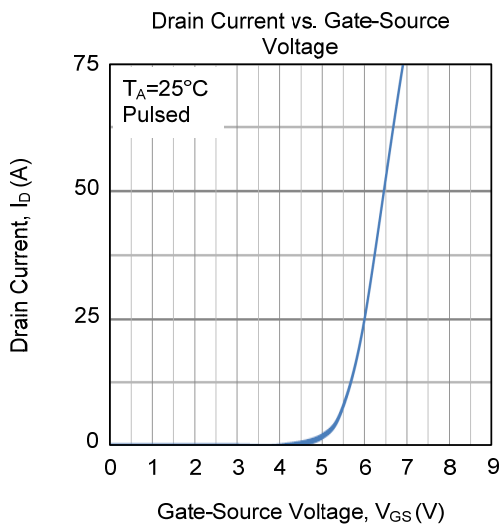
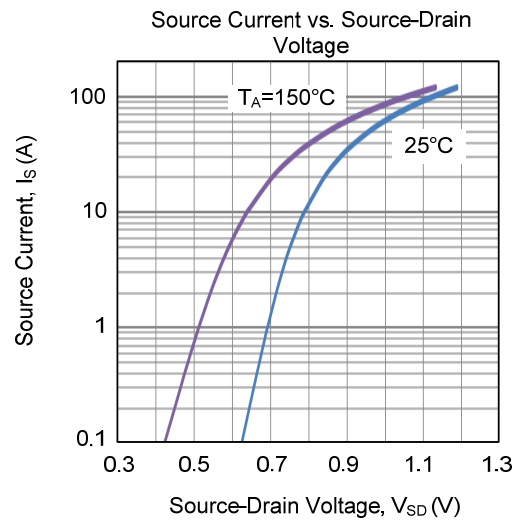
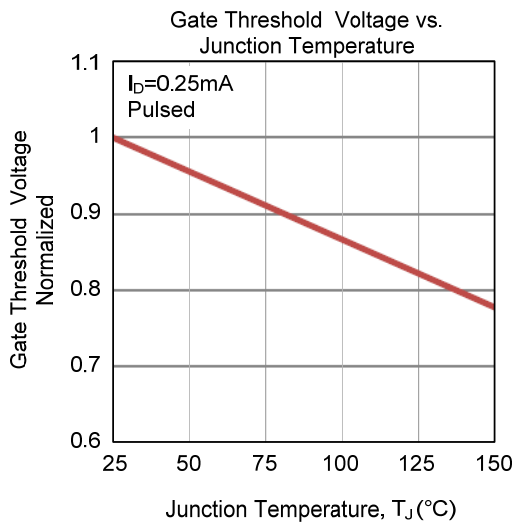


Unclamped Inductive Switching Waveforms

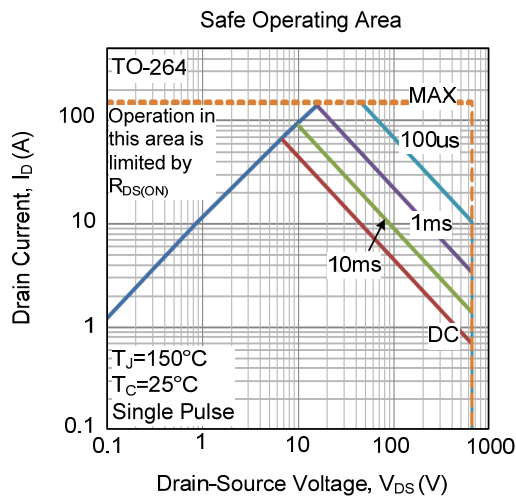
TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS (Cont.)



■ TYPICAL CHARACTERISTICS (Cont.)



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