



## 7N90-MK6

Preliminary

Power MOSFET

### 7A, 900V N-CHANNEL POWER MOSFET

#### DESCRIPTION

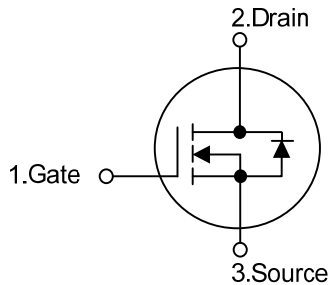
The UTC **7N90-MK6** is an N-channel mode power MOSFET using UTC's advanced technology to provide costumers with planar stripe and DMOS technology. This technology specializes in allowing a minimum on-state resistance and superior switching performance. It also can withstand high energy pulse in the avalanche and commutation mode.

The UTC **7N90-MK6** is universally applied in active power factor correction, electronic lamp ballast based on half bridge topology and high efficient switched mode power supply.

#### FEATURES

- \* High switching speed
- \*  $R_{DS(ON)} < 2.2\Omega @ V_{GS}=10V, I_D=3.5A$
- \* 100% avalanche tested
- \* Improved dv/dt capability

#### SYMBOL



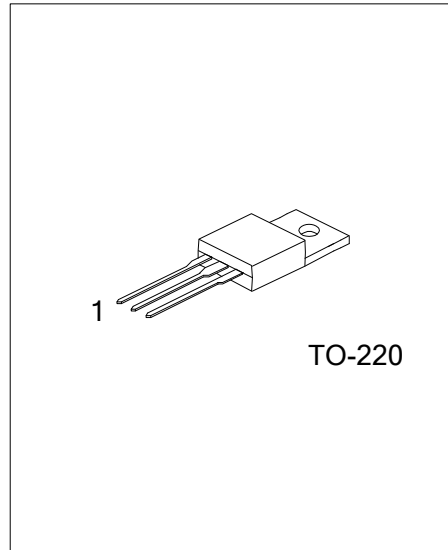
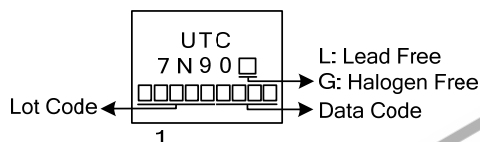
#### ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
7N90L-TA3-T	7N90G-TA3-T	TO-220	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>7N90L-TA3-T</p> <p>(1) Packing Type (2) Package Type (3) Green Package</p>	<p>(1) T: Tube (2) TA3: TO-220 (3) L: Lead Free, G: Halogen Free and Lead Free</p>
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#### MARKING



### ■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNIT	
Drain to Source Voltage	$V_{DSS}$	900	V	
Gate to Source Voltage	$V_{GSS}$	$\pm 30$	V	
Continuous Drain Current	$I_D$	$T_C=25^\circ\text{C}$	7.0	A
		$T_C=100^\circ\text{C}$	4.4	A
Pulsed Drain Current (Note 2)	$I_{DM}$	28	A	
Peak Diode Recovery $dv/dt$ (Note 3)	$dv/dt$	4.0	V/ns	
Power Dissipation	$P_D$	52	W	
Junction Temperature	$T_J$	+150	$^\circ\text{C}$	
Storage Temperature	$T_{STG}$	-55 ~ +150	$^\circ\text{C}$	

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating : Pulse width limited by maximum junction temperature

3.  $I_{SD} \leq 7.0\text{A}$ ,  $di/dt \leq 200\text{A}/\mu\text{s}$ ,  $V_{DD} \leq BV_{DSS}$ , Starting  $T_J=25^\circ\text{C}$

### ■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	$\theta_{JA}$	62.5	$^\circ\text{C}/\text{W}$
Junction to Case	$\theta_{JC}$	2.4	$^\circ\text{C}/\text{W}$

### ■ ELECTRICAL CHARACTERISTICS ( $T_C=25^\circ\text{C}$ , unless otherwise specified)

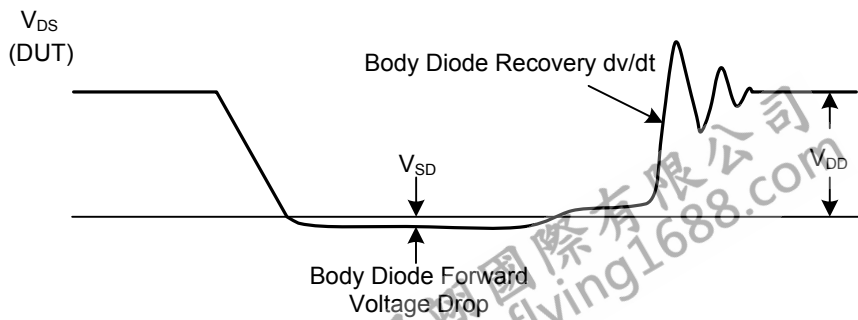
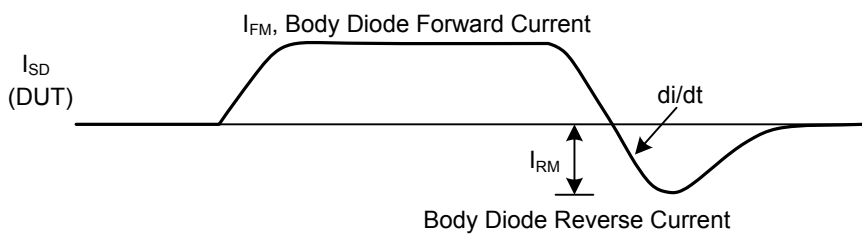
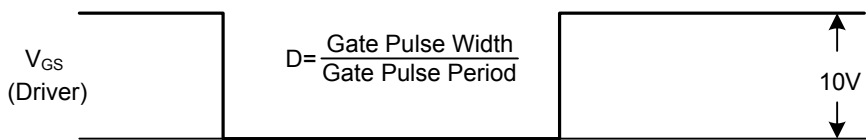
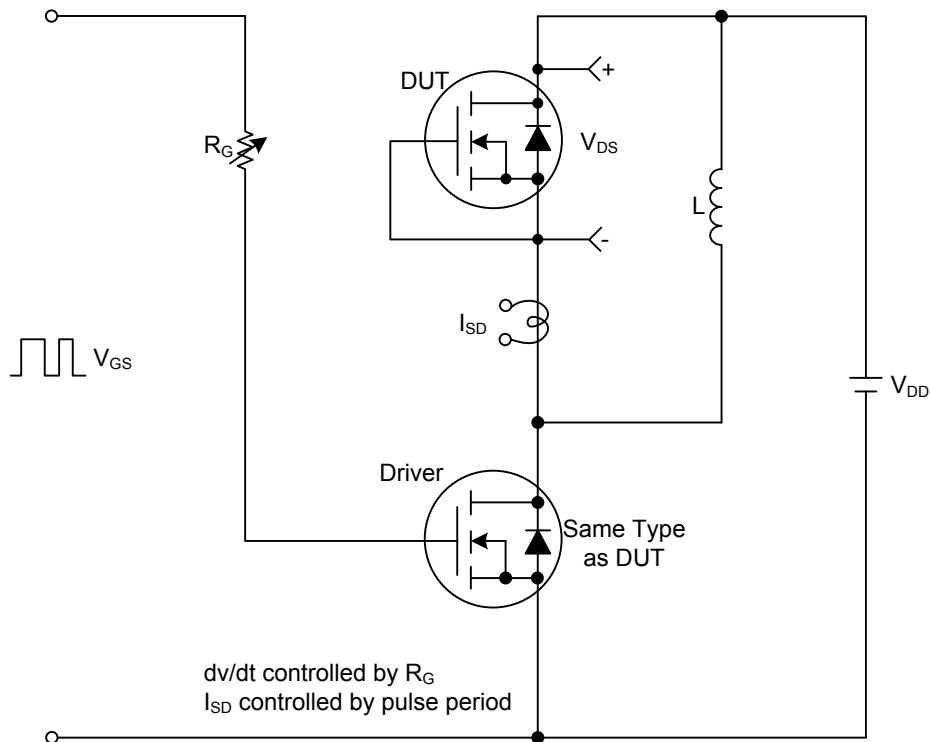
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>OFF CHARACTERISTICS</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0\text{V}$ , $I_D=250\mu\text{A}$	900			V
Breakdown Voltage Temperature Coefficient	$\Delta BV_{DSS}/\Delta T_J$	$I_D=250\mu\text{A}$ , Referenced to $25^\circ\text{C}$		0.96		$\text{V}/^\circ\text{C}$
Drain-Source Leakage Current	$I_{DSS}$	$V_{DS}=900\text{V}$ , $V_{GS}=0\text{V}$			10	$\mu\text{A}$
		$V_{DS}=720\text{V}$ , $T_C=125^\circ\text{C}$			100	$\mu\text{A}$
Gate-Source Leakage Current	Forward	$I_{GSS}$ , $V_{DS}=0\text{V}$ , $V_{GS}=30\text{V}$			100	nA
	Reverse	$I_{GSS}$ , $V_{DS}=0\text{V}$ , $V_{GS}=-30\text{V}$			-100	nA
<b>ON CHARACTERISTICS</b>						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}$ , $I_D=250\mu\text{A}$	3.0		5.0	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$ , $I_D=3.5\text{A}$		1.8	2.2	$\Omega$
<b>DYNAMIC PARAMETERS</b>						
Input Capacitance	$C_{ISS}$	$V_{DS}=25\text{V}$ , $V_{GS}=0\text{V}$ , $f=1.0\text{MHz}$		1450	1880	pF
Output Capacitance	$C_{OSS}$			115	140	pF
Reverse Transfer Capacitance	$C_{RSS}$			95	110	pF
<b>SWITCHING PARAMETERS</b>						
Turn-ON Delay Time	$t_{D(ON)}$	$V_{DD}=30\text{V}$ , $I_D=0.5\text{A}$ , $R_G=25\Omega$ (Note 4,5)		90		ns
Turn-ON Rise Time	$t_R$			56		ns
Turn-OFF Delay Time	$t_{D(OFF)}$			138		ns
Turn-OFF Fall Time	$t_F$			34		ns
<b>SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS</b>						
Maximum Body-Diode Continuous Current	$I_S$				7	A
Maximum Body-Diode Pulsed Current	$I_{SM}$				28	A
Drain-Source Diode Forward Voltage	$V_{SD}$	$I_S=7.0\text{A}$ , $V_{GS}=0\text{V}$			1.4	V

Notes: 1. Pulse Test : Pulse width  $\leq 300\mu\text{s}$ , Duty cycle  $\leq 2\%$

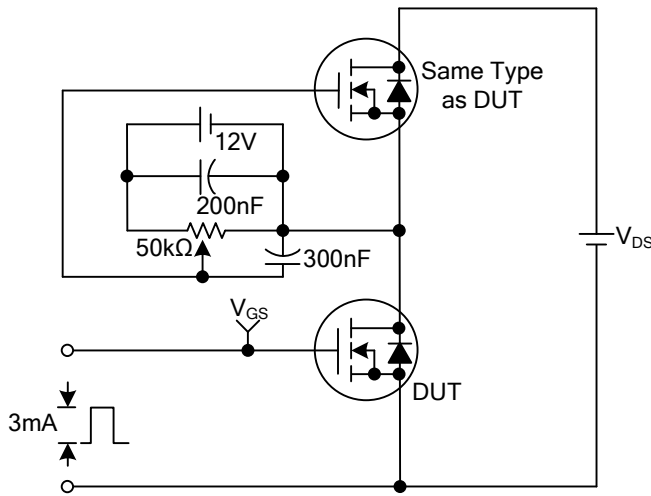
2. Essentially independent of operating temperature

■ TEST CIRCUITS AND WAVEFORMS

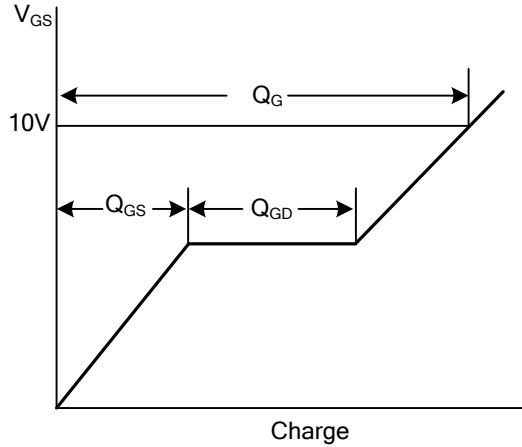
Peak Diode Recovery dv/dt Test Circuit & Waveforms



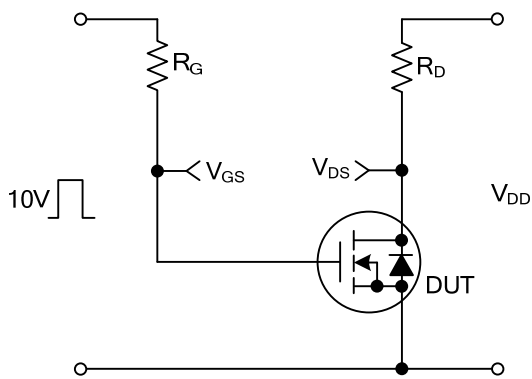
■ TEST CIRCUITS AND WAVEFORMS(Cont.)



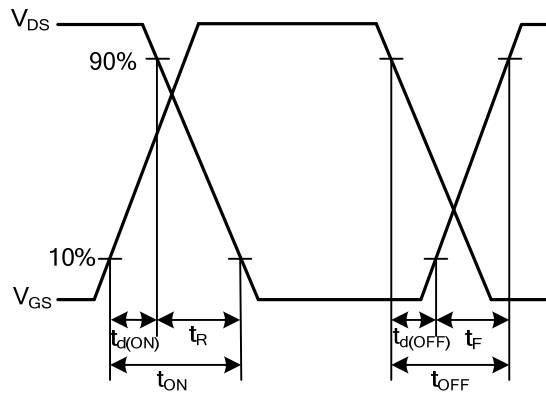
Gate Charge Test Circuit



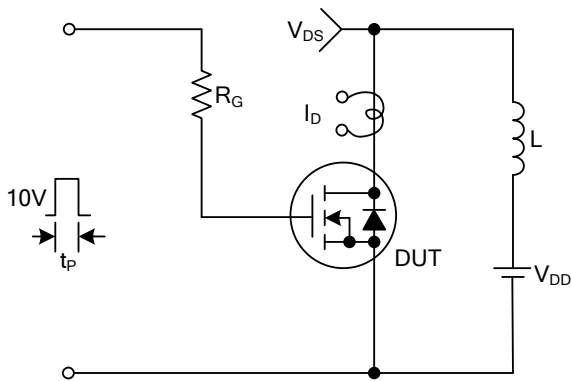
Gate Charge Waveforms



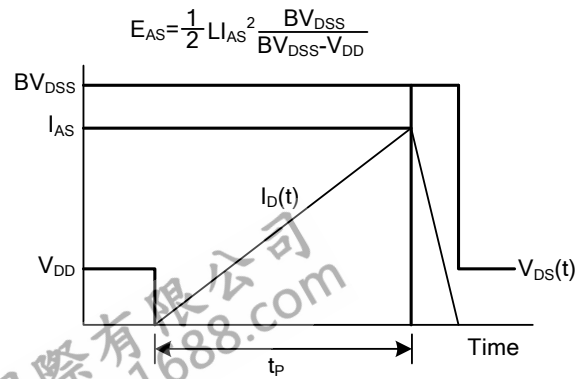
Resistive Switching Test Circuit



Resistive Switching Waveforms



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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