80N08-S **Power MOSFET**

80A, 80V N-CHANNEL **POWER MOSFET**

DESCRIPTION

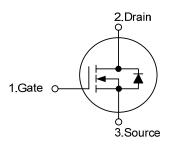
The UTC 80N08-S is a N-channel MOSFET using UTC advanced technology.

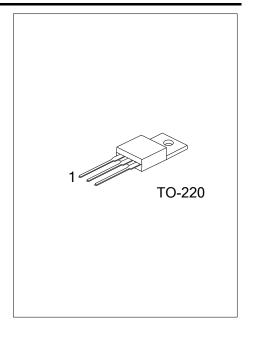
The UTC 80N08-S is suitable for power supply (secondary synchronous rectification), industrial and primary switch etc.



* $R_{DS(on)}$ < 18 m Ω @ V_{GS} =10V, I_{D} =40A

SYMBOL

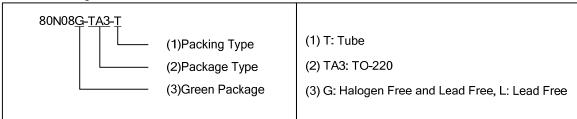




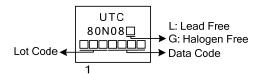
ORDERING INFORMATION

Ordering Number		Doolsons	Pin Assignment			Daakina	
Lead Free	Halogen Free	Package	1	2	3	Packing	
80N08L-TA3-T	80N08G-TA3-T	TO-220	G	D	S	Tube	

Note: Pin Assignment: G: Gate D: Drain S: Source



MARKING



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ABSOLUTE MAXIMUM RATINGS (T_C=25°C, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT	
Drain-Source Voltage		V_{DSS}	80	V	
Gate-Source Voltage		V_{GSS}	±20	V	
Continuous Drain Current	Continuous	Ι _D	80	Α	
Pulsed Drain Current	Pulsed (Note 2)	I_{DM}	320	Α	
Avalanche Current (Note 3)		I _{AR}	91	Α	
Avalanche energy	Single Pulsed (Note 3)	E _{AS}	414	mJ	
Peak Diode Recovery dv/dt (Note 4)		dv/dt	15	V/nS	
Power Dissipation		P_D	200	W	
Junction Temperature		T_J	+150	°C	
Storage Temperature Range		T _{STG}	-55 ~ +150	°C	

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

- 2. Repetitive Rating: Pulse width limited by maximum junction temperature.
- 3. L=0.1mH, I_{AS} =91A, V_{DD} =50V, R_{G} =25 Ω , Starting T_{J} = 25 $^{\circ}$ C.
- 4. $I_{SD} \leq 30A$, $di/dt \leq 200A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J = 25$ °C.

THERMAL DATA

PARAMETER	SYMBOL	MAX	UNIT	
Junction to Ambient	θ_{JA}	62	°C/W	
Junction to Case	θ_{JC}	0.75	°C/W	

ELECTRICAL CHARACTERISTICS (T_J =25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT		
OFF CHARACTERISTICS								
Drain-Source Breakdown Voltage	BV _{DSS}	I _D =1mA, V _{GS} =0V	80			V		
Drain-Source Leakage Current	I _{DSS}	V _{DS} =80V, V _{GS} =0V, T _J =25°C			1	μΑ		
Gate-Source Leakage Current	I_{GSS}	V_{DS} =0V, V_{GS} =±20V			±100	nA		
ON CHARACTERISTICS								
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}$, $I_D=250\mu A$	1.0		3.0	V		
Static Drain-Source On-State Resistance	R _{DS(ON)}	V_{GS} =10V, I_D =40A			18	mΩ		
DYNAMIC PARAMETERS								
Input Capacitance	C _{ISS}			3550		pF		
Output Capacitance	Coss	V_{GS} =0V, V_{DS} =25V, f=1.0MHz		463		pF		
Reverse Transfer Capacitance	C_{RSS}			36		pF		
SWITCHING PARAMETERS								
Total Gate Charge (Note 1)	Q_G	V _{DS} =50V, I _D =1.3A, V _{GS} =10V		223		nC		
Gate to Source Charge	Q_GS	V _{DS} =50V, I _D =1.3A, V _{GS} =10V I _G =100μA (Note1, 2)		15		nC		
Gate to Drain Charge	Q_GD	IG-100μΑ (Note1, 2)		19.2		nC		
Turn-ON Delay Time (Note 1)	t _{D(ON)}			70		ns		
Rise Time	t_R	V_{DD} =30V, I_{D} =0.5A, R_{G} =25 Ω ,		73		ns		
Turn-OFF Delay Time	t _{D(OFF)}	V _{GS} =0V (Note1, 2)		1085		ns		
Fall-Time	t_{F}			205		ns		
SOURCE- DRAIN DIODE RATINGS AND CHA	ARACTERIS	TICS						
Maximum Body-Diode Continuous Current	I_S	~ 2			80	Α		
Maximum Body-Diode Pulsed Current	I _{SM}	10.10	3		320	^		
Drain-Source Diode Forward Voltage (Note 1)	V_{SD}	I _S =30A, V _{GS} =0V			1.3	V		
Body Diode Reverse Recovery Time (Note 1)	t _{rr}	I _S =30A, V _{GS} =0V		63.6		ns		
Body Diode Reverse Recovery Charge	Q _{rr}	df _F /dt=100A/µs		164		nC		

Note: 1. Pulse Test: Pulse width ≤ 300µs, Duty cycle ≤ 2%

2. Essentially independent of operating temperature.

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■ TEST CIRCUITS AND WAVEFORMS

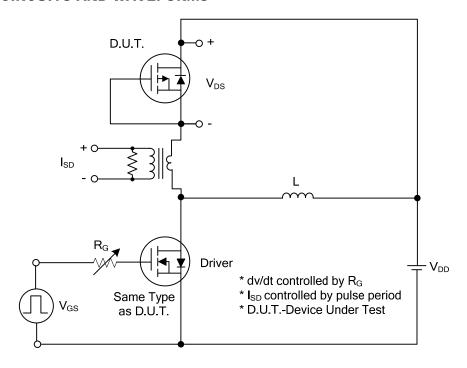


Fig. 1A Peak Diode Recovery dv/dt Test Circuit

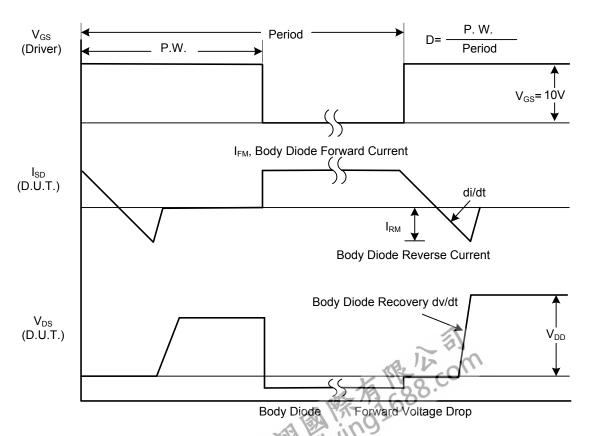
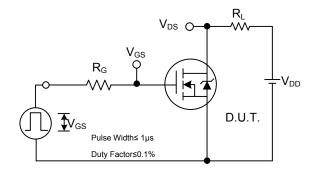


Fig. 1B Peak Diode Recovery dv/dt Waveforms

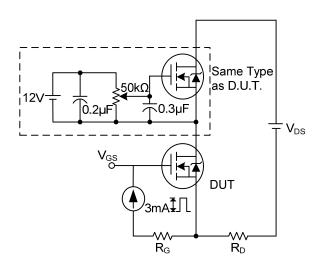
TEST CIRCUITS AND WAVEFORMS (Cont.)

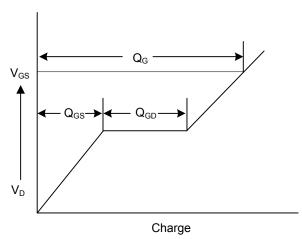


 V_{DS} 90% 10%

2A Switching Test Circuit

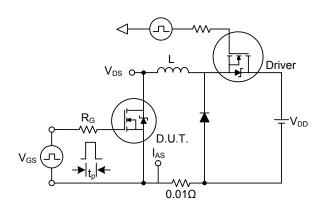
2B Switching Waveforms

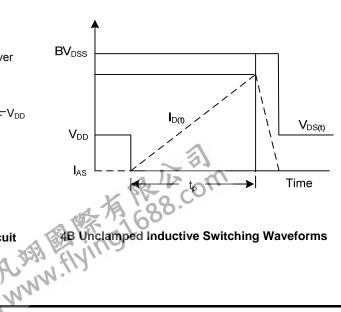




3A Gate Charge Test Circuit

3B Gate Charge Waveform





4A Unclamped Inductive Switching Test Circuit

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