

# **Power MOSFET**

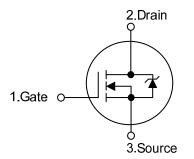
# 8A, 500V N-CHANNEL POWER MOSFET

### DESCRIPTION

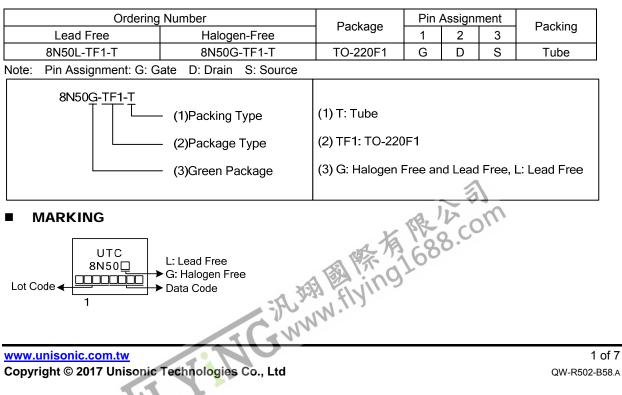
The N-Channel enhancement mode silicon gate power MOSFET is designed for high voltage, high speed power switching applications such as switching regulators, switching converters, solenoid, motor drivers, relay drivers.

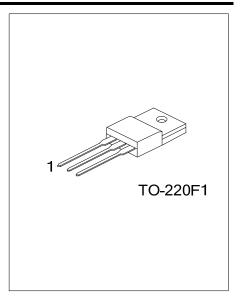
### FEATURES

- \* Low R\_{DS(ON)}< 0.87 \Omega @ V\_{GS}=10V. I\_D = 4.4 A
- \* Single Pulse Avalanche Energy Rated
- \* Fast Switching Speeds
- \* Linear Transfer Characteristics
- \* High Input Impedance
- SYMBOL



### ORDERING INFORMATION





### ■ **ABSOLUTE MAXIMUM RATINGS** (T<sub>c</sub> = 25°C, unless Otherwise Specified)

PARAMETE	R	SYMBOL	RATINGS	UNIT
Drain to Source Voltage (T <sub>J</sub> =25°C ~125°C)		V <sub>DSS</sub>	500	V
Drain to Gate Voltage (R <sub>GS</sub> = 20kΩ, T <sub>J</sub> =25°C ~125°C)		V <sub>DGR</sub>	500	V
Gate to Source Voltage		V <sub>GSS</sub>	±30	V
Drain Current (Note 2)	Continuous	I <sub>D</sub>	8.0	А
	Pulsed	I <sub>DM</sub>	32	А
Single Pulse Avalanche Energy (Note 3)		E <sub>AS</sub>	336	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	3.3	V/ns
Power Dissipation		PD	44	W
Junction Temperature		TJ	+150	°C
Storage Temperature		T <sub>STG</sub>	-55 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. L = 10mH,  $I_{AS}$  = 8.0A,  $V_{DD}$  = 50V,  $R_{G}$  = 25 $\Omega$ , Starting  $T_{J}$  = 25°C.

4.  $I_{SD} \le 8.0A$ , di/dt  $\le 200A/\mu s$ ,  $V_{DD} \le BV_{DSS}$ , Starting  $T_J = 25^{\circ}C$ .

### THERMAL DATA

PARAMETER	SYMBOL	RATING	UNIT	
Junction to Ambient	$\theta_{JA}$	62.5	°C/W	
Junction to Case	θ <sub>JC</sub>	2.7	°C/W	

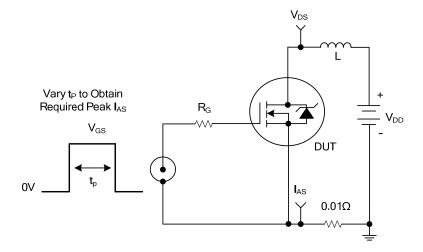
#### ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C, unless otherwise specified)

h							
PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV <sub>DSS</sub>	I <sub>D</sub> = 250μA, V <sub>GS</sub> = 0V	500			V
Drain-Source Leakage Current		I <sub>DSS</sub>	V <sub>DS</sub> =Rated BV <sub>DSS</sub> , V <sub>GS</sub> = 0V			25	μA
Gate-Source Leakage Current	Forward	- I <sub>GSS</sub>	V <sub>GS</sub> =+30V, V <sub>DS</sub> =0V			+100	nA
	Reverse		V <sub>GS</sub> =-30V, V <sub>DS</sub> =0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		V <sub>GS(TH)</sub>	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> = 250μA	2.0		4.0	V
Static Drain-Source On-State Resistance		R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V. I <sub>D</sub> =4.4A			0.87	Ω
DYNAMIC PARAMETERS							
Input Capacitance		CISS			920		pF
Output Capacitance Reverse Transfer Capacitance		Coss	V <sub>GS</sub> =0V, V <sub>DS</sub> =25V, f=1.0MHz		105		pF
					10		pF
SWITCHING PARAMETERS							
Total Gate Charge (Note 1)		$Q_{G}$	V <sub>DS</sub> =400V, V <sub>GS</sub> =10V, I <sub>D</sub> =8A, I <sub>G</sub> =10mA (Note 1, 2)		24		nC
Gate to Source Charge		$Q_{GS}$			3		nC
Gate to Drain Charge		$Q_{GD}$	$I_G$ = IOITIA (Note 1, 2)		2		nC
Turn-on Delay Time (Note 1)		t <sub>D(ON)</sub>			4.8		ns
Rise Time		t <sub>R</sub>	V <sub>DS</sub> =250V, V <sub>GS</sub> =10V, I <sub>D</sub> =8A,		11.6		ns
Turn-off Delay Time		t <sub>D(OFF)</sub>	R <sub>G</sub> =25Ω (Note 1, 2)		56		ns
Fall-Time		t <sub>F</sub>			20		ns
SOURCE- DRAIN DIODE RATIN	IGS AND CH	ARACTERIS	TICS	3			
Maximum Body-Diode Continuous Current		ls	AR CO	1.		8	Α
Maximum Body-Diode Pulsed Current		I <sub>SM</sub>	1 18 000.			32	Α
Drain-Source Diode Forward Voltage (Note 1)		$V_{SD}$	I <sub>8</sub> =8.0A, V <sub>GS</sub> =0V			2	V
Reverse Recovery Time (Note 1)		t <sub>rr</sub>	I <sub>S</sub> =8.0A, V <sub>GS</sub> =0∨,		312		nS
Reverse Recovery Charge		Qrr	dl <sub>⊭</sub> /dt=100A/µs		3.1		μC
Notes: 1 Pulse Test: Pulse width		v cvcle<2%	N				

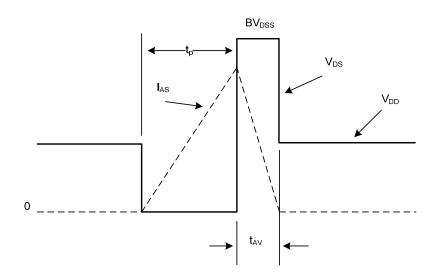
Notes: 1. Pulse Test: Pulse width  $\leq$  300µs, Duty cycle $\leq$ 2%.

2. Essentially independent of operating temperature.

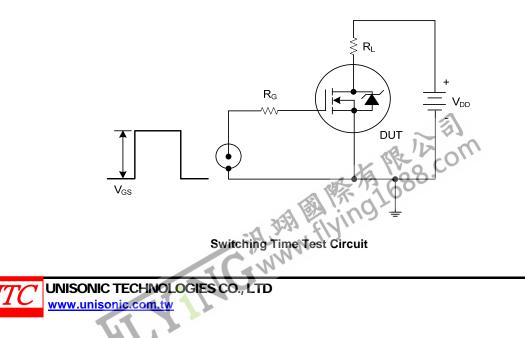
## TEST CIRCUITS AND WAVEFORMS



#### **Unclamped Energy Test Circuit**



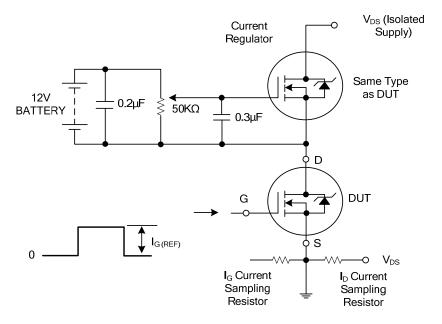
#### **Unclamped Energy Waveforms**



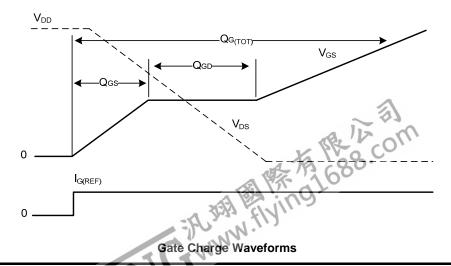
## ■ TEST CIRCUITS AND WAVEFORMS (Cont.)

 $\mathbf{t}_{\text{ON}}$  $t_{OFF}$  $t_{\text{DLY}(\text{ON})}$ t<sub>DLY(OFF)</sub> t<sub>R</sub> te  $V_{\text{DS}}$ 90% 90% 10% 10% 0 ..... 90%  $V_{GS}$ 50% 50% 0 \_\_\_\_\_ PULSE WIDTH

**Resistive Switching Waveforms** 

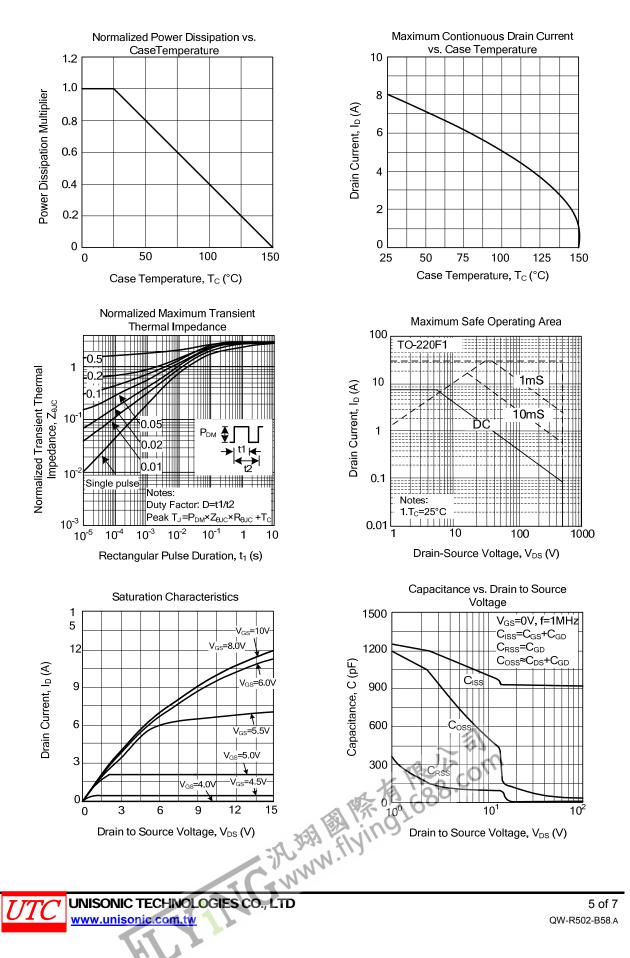


**Gate Charge Test Circuit** 

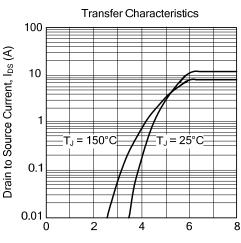


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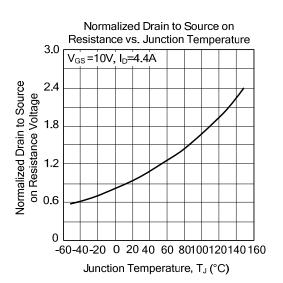
### TYPICAL CHARACTERISTICS



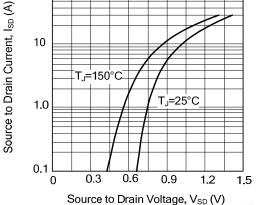
# **TYPICAL CHARACTERISTICS (Cont.)**

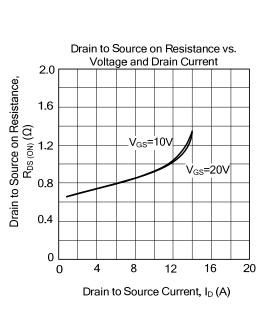


Gate to Source Voltage, V<sub>GS</sub> (V)

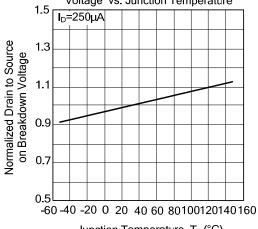


Source to Drain DIODE Voltage 100 10 T\_=150°C

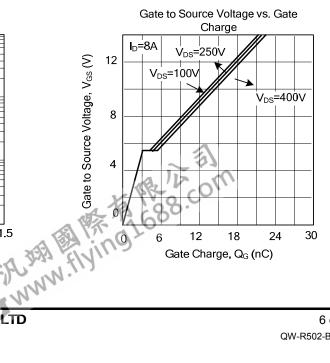




Normalized Drain to Source Breakdown Voltage vs. Junction Temperature



Junction Temperature, T<sub>J</sub> (°C)



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