

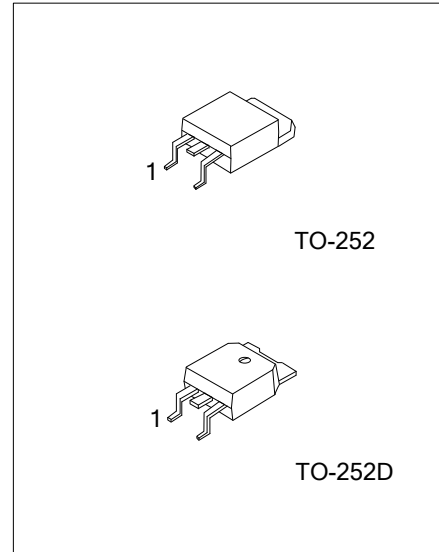


9A, 650V N-CHANNEL POWER MOSFET

DESCRIPTION

The UTC 9N65-TC2 is an N-channel mode power MOSFET using UTC's advanced technology to provide costumers with planar stripe and DMOS technology. This technology is specialized in allowing a minimum on-state resistance and superior switching performance. It also can withstand high energy pulse in the avalanche and commutation mode.

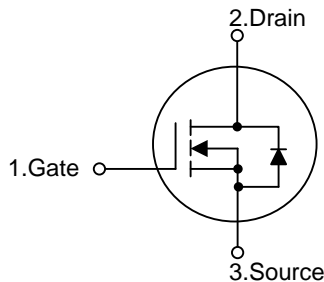
The UTC 9N65-TC2 is universally applied in active power factor correction and high efficient switched mode power supplies.



FEATURES

- * $R_{DS(ON)} \leq 1.3 \Omega @ V_{GS}=10V, I_D=4.5A$
- * High switching speed
- * Improved dv/dt capability

SYMBOL



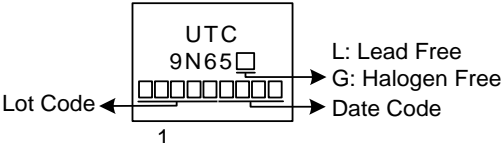
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
9N65L-TN3-R	9N65G-TN3-R	TO-252	G	D	S	Tape Reel
9N65L-TND-R	9N65G-TND-R	TO-252D	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>9N65G-TN3-R</p> <p>(1)Packing Type</p> <p>(2)Package Type</p> <p>(3)Green Package</p>	<p>(1) R: Tape Reel</p> <p>(2) TN3: TO-252, TND: TO-252D</p> <p>(3) G: Halogen Free and Lead Free, L: Lead Free</p>
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MARKING



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■ **ABSOLUTE MAXIMUM RATINGS** ($T_C=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Drain to Source Voltage	V_{DSS}	650	V
Gate to Source Voltage	V_{GSS}	± 30	V
Continuous Drain Current	Continuous	I_D	9
	Pulsed (Note 2)	I_{DM}	18
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	240
Peak Diode Recovery dv/dt (Note 3)	dv/dt	4.5	V/ns
Power Dissipation	P_D	55	W
Junction Temperature	T_J	+150	$^{\circ}\text{C}$
Storage Temperature	T_{STG}	-55 ~ +150	$^{\circ}\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating : Pulse width limited by maximum junction temperature.

3. $L = 30\text{mH}$, $I_{AS} = 4.0\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 25\ \Omega$, Starting $T_J = 25^{\circ}\text{C}$

4. $I_{SD} \leq 9.0\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^{\circ}\text{C}$.

■ **THERMAL DATA**

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	110	$^{\circ}\text{C}/\text{W}$
Junction to Case	θ_{JC}	2.27 (Note)	$^{\circ}\text{C}/\text{W}$

Note: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

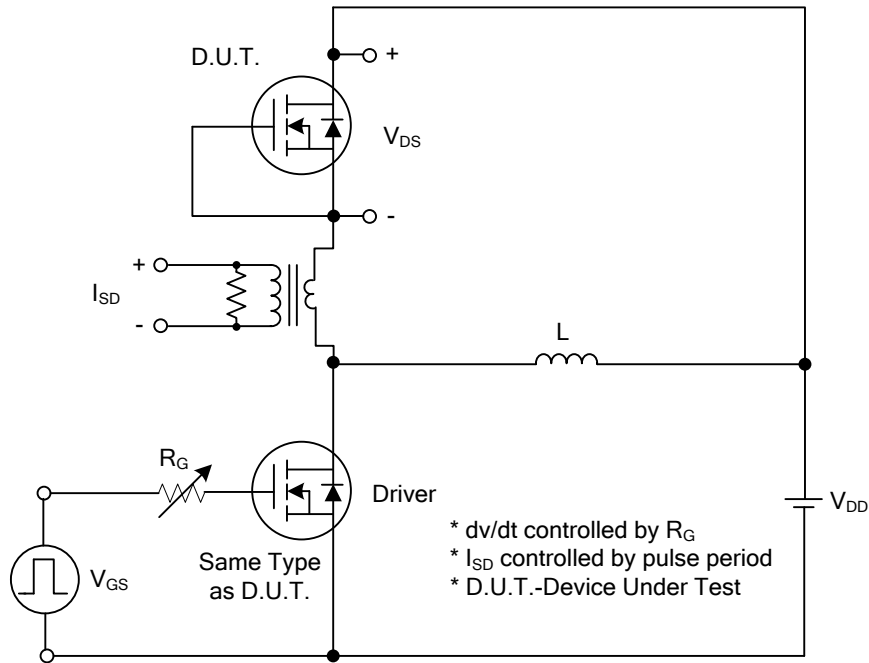
■ **ELECTRICAL CHARACTERISTICS** ($T_J = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	650			V
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=650V, V_{GS}=0V$			10	μA
Gate- Source Leakage Current	Forward	I_{GSS}			+100	nA
	Reverse					
		$V_{GS}=-30V, V_{DS}=0V$			-100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2.0		4.0	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=4.5A$			1.3	Ω
DYNAMIC CHARACTERISTICS						
Input Capacitance	C_{ISS}	$V_{DS}=25V, V_{GS}=0V, f=1\text{MHz}$		1150		pF
Output Capacitance	C_{OSS}			110		pF
Reverse Transfer Capacitance	C_{RSS}			4.8		pF
DYNAMIC CHARACTERISTICS						
Total Gate Charge	Q_G	$V_{DS}=520V, V_{GS}=10V, I_D=9A$ $I_G=1\text{mA}$ (Note 1, 2)		25		nC
Gate-Source Charge	Q_{GS}			6.5		nC
Gate-Drain Charge	Q_{GD}			4.2		nC
Turn-on Delay Time (Note 1)	$t_{D(ON)}$	$V_{DS}=100V, V_{GS}=10V, I_D=9A,$ $R_G=25\Omega$ (Note 1, 2)		13.5		ns
Rise Time	t_R			18		ns
Turn-off Delay Time	$t_{D(OFF)}$			78		ns
Fall-Time	t_F			36		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Continuous Drain-Source Diode Forward Current	I_S				9	A
Maximum Pulsed Drain-Source Diode Forward Current	I_{SM}				18	A
Drain-Source Diode Forward Voltage (Note 1)	V_{SD}	$I_S=9A, V_{GS}=0V$			1.4	V
Body Diode Reverse Recovery Time (Note 1)	t_{rr}	$I_S=9A, V_{GS}=0V,$ $di_F/dt=100A/\mu s$		470		nS
Body Diode Reverse Recovery Charge	Q_{rr}			9.5		μC

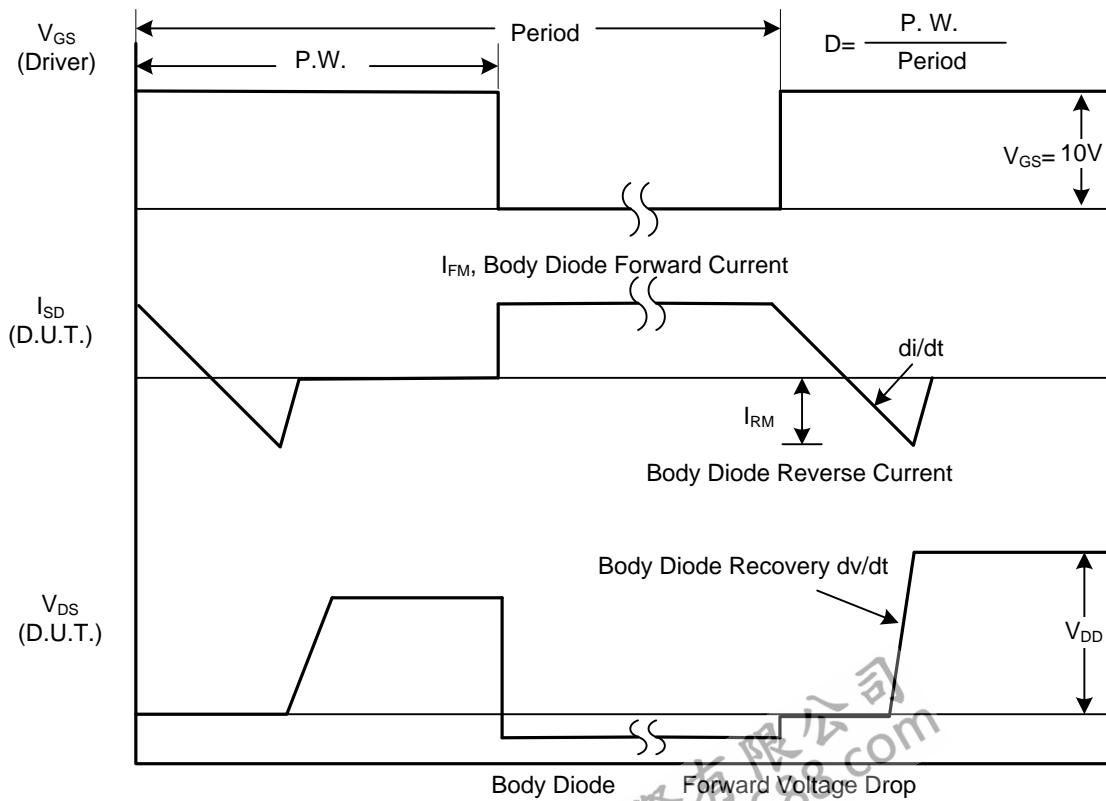
Notes: 1. Pulse Test : Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

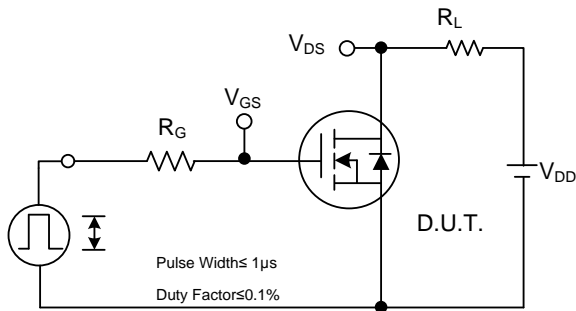


Peak Diode Recovery dv/dt Test Circuit

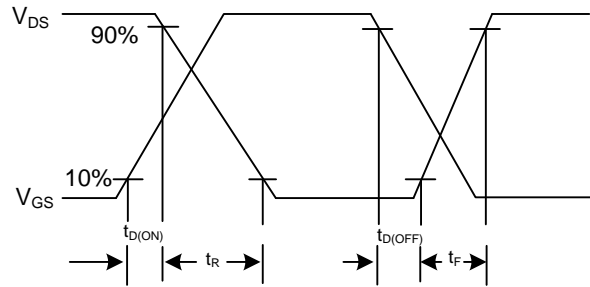


Peak Diode Recovery dv/dt Waveforms

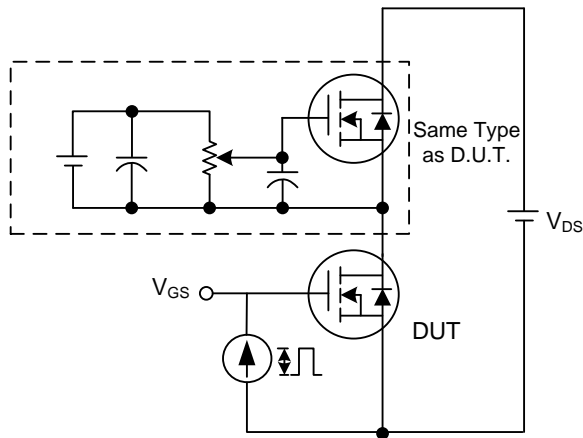
TEST CIRCUITS AND WAVEFORMS



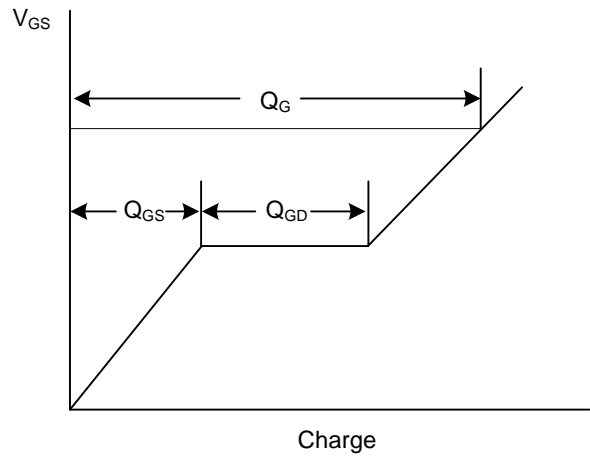
Switching Test Circuit



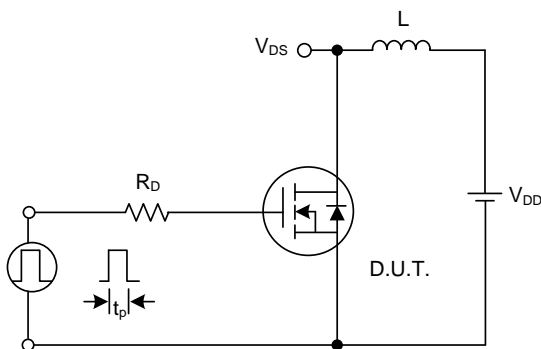
Switching Waveforms



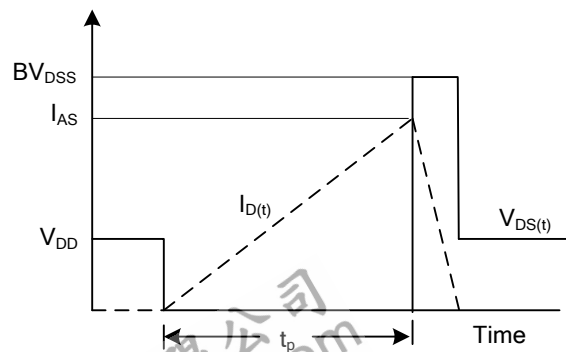
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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