



## 9NM60-FD

Power MOSFET

### 9A, 600V N-CHANNEL SUPER-JUNCTION MOSFET

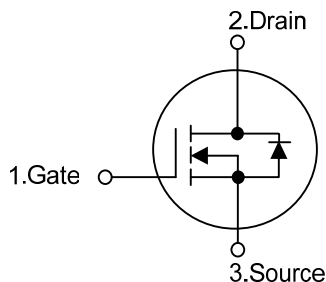
#### DESCRIPTION

The **UTC 9NM60-FD** is a Super Junction MOSFET Structure and is designed to have better characteristics, such as fast switching time, low gate charge, low on-state resistance and a high rugged avalanche characteristics. This power MOSFET is usually used at DC-DC, AC-DC converters for power applications.

#### FEATURES

- \*  $R_{DS(ON)} \leq 0.58\Omega$  @  $V_{GS}=10V$ ,  $I_D=4.5A$
- \* Fast Switching Capability
- \* Avalanche Energy Tested
- \* Improved  $dv/dt$  Capability, High Ruggedness

#### SYMBOL



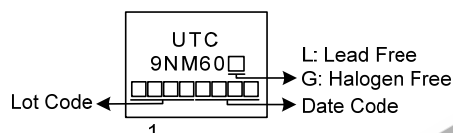
#### ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
9NM60L-TN3-R	9NM60G-TN3-R	TO-252	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

	(1) R: Tape Reel (2) TN3: TO-252 (3) G: Halogen Free and Lead Free, L: Lead Free
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#### MARKING



■ ABSOLUTE MAXIMUM RATINGS ( $T_C = 25^\circ\text{C}$ , unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		$V_{DSS}$	600	V
Gate-Source Voltage		$V_{GSS}$	$\pm 30$	V
Drain Current	Continuous	$I_D$	9	A
	Pulsed (Note 2)	$I_{DM}$	18	A
Avalanche Energy	Single Pulsed (Note 3)	$E_{AS}$	48	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	12.7	V/ns
Power Dissipation		$P_D$	60	W
Junction Temperature		$T_J$	+150	$^\circ\text{C}$
Storage Temperature		$T_{STG}$	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3.  $L=10\text{mH}$ ,  $I_{AS}=3.1\text{A}$ ,  $V_{DD}=50\text{V}$ ,  $R_G=25\ \Omega$ , Starting  $T_J = 25^\circ\text{C}$

4.  $I_{SD}\leq 8.0\text{A}$ ,  $di/dt\leq 200\text{A}/\mu\text{s}$ ,  $V_{DD}\leq BV_{DSS}$ , Starting  $T_J = 25^\circ\text{C}$

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	$\theta_{JA}$	110	$^\circ\text{C}/\text{W}$
Junction to Case	$\theta_{JC}$	2.08 (Note)	$^\circ\text{C}/\text{W}$

Note: Device mounted on FR-4 substrate  $P_C$  board, 2oz copper, with 1inch square copper plate.

■ ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ , unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV <sub>DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA	600			V
Drain-Source Leakage Current		I <sub>DSS</sub>	V <sub>DS</sub> = 600V, V <sub>GS</sub> = 0V			10	μA
Gate- Source Leakage Current	Forward	I <sub>GSS</sub>	V <sub>GS</sub> = 30V, V <sub>DS</sub> = 0V			100	nA
	Reverse		V <sub>GS</sub> = -30V, V <sub>DS</sub> = 0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		V <sub>GS(TH)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	2.5		4.5	V
Static Drain-Source On-State Resistance		R <sub>DS(ON)</sub>	V <sub>GS</sub> = 10V, I <sub>D</sub> = 4.0A			0.58	Ω
DYNAMIC CHARACTERISTICS							
Input Capacitance		C <sub>ISS</sub>	V <sub>GS</sub> =0V, V <sub>DS</sub> =25V, f=1.0 MHz		580		pF
Output Capacitance		C <sub>OSS</sub>			460		pF
Reverse Transfer Capacitance		C <sub>RSS</sub>			52		pF
SWITCHING CHARACTERISTICS							
Total Gate Charge (Note 1)		Q <sub>G</sub>	V <sub>DS</sub> =100V, V <sub>GS</sub> =10V, I <sub>D</sub> =9.0A, I <sub>G</sub> =1mA (Note 1, 2)		31		nC
Gate to Source Charge		Q <sub>GS</sub>			5.5		nC
Gate to Drain Charge		Q <sub>GD</sub>			8.2		nC
Turn-ON Delay Time (Note 1)		t <sub>D(ON)</sub>	V <sub>DD</sub> =100V, V <sub>GS</sub> =10V, I <sub>D</sub> =9.0A, R <sub>G</sub> =25Ω (Note 1, 2)		9		ns
Rise Time		t <sub>R</sub>			25.5		ns
Turn-OFF Delay Time		t <sub>D(OFF)</sub>			76		ns
Fall-Time		t <sub>F</sub>			46.5		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Continuous Drain-Source Diode Forward Current		I <sub>S</sub>				9	A
Maximum Pulsed Drain-Source Diode Forward Current		I <sub>SM</sub>				18	A
Drain-Source Diode Forward Voltage (Note 1)		V <sub>SD</sub>	I <sub>S</sub> =9.0A, V <sub>GS</sub> =0V			1.4	V
Body Diode Reverse Recovery Time (Note 1)		t <sub>rr</sub>	I <sub>S</sub> =9.0A, V <sub>GS</sub> =0V,		155		ns
Body Diode Reverse Recovery Charge		Q <sub>rr</sub>	dl <sub>F</sub> /dt=100A/μs		0.95		μC

Notes: 1. Pulse Test: Pulse width  $\leq 300\mu s$ , Duty cycle  $\leq 2\%$ .

2. Essentially independent of operating temperature.

[illegible]

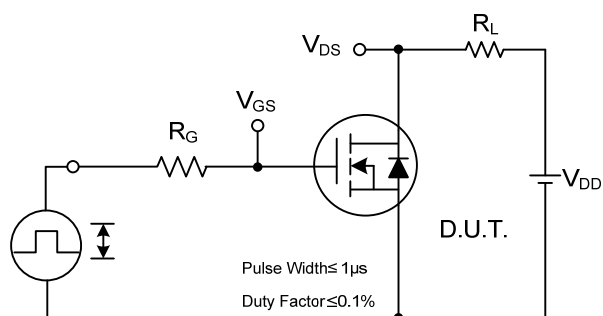
Timing diagram for a MOSFET switching a load inductor. The diagram shows three waveforms:

- $V_{GS}$  (Driver):** A square wave with pulse width (P.W.) and period. The duty cycle is given by  $D = \frac{\text{P. W.}}{\text{Period}}$ . The peak voltage is  $V_{GS} = 10V$ .
- $I_{SD}$  (D.U.T.):** The source-drain current. It shows forward current  $I_{FM}$  (Body Diode Forward Current) during the pulse and reverse current  $I_{RM}$  (Body Diode Reverse Current) during the fall time. The rate of change of current is labeled  $di/dt$ .
- $V_{DS}$  (D.U.T.):** The drain-source voltage. It shows the switching transient, including the Body Diode Recovery  $dv/dt$  phase. The peak voltage is  $V_{DD}$ .

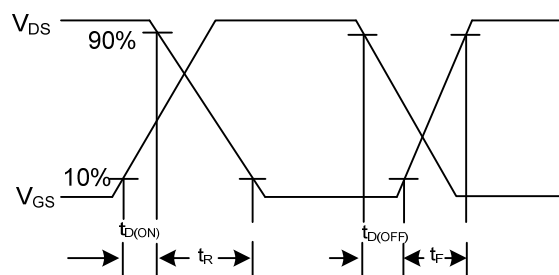
Additional labels include "Body Diode Forward Voltage Drop" and "Body Diode Recovery". A watermark "www.electronicshub.com" is visible across the diagram.

### Peak Diode Recovery dv/dt Waveforms

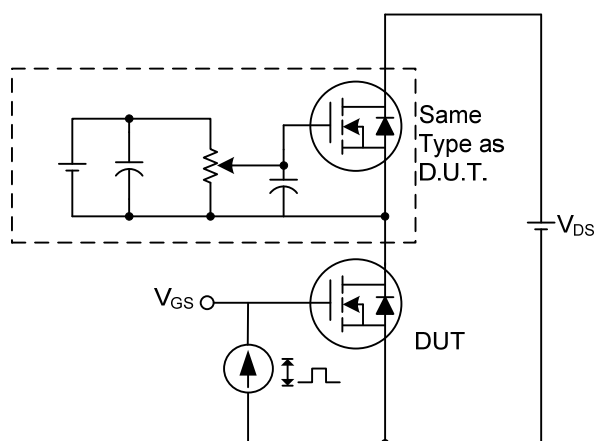
## ■ TEST CIRCUITS AND WAVEFORMS (Cont.)



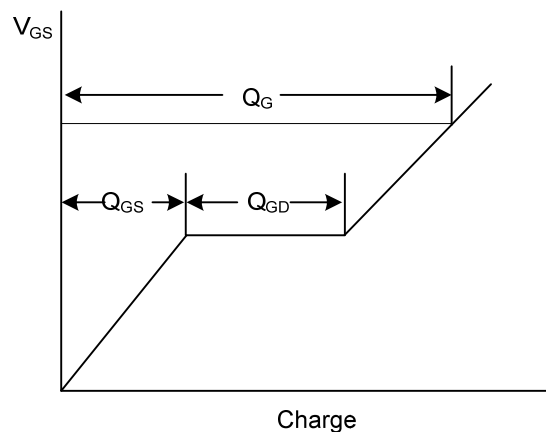
Switching Test Circuit



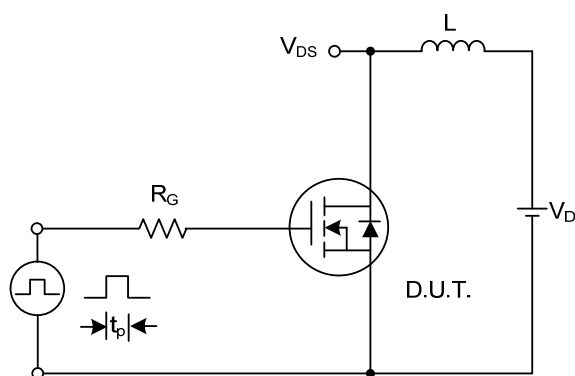
Switching Waveforms



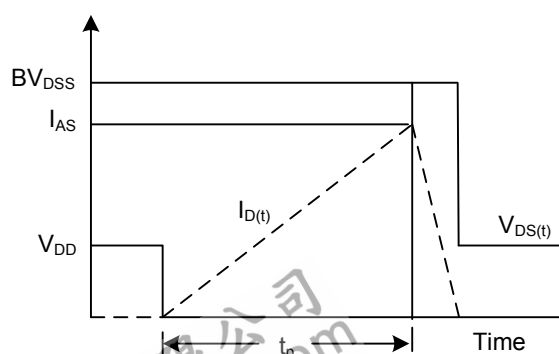
Gate Charge Test Circuit



Gate Charge Waveform

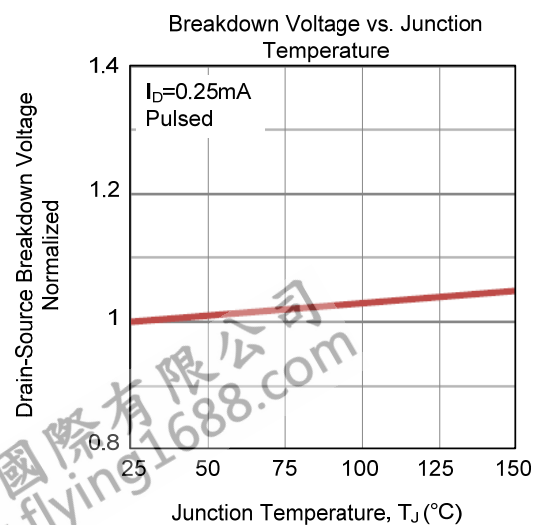
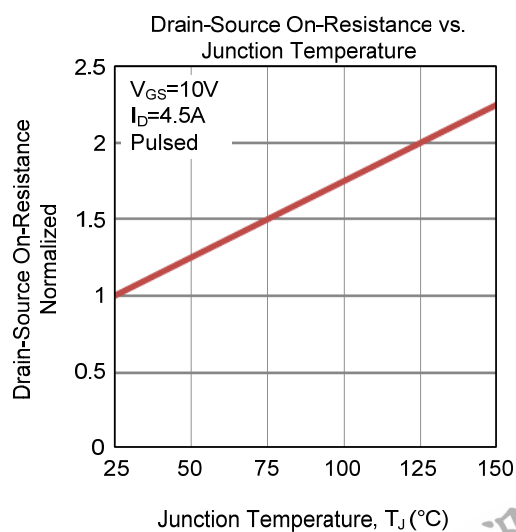
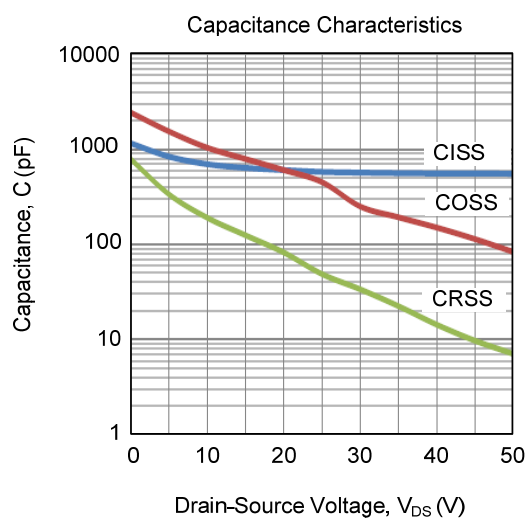
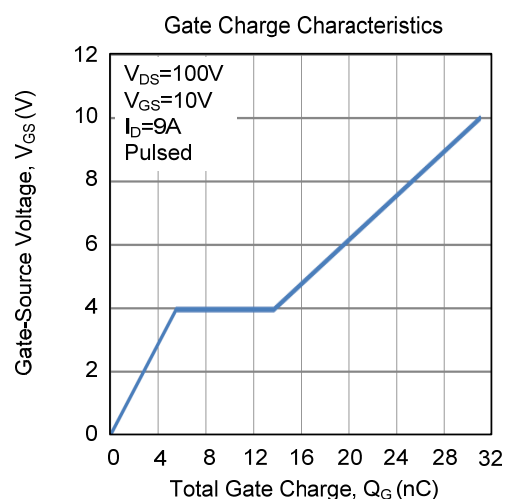
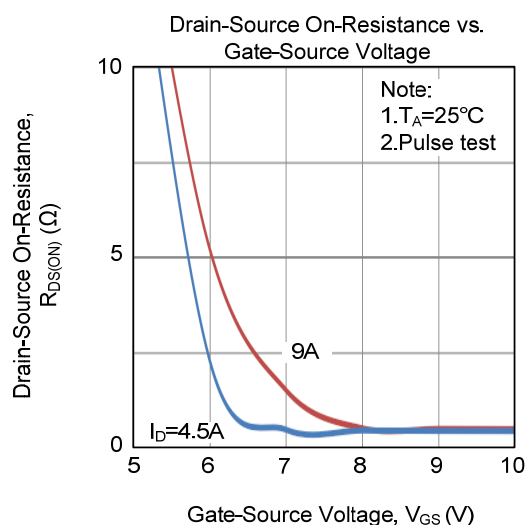
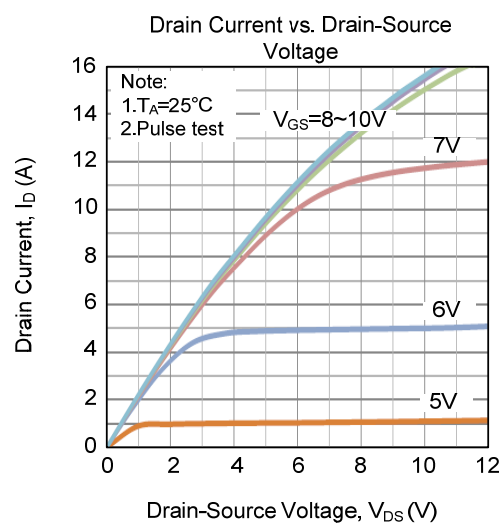


Unclamped Inductive Switching Test Circuit

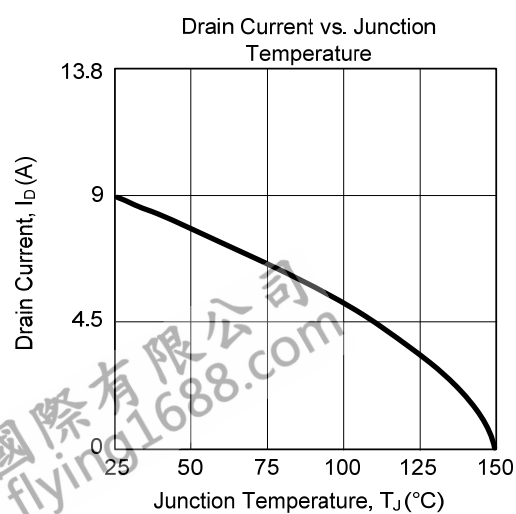
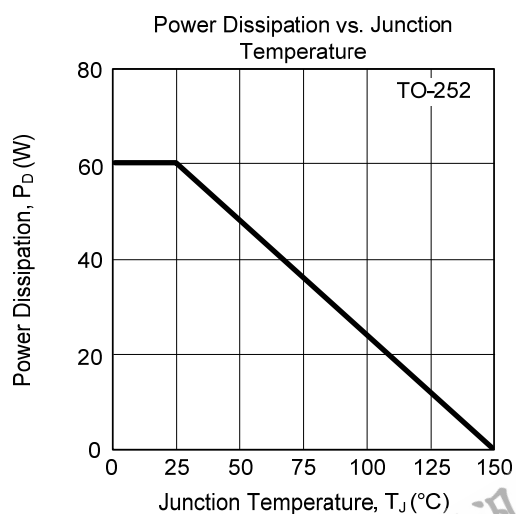
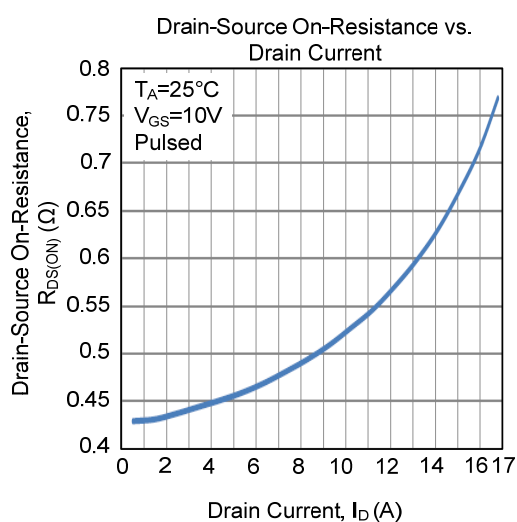
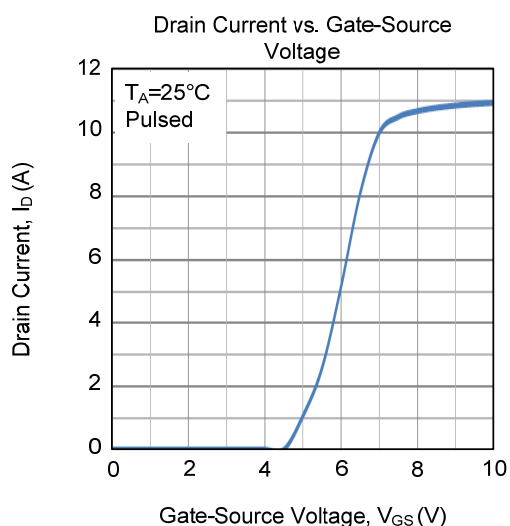
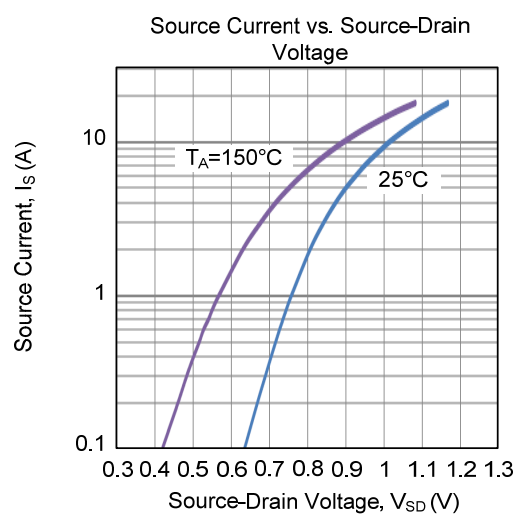
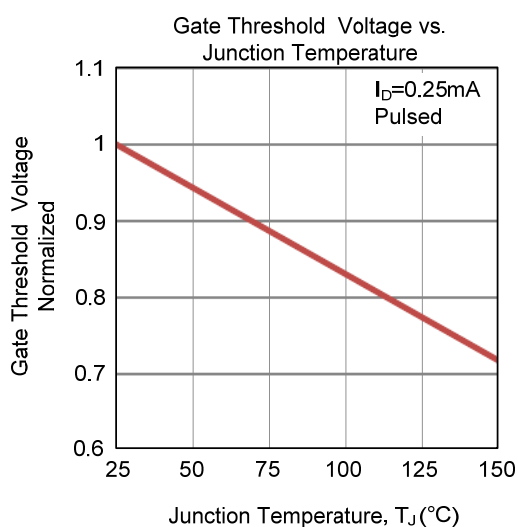


Unclamped Inductive Switching Waveforms

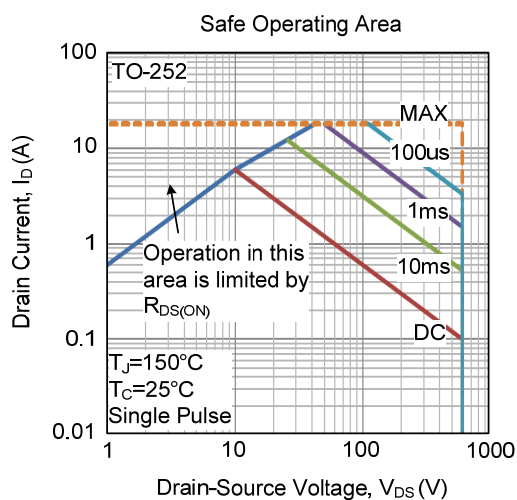
# TYPICAL CHARACTERISTICS



## ■ TYPICAL CHARACTERISTICS (Cont.)



# ■ TYPICAL CHARACTERISTICS (Cont.)



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