



9NM65-VS

Power MOSFET

9A, 650V N-CHANNEL SUPER-JUNCTION MOSFET

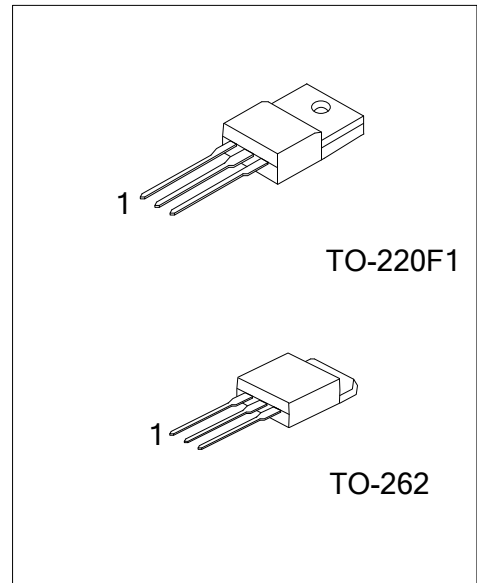
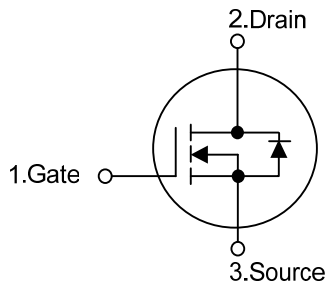
DESCRIPTION

The **UTC 9NM65-VS** is a Super Junction MOSFET Structure and is designed to have better characteristics, such as fast switching time, low gate charge, low on-state resistance and a high rugged avalanche characteristics. This power MOSFET is usually used at DC-DC, AC-DC converters for power applications.

FEATURES

- * $R_{DS(ON)} < 0.62 \Omega @ V_{GS} = 10V, I_D = 4.5A$
- * Fast Switching Capability
- * Avalanche Energy Tested
- * Improved dv/dt Capability, High Ruggedness

SYMBOL



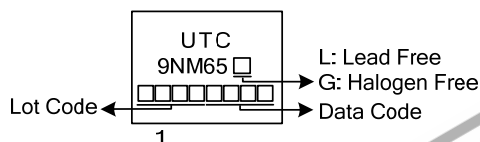
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen-Free		1	2	3	
9NM65L-TF1-T	9NM65G-TF1-T	TO-220F1	G	D	S	Tube
9NM65L-T2Q-T	9NM65G-T2Q-T	TO-262	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>9NM65G-TF1-T</p> <p>(1)Packing Type (2)Package Type (3)Green Package</p>	<p>(1) T: Tube (2) TF1: TO-220F1, T2Q: TO-262 (3) G: Halogen Free and Lead Free, L: Lead Free</p>
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MARKING



■ ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	650	V
Gate-Source Voltage		V_{GSS}	± 30	V
Drain Current	Continuous	I_D	9	A
	Pulsed (Note 2)	I_{DM}	20	A
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	157	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	4	V/ns
Power Dissipation	TO-220F1	P_D	28	W
	TO-262		83	W
Junction Temperature		T_J	+150	$^\circ\text{C}$
Storage Temperature		T_{STG}	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $L=65\text{mH}$, $I_{AS}=2.2\text{A}$, $V_{DD}=50\text{V}$, $R_G=25\ \Omega$, Starting $T_J = 25^\circ\text{C}$

4. $I_{SD}\leq 9.0\text{A}$, $di/dt\leq 200\text{A}/\mu\text{s}$, $V_{DD}\leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$

■ THERMAL DATA

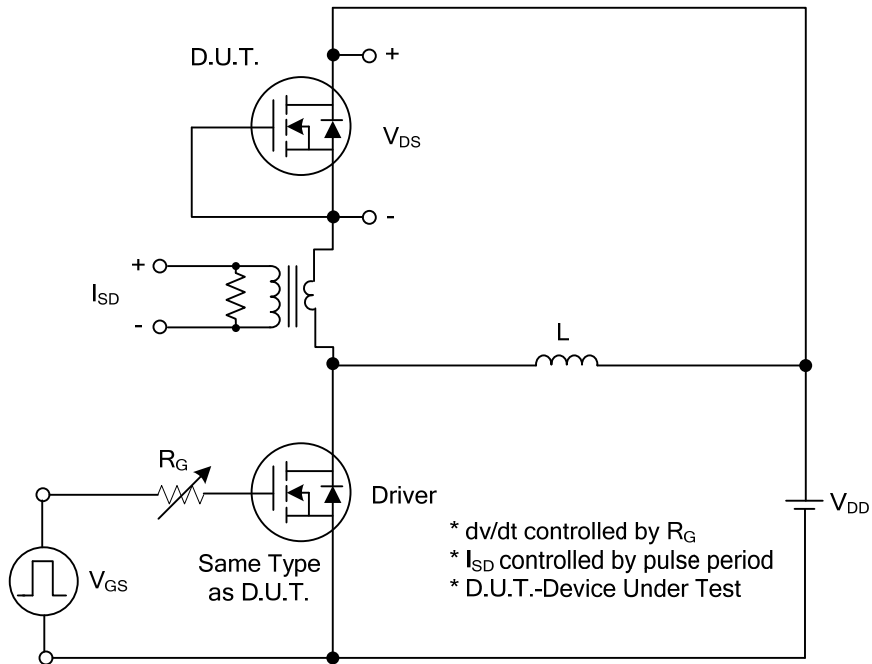
PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient		θ_{JA}	62.5	$^\circ\text{C}/\text{W}$
Junction to Case	TO-220F1	θ_{JC}	4.5	$^\circ\text{C}/\text{W}$
	TO-262		1.5	$^\circ\text{C}/\text{W}$

■ ELECTRICAL CHARACTERISTICS (T_J=25°C, unless otherwise specified)

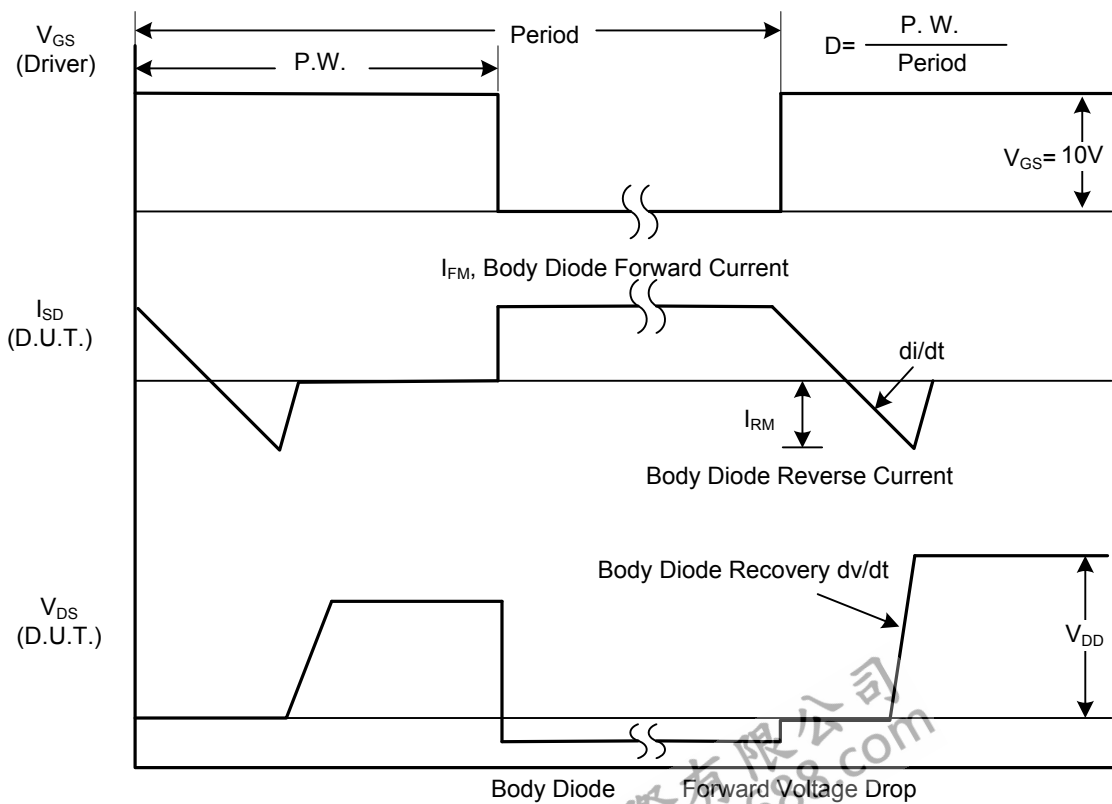
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D = 250μA	650			V
Drain-Source Leakage Current	I _{DSS}	V _{DS} = 650V, V _{GS} = 0V			10	μA
Gate- Source Leakage Current	Forward	V _{GS} = 30V, V _{DS} = 0V			100	nA
	Reverse		V _{GS} = -30V, V _{DS} = 0V			-100
ON CHARACTERISTICS						
Gate Threshold Voltage	V _{GS(TH)}	V _{DS} = V _{GS} , I _D = 250μA	2.0		4.0	V
Static Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} = 10V, I _D = 4.5A			0.62	Ω
DYNAMIC CHARACTERISTICS						
Input Capacitance	C _{ISS}	V _{GS} =0V, V _{DS} =25V, f=1.0 MHz		620		pF
Output Capacitance	C _{OSS}			480		pF
Reverse Transfer Capacitance	C _{RSS}			38		pF
SWITCHING CHARACTERISTICS						
Total Gate Charge (Note 1)	Q _G	V _{DS} =300V, V _{GS} =10V, I _D =1.5A, I _G =2mA (Note 1, 2)		26.2		nC
Gate to Source Charge	Q _{GS}			3.5		nC
Gate to Drain Charge	Q _{GD}			9.8		nC
Turn-ON Delay Time (Note 1)	t _{D(ON)}	V _{DD} =100V, V _{GS} =10V, I _D =1.0A, R _G =25Ω (Note 1, 2)		8		ns
Rise Time	t _R			20		ns
Turn-OFF Delay Time	t _{D(OFF)}			100		ns
Fall-Time	t _F			48		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Body-Diode Continuous Current	I _S				9	A
Maximum Body-Diode Pulsed Current	I _{SM}				36	A
Drain-Source Diode Forward Voltage (Note 1)	V _{SD}	I _S =9.0A, V _{GS} =0V			1.4	V
Body Diode Reverse Recovery Time (Note 1)	t _{rr}	I _S =9.0A, V _{GS} =0V, di _F /dt=100A/μs		234		ns
Body Diode Reverse Recovery Charge	Q _{rr}				2	

Notes: 1. Pulse Test: Pulse width ≤ 300μs, Duty cycle ≤ 2%.
 2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

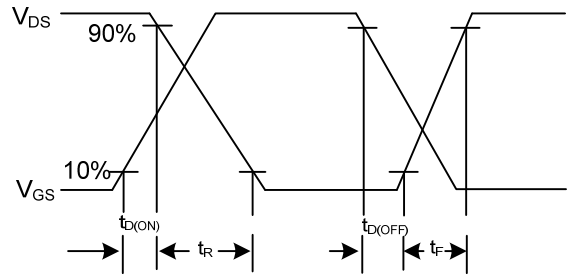
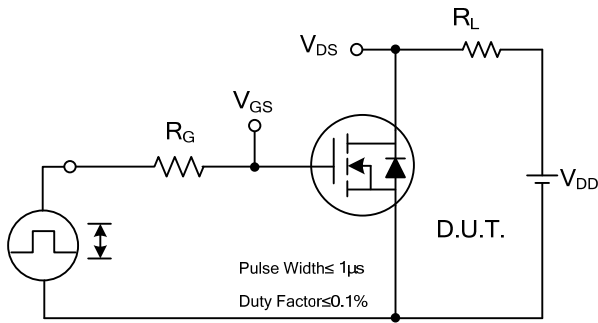


Peak Diode Recovery dv/dt Test Circuit



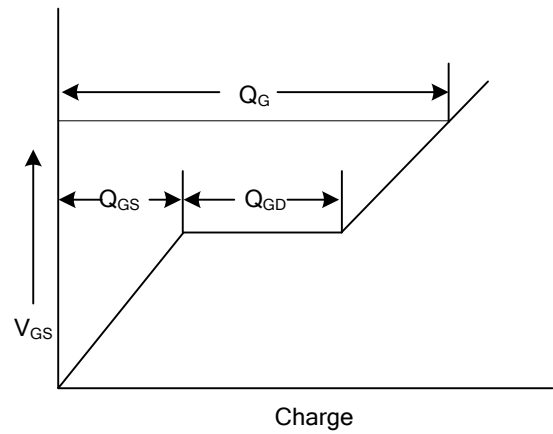
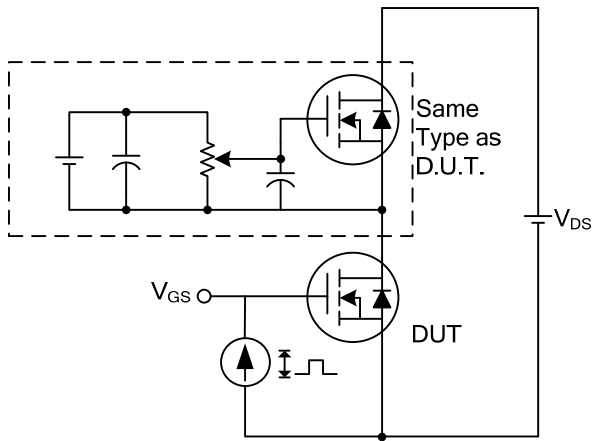
Peak Diode Recovery dv/dt Waveforms

■ TEST CIRCUITS AND WAVEFORMS (Cont.)



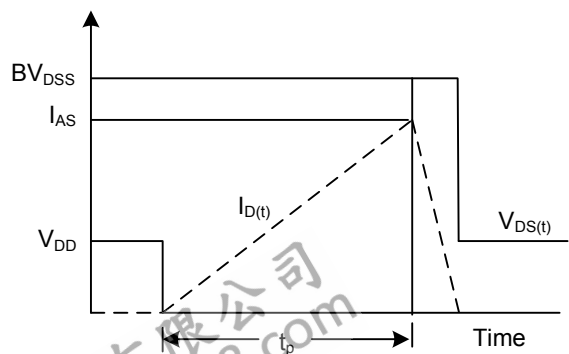
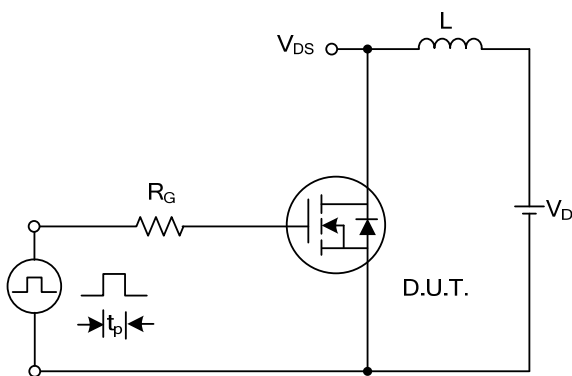
Switching Test Circuit

Switching Waveforms



Gate Charge Test Circuit

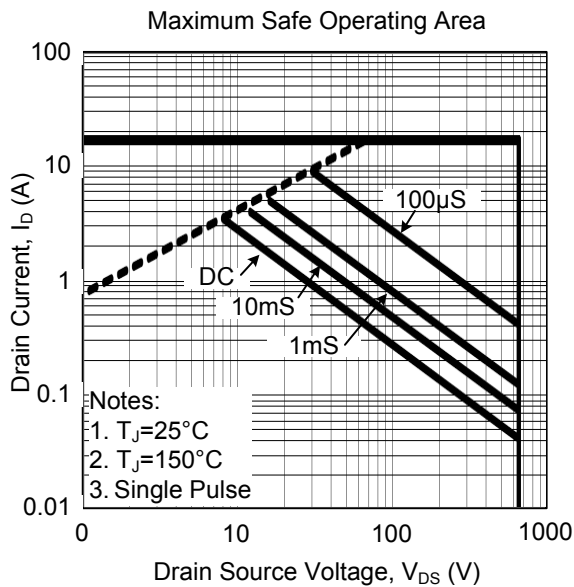
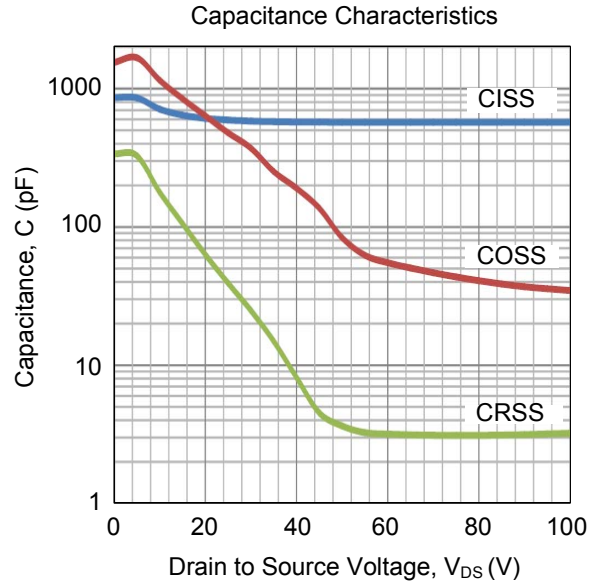
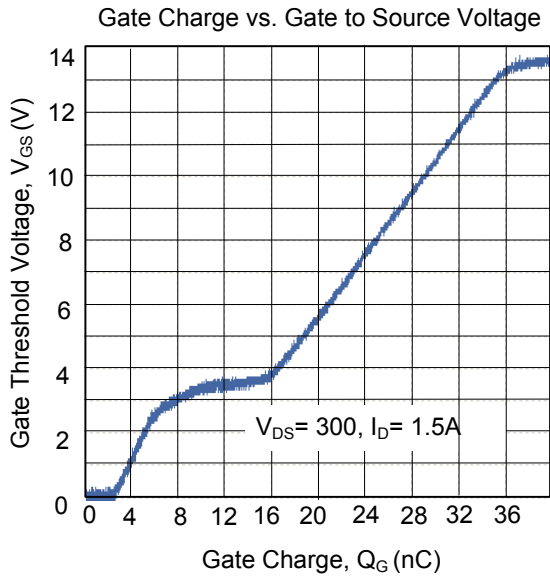
Gate Charge Waveform



Unclamped Inductive Switching Test Circuit

Unclamped Inductive Switching Waveforms

TYPICAL CHARACTERISTICS



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