



BSS127

Power MOSFET

0.021A, 600V ENHANCEMENT N-CHANNEL MOSFET

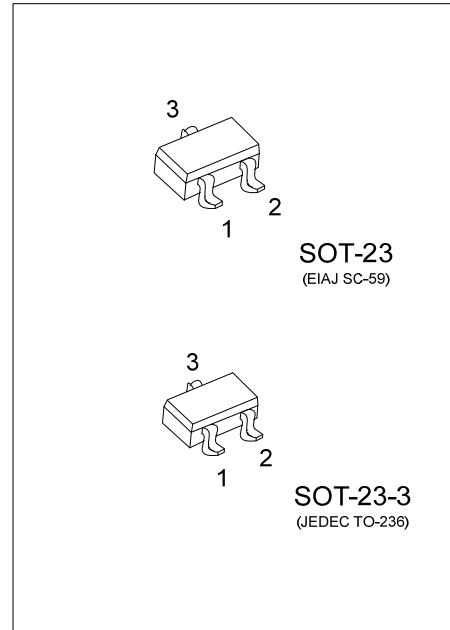
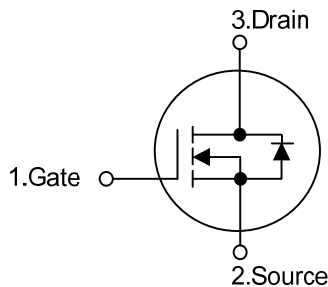
DESCRIPTION

The UTC **BSS127** is an enhancement N-channel mode Power FET, it uses UTC's advanced technology to provide customers ultra high switching speed and ultra low gate charge.

FEATURES

- * $R_{DS(ON)} \leq 600\Omega @ V_{GS}=4.5V, I_D=0.016A$
- * $R_{DS(ON)} \leq 500\Omega @ V_{GS}=10V, I_D=0.016A$
- * Ultra Low Gate Charge (Typical 140nC)
- * Ultra High Switching Speed

SYMBOL



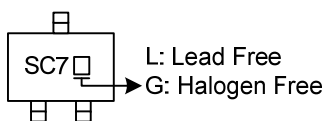
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
BSS127L-AE2-R	BSS127G-AE2-R	SOT-23-3	G	S	D	Tape Reel
BSS127L-AE3-R	BSS127G-AE3-R	SOT-23	G	S	D	Tape Reel

Note: Pin Assignment: G: Gate S: Source D: Drain

<p>BSS127G-AE2-R</p> <p>(1)Packing Type</p> <p>(2)Package Type</p> <p>(3)Green Package</p>	<p>(1) R: Tape Real</p> <p>(2) AE2: SOT-23-3, AE3: SOT-23</p> <p>(3) G: Halogen Free and Lead Free, L: Lead Free</p>
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MARKING



■ ABSOLUTE MAXIMUM RATINGS ($T_A=25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	600	V
Gate-Source Voltage		V_{GSS}	± 20	V
Drain Current	Continuous	$T_A=25^\circ\text{C}$	0.021	A
		$T_A=70^\circ\text{C}$	0.017	A
	Pulsed ($T_A=25^\circ\text{C}$)	I_{DM}	0.09	A
Peak Diode Recovery dv/dt		dv/dt	6	kV/ μs
Power Dissipation ($T_A=25^\circ\text{C}$)		P_D	0.3	W
Junction Temperature		T_J	-55 ~ +150	$^\circ\text{C}$
Storage Temperature Range		T_{STG}	-55 ~ +150	$^\circ\text{C}$

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL CHARACTERISTICS

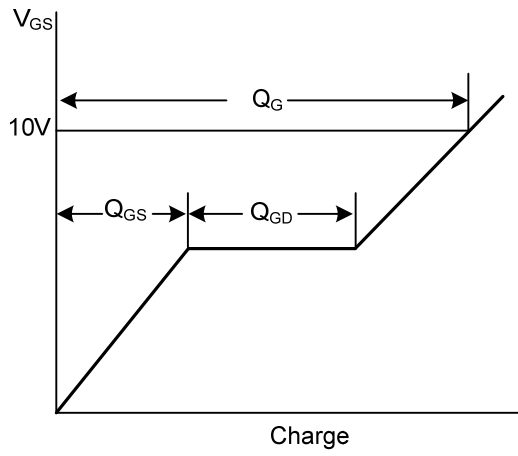
PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	325	$^\circ\text{C/W}$

■ ELECTRICAL CHARACTERISTICS ($T_J=25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D=250\mu\text{A}, V_{GS}=0\text{V}$	600			V
Gate-Source Leakage Current	I_{GSS}	Forward	$V_{GS}=+20\text{V}, V_{DS}=0\text{V}$	+10	+100	nA
		Reverse	$V_{GS}=-20\text{V}, V_{DS}=0\text{V}$	-10	-100	nA
Drain-Source Leakage Current	$I_{D(OFF)}$	$V_{GS}=0\text{V}, V_{DS}=600\text{V}, T_J=25^\circ\text{C}$			0.1	μA
		$V_{GS}=0\text{V}, V_{DS}=600\text{V}, T_J=150^\circ\text{C}$			10	μA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}, I_D=8\mu\text{A}$	1.4	2.0	2.6	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=4.5\text{V}, I_D=0.016\text{A}$		330	600	Ω
		$V_{GS}=10\text{V}, I_D=0.016\text{A}$		310	500	Ω
Forward Transconductance	g_{FS}	$ V_{DS} > 2 I_D R_{DS(ON)MAX}, I_D=0.01\text{A}$	0.007	0.015		S
DYNAMIC PARAMETERS						
Input Capacitance	C_{ISS}	$V_{GS}=0\text{V}, V_{DS}=25\text{V}, f=1.0\text{MHz}$		21	28	pF
Output Capacitance	C_{OSS}			2.4	3	pF
Reverse Transfer Capacitance	C_{RSS}			1.0	1.5	pF
SWITCHING PARAMETERS						
Total Gate Charge	Q_G	$V_{GS}=0\sim 10\text{V}, V_{DS}=300\text{V}, I_D=0.01\text{A}$		0.07	0.10	nC
Gate to Source Charge	Q_{GS}			0.31	0.5	nC
Gate to Drain Charge	Q_{GD}			0.65	1.0	nC
Gate Plateau Voltage	$V_{plateau}$			3.56		V
Turn-ON Delay Time	$t_{D(ON)}$	$V_{DD}=300\text{V}, V_{GS}=10\text{V}, I_D=0.01\text{A}, R_G=6\Omega$		6.1	19.0	ns
Rise Time	t_R			9.7	14.5	ns
Turn-OFF Delay Time	$t_{D(OFF)}$			14	21	ns
Fall-Time	t_F			115	170	ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Continuous Drain-Source Diode Forward Current	I_S	$T_A=25^\circ\text{C}$			0.016	A
Maximum Pulsed Drain-Source Diode Forward Current	I_{SM}	$T_A=25^\circ\text{C}$			0.09	A
Drain-Source Diode Forward Voltage	V_{SD}	$I_F=0.016\text{A}, V_{GS}=0\text{V}, T_J=25^\circ\text{C}$		0.82	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$V_R=300\text{V}, I_F=0.016\text{A}$		160	240	ns
Body Diode Reverse Recovery Charge	Q_{rr}	$di_F/dt=100\text{A}/\mu\text{s}$		13.2	19.8	μC

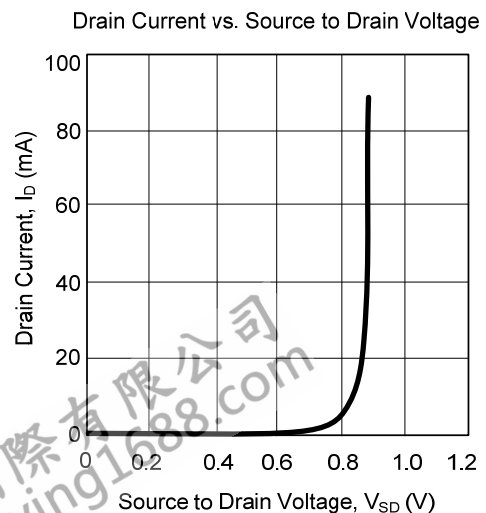
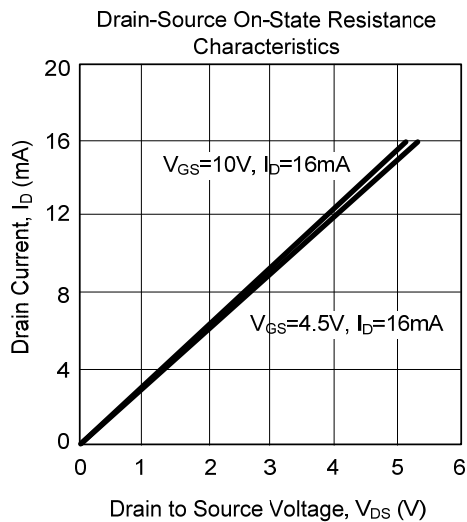
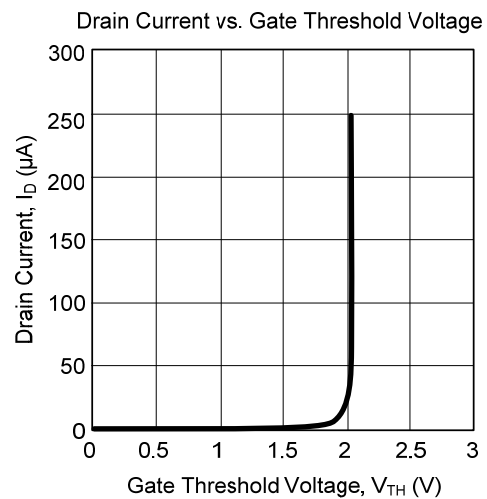
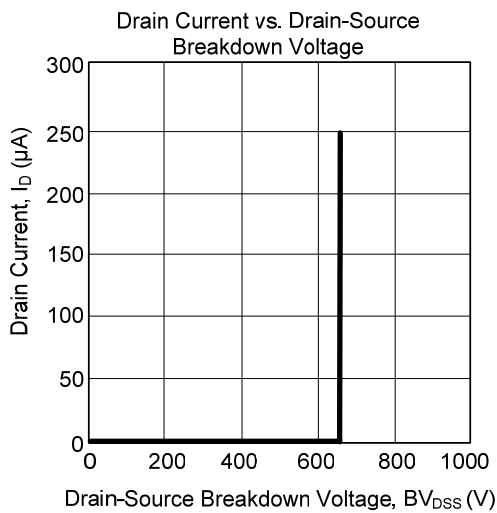
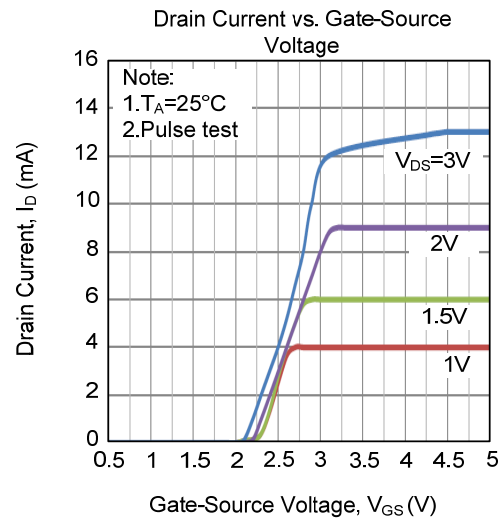
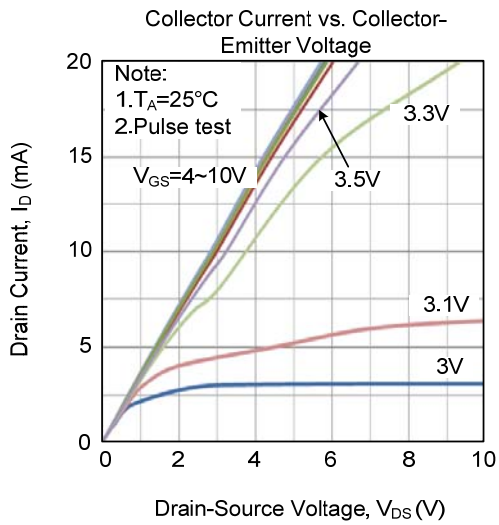
Notes: 1. The Power Dissipation of the package may result in a lower continuous drain current.
2. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2.0\%$.

■ TEST CIRCUITS AND WAVEFORMS



Gate Charge Waveforms

TYPICAL CHARACTERISTICS



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