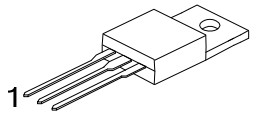
BT150

SCR

SCRS

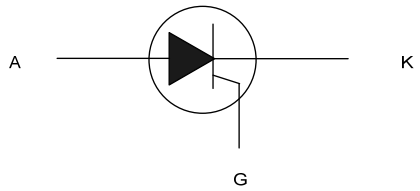


TO-220

■ DESCRIPTION

Passivated thyristors in a plastic envelope, intended for use in applications requiring high bidirectional blocking voltage capability and high thermal cycling performance. Typical applications include motor control, industrial and domestic lighting, heating and static switching.

■ SYMBOL



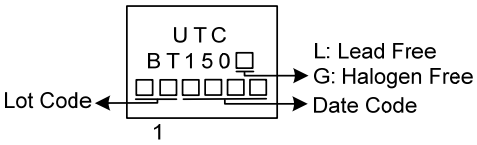
■ ORDERING INFORMATION

Order Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
BT150L-TA3-T	BT150G-TA3-T	TO-220	K	A	G	Tube

Note: Pin Assignment: K: Cathode A: Anode G: Gate

BT150G-TA3-T (1)Packing Type	(1) T: Tube
(2)Package Type	(2) TA3: TO-220
(3)Green Package	(3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



■ ABSOLUTE MAXIMUM RATING

PARAMETER		SYMBOL	RATINGS	UNIT
Repetitive Peak Off-State Voltages	BT150-500	V_{DRM} V_{RRM}	500(Note 2)	V
	BT150-650		650(Note 2)	
	BT150-800		800	
Average On-State Current (half sine wave; T_A ≤113°C)		$I_{T(AV)}$	2.5	A
RMS on-State Current (all conduction angles)		$I_{T(RMS)}$	4	A
Non-Repetitive Peak On-State Current (half sine wave; T_J = 25 °C prior to surge)	t=10ms	I_{TSM}	35	A
	t=8.3ms		38	
I^2t for Fusing (t = 10 ms)		I^2t	6.1	A^2s
Repetitive Rate of Rise of On-State Current After Triggering (I_{TM} = 10 A; I_G = 50 mA; d_{IG} /dt = 50 mA/ms)		d_{IT} /dt	50	A/μs
Peak Gate Current		I_{GM}	2	A
Peak Gate Voltage		V_{GM}	5	V
Peak Reverse Gate Voltage		V_{RGM}	5	V
Peak Gate Power (over any 20 ms period)		P_{GM}	5	W
Average Gate Power		$P_{G(AV)}$	0.5	W
Operating Junction Temperature		T_J	125 (Note 3)	°C
Storage Temperature		T_{STG}	-40 ~150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. Although not recommended, off-state voltages up to 800V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15A/μs.
3. Operation above 110°C may require the use of a gate to cathode resistor of 1kΩ or less.

■ THERMAL RESISTANCES

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Junction to Ambient	$θ_{JA}$		60		K/W
Junction to Case	$θ_{JC}$			4	K/W

■ ELECTRICAL CHARACTERISTICS (T_J=25°C, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Gate Trigger Current	I_{GT}	V_D=12V, I_T=0.1A		15	200	μA
Latching Current	I_L	V_D=12V, I_{GT}=0.1A		0.17	10	mA
Holding Current	I_H	V_D=12V, I_{GT}=0.1A		0.10	6	mA
On-State Voltage	V_T	I_T=5A		1.23	1.8	V
Gate Trigger Voltage	V_{GT}	V_D=12V, I_T =0.1A V_D=$V_{DRM(max)}$, I_T=0.1A, T_J=110°C	0.1	0.4 0.2	1.5	V
Off-State Leakage Current	I_D , I_R	V_D=$V_{DRM(max)}$, V_R=$V_{RRM(max)}$,T_J=125°C		0.1	0.5	mA
Critical Rate of Rise of Off-State Voltage	dV_D /dt	V_{DM}=67%$V_{DRM(max)}$, T_J=125°C,exponential waveform; R_{GK}=100Ω		50		V/μs
Gate Controlled Turn-on Time	t_{gt}	I_{TM}=10A, V_D=$V_{DRM(max)}$, I_G=5mA, dI_G/dt=0.2 A/μs		2		μs
Circuit Commutated Turn-off tIme	t_q	V_D=67% $V_{DRM(max)}$, T_J=125°C, I_{TM}=8A, V_R=25V, dI_{TM}/dt=10A/μs, dV_D/dt=2 V/μs, R_{GK}=1KΩ		100		μs

■ TYPICAL CHARACTERISTICS

Fig 1. Maximum On-State Dissipation, p_{tot}, Versus Average On-State Current, $I_{T(AV)}$, Where a=form factor=$I_{T(RMS)}/I_{T(AV)}$

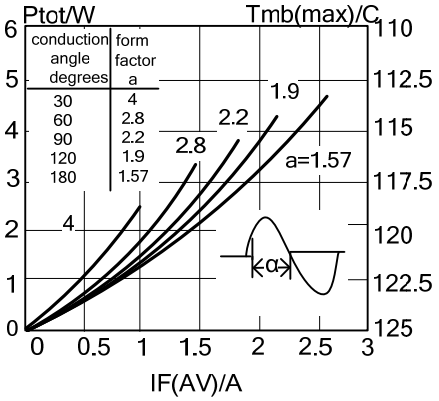


Fig 2. Maximum Permissible Non-Repetitive Peak On-State Current I_{TSM},Versus Pulse Width tp, for Sinusoidal Currents, tp≤ 10ms

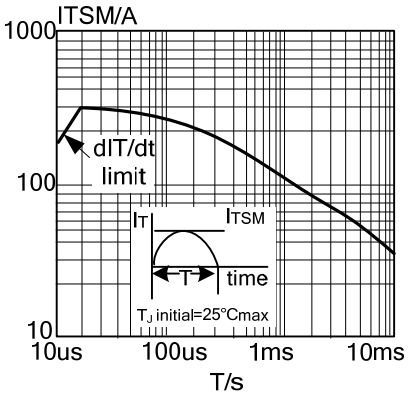


Fig 3. Maximum Permissible Rms Current IT(RMS), Versus Mounting Base Temperature Tmb

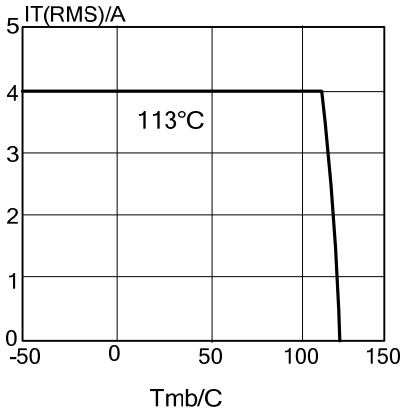


Fig 4. Maximum Permissible Non-Repetitive Peak On-State Current I_{TSM},Versus Number Of Cycles,For Sinusoidal Currents, f=50HZ

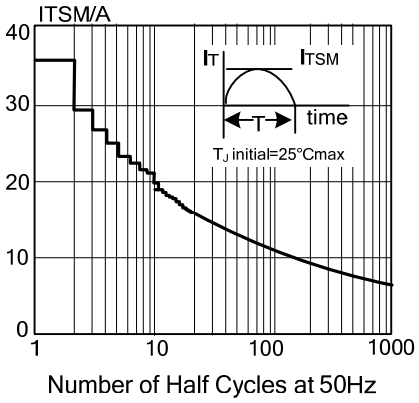


Fig 5. Maximum Permissible Repetitive Rms On-State Current $I_{T(RMS)}$,Versus Surge Duration, For Sinusoidal Currents, f=50HZ; Tmb≤ 113°C

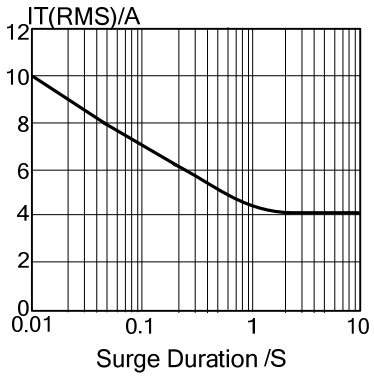
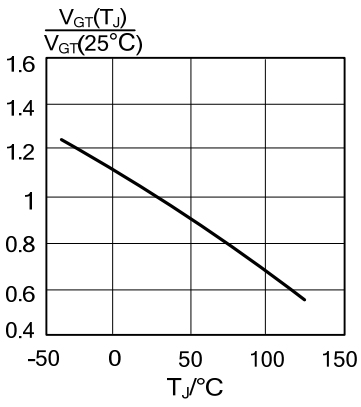


Fig 6. Normalised Gate Trigger Voltage $V_{GT}(T_J)/V_{GT}(25°C)$,Versus Junction Temperature T_J



■ TYPICAL CHARACTERISTICS(Cont.)

Fig 7. Normalised Gate Trigger Current $I_{GT}(T_J)$/ $I_{GT}(25°C)$, Versus Junction Temperature T_J

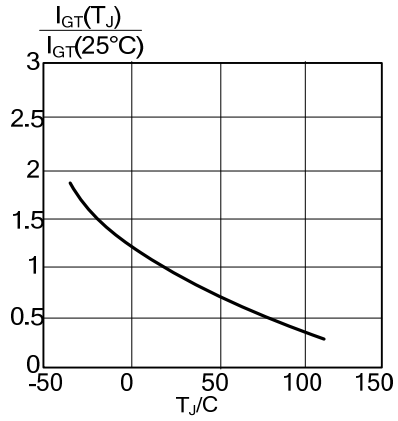


Fig 8. Normalised Latching Current $I_L(T_J)/I_L(25°C)$, Versus Junction Temperature T_J

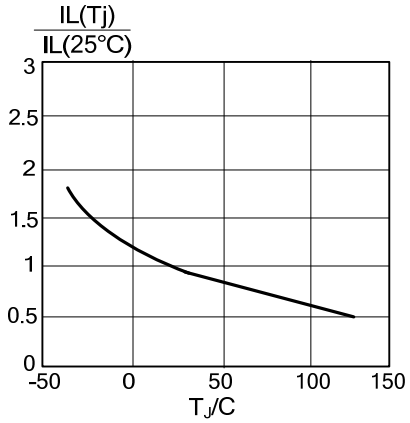


Fig 9. Normalised Holding Current $I_H(T_J)/I_H(25°C)$, Versus Junction Temperature T_J

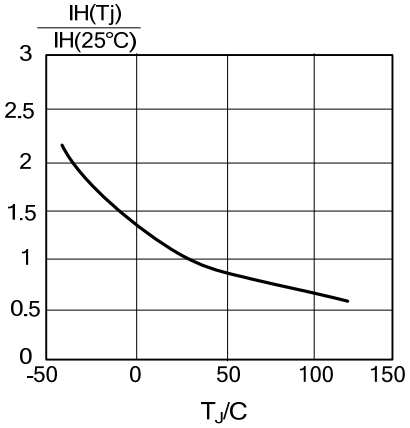


Fig 10. Typical and Maximum On-State Characteristic

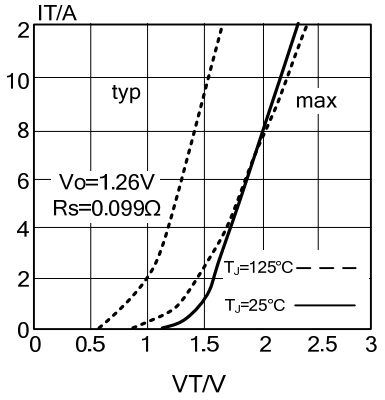


Fig 11.Transient Thermal Impedance Zthj-mb, Versus Pulse Width tp

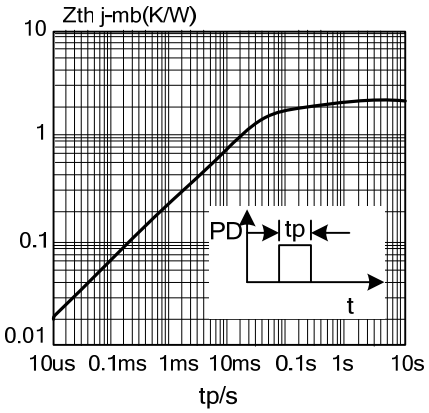


Fig 12. Typical, Critical Rate Of Rise Of Off-State Voltage, dV_D/dt Versus Junction Temperature T_J