



**Description**

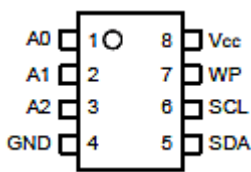
The EC24C02A/04A/08A/16A provides 2048/4096 /8192/16384 bits of serial electrically erasable and programmable read-only memory (EEPROM) organized as 256/512/1024/2048 words of 8 bits each. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation are essential. The EC24C02A/04A/08A/16A is available in space saving PDIP-8,SOP-8, TSSOP-8,MSOP8, DFN-8 and SOT23-5 packages and is accessed via a two-wire serial interface.

**Features**

- Wide Voltage Operation
  - V<sub>cc</sub> = 1.7V to 5.5V
- Operating Ambient Temperature: -40°C to +85°C
- Internally Organized:
  - EC24C02A, 256 X 8 (2K bits)
  - EC24C04A, 512 X 8 (4K bits)
  - EC24C08A, 1024 X 8 (8K bits)
  - EC24C16A, 2048 X 8 (16K bits)
- Two-wire Serial Interface
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- Bidirectional Data Transfer Protocol
- 1 MHz (5V), 400 kHz (1.7V, 2.5V, 2.7V) Compatibility
- Write Protect Pin for Hardware Data Protection
- 8-byte Page (2K), 16-byte Page (4K, 8K,16K) Write Modes
- Partial Page Writes Allowed
- Self-timed Write Cycle (5 ms max)
- High-reliability
  - Endurance: 1 Million Write Cycles
  - Data Retention: 100 Years
- PDIP-8,SOP-8, TSSOP-8,MSOP-8,DFN-8 and SOT23-5 packages

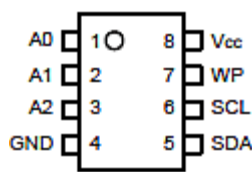
**Pin Configuration**

**SOP-8**  
(EC24C02A/04A/08A/16A)



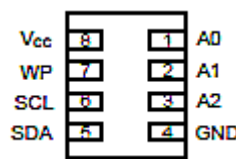
Top-View

**TSSOP-8**  
(EC24C02A/04A/08A/16A)



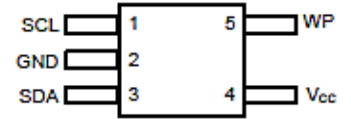
Top-View

**DFN-8**  
(EC24C02A/04A/08A/16A)



Bottom view

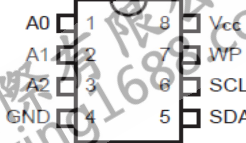
**SOT23-5**  
(EC24C02A/04A/08A)



Top-View

**PDIP-8**

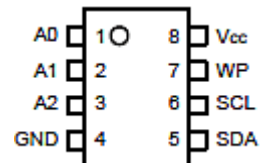
(EC24C02A/04A/08A/16A)



Top-View

**MSOP-8**

(EC24C02A/04A/08A/16A)

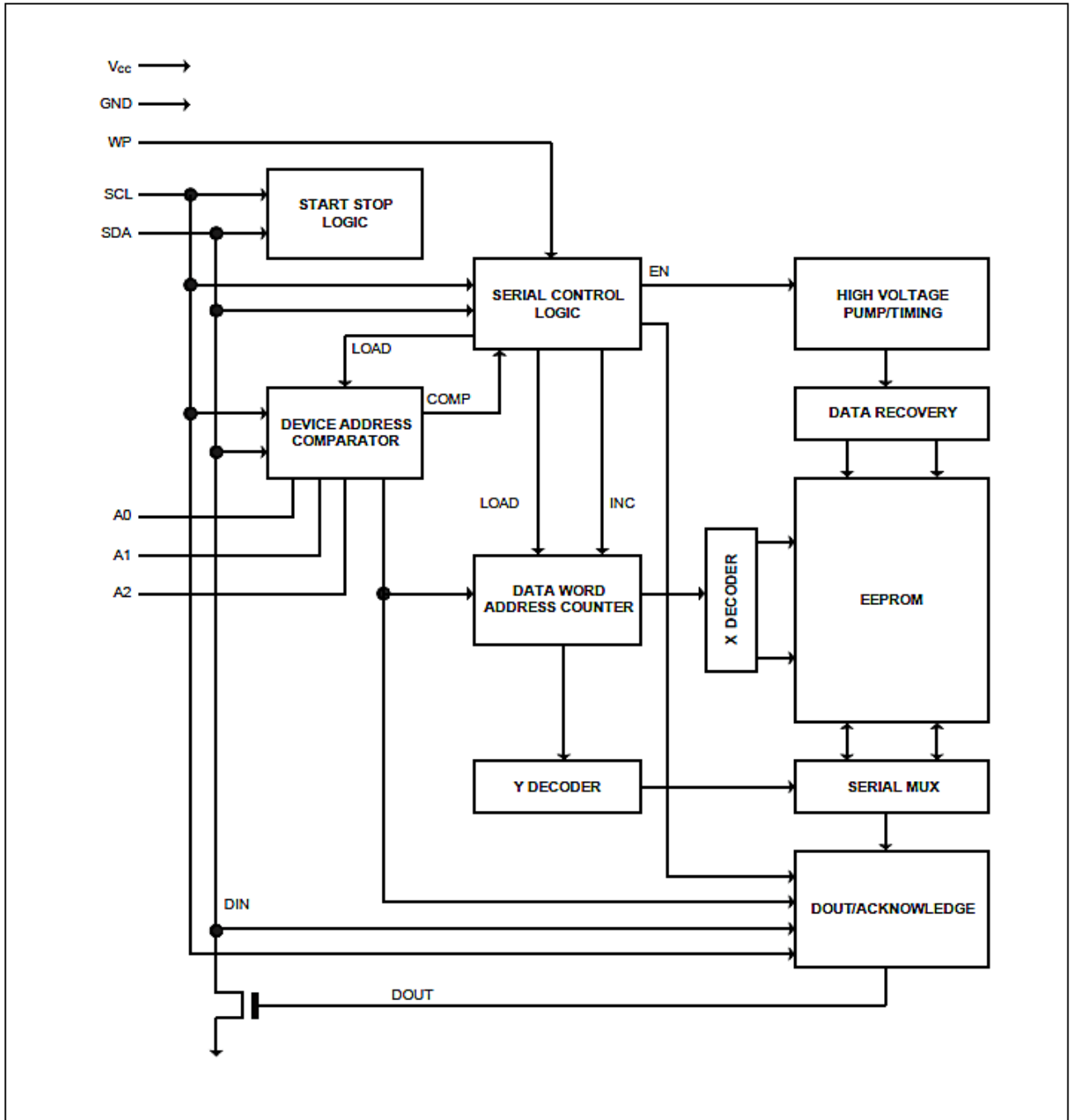


Top-View

Pin Name	Functions
A0 - A2	Address Inputs
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect
GND	Ground
Vcc	Power Supply



Block Diagram





2K/4K/8K/16K-bit 2-WIRE SERIAL CMOS EEPROM

**Pin Descriptions**

**DEVICE/PAGE ADDRESSES (A2, A1 and A0):** The A2, A1 and A0 pins are device address inputs that are hard-wired for the EC24C02A. Eight 2K devices may be addressed on a single bus system (device addressing is discussed in detail under the Device Addressing section).

The EC24C04A uses the A2 and A1 inputs for hard-wired addressing and a total of four 4K devices may be addressed on a single bus system. The A0 (P0) pin is a no connection or can be connected to ground.

The EC24C08A only uses the A2 input for hard-wired addressing and a total of two 8K devices may be addressed on a single bus system. The A0 (P0) and A1 (P1) pins are no connections or can be connected to ground.

The EC24C16A does not use the device address pins, which limits the number of devices on a single bus to one. The A0 (P0), A1 (P1), and A2 (P2) pins are no connections or can be connected to ground.

**SERIAL DATA (SDA):** The SDA pin is bi-directional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open-collector devices.

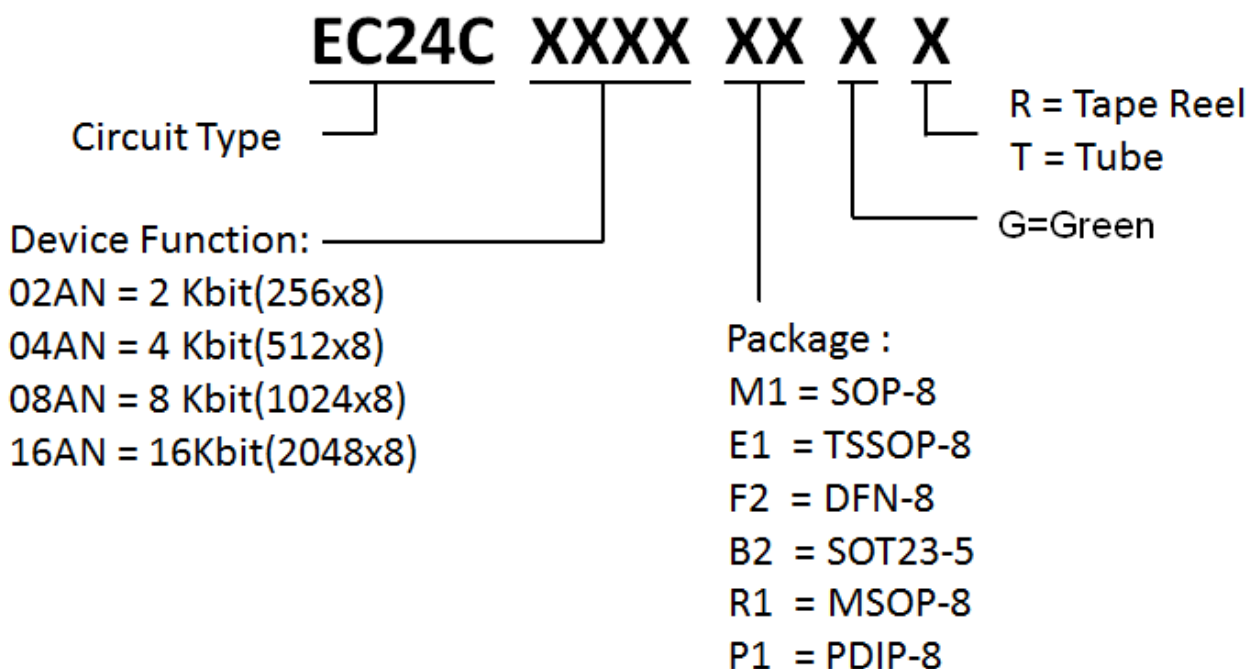
**SERIAL CLOCK (SCL):** The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

**WRITE PROTECT (WP):** The EC24C02A/04A/08A/16A has a Write Protect pin that provides hardware data protection. The Write Protect pin allows normal read/write operations when connected to ground (GND). When the Write Protect pin is connected to VCC, the write protection feature is enabled and operates as shown in the following.

**Write Protect**

WP Pin Status	Part of the Array Protected			
	EC24C02A	EC24C04A	EC24C08A	EC24C16A
At Vcc	Full (2K) Array	Full (4K) Array	Full (8K) Array	Full (16K) Array
At GND	Normal Read / Write Operations			

**Ordering Information**



**Available package types**

Part Number	SOP-8	TSSOP-8	DFN-8	SOT23-5	MSOP-8	PDIP-8
EC24C02A	√	√	√	√	√	√
EC24C04A	√	√	√	√	√	√
EC24C08A	√	√	√	√	√	√
EC24C16A	√	√	√	--	√	√

**Marking Information**

Package type	Part Number	Marking	Marking Information
PDIP-8	EC24CXXANP1GX	24CXXA LLLLL YYWWT	XX is the memory of production. LLLLL is the last five numbers of wafer lot number YYWW is Date Code. T is tracking Code ,T=X
SOP-8	EC24CXXANM1GX		
TSSOP-8	EC24CXXANE1GX		
MSOP-8	EC24CXXANR1GX		
SOT23-5	EC24CXXANB2GX	24CXXA LLLLL	XX is the memory of production. LLLLL is the last five numbers of wafer lot number
DFN-8	EC24CXXANF2GX	CXXA LLLL	XX is the memory of production. LLLL is the last four numbers of wafer lot number

**Memory Organization**

**EC24C02A, 2K SERIAL EEPROM:** Internally organized with 32 pages of 8 bytes each, the 2K requires an 8-bit data word address for random word addressing.

**EC24C04A, 4K SERIAL EEPROM:** Internally organized with 32 pages of 16 bytes each, the 4K requires a 9-bit data word address for random word addressing.

**EC24C08A, 8K SERIAL EEPROM:** Internally organized with 64 pages of 16 bytes each, the 8K requires a 10-bit data word address for random word addressing.

**EC24C16, 16K SERIAL EEPROM:** Internally organized with 128 pages of 16 bytes each, the 16K requires an 11-bit data word address for random word addressing.

**Device Operation**

**CLOCK and DATA TRANSITIONS:** The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see to Figure 1). Data changes during SCL high periods will indicate a start or stop condition as defined below.

**START CONDITION:** A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (see to Figure 2).

**STOP CONDITION:** A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (see to Figure 2).

**ACKNOWLEDGE:** All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a "0" to acknowledge that it has received each word. This happens during the ninth clock cycle (see to Figure 3).

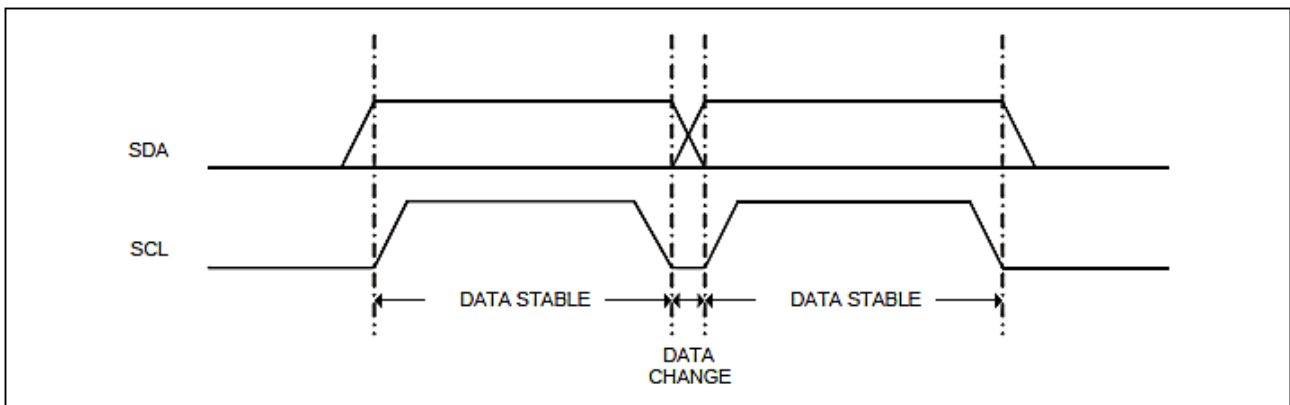
2K/4K/8K/16K-bit 2-WIRE SERIAL CMOS EEPROM

**STANDBY MODE:** The EC24C02A/04A/08A/16A features a low-power standby mode which is enabled: (a) upon power-up and (b) after the receipt of the STOP bit and the completion of any internal operations.

**MEMORY RESET:** After an interruption in protocol, power loss or system reset, any two-wire part can be reset by following these steps:

1. Clock up to 9 cycles.
2. Look for SDA high in each cycle while SCL is high.
3. Create a start condition.

**Figure 1: Data Validity**



**Figure 2: Start and Stop Definition**

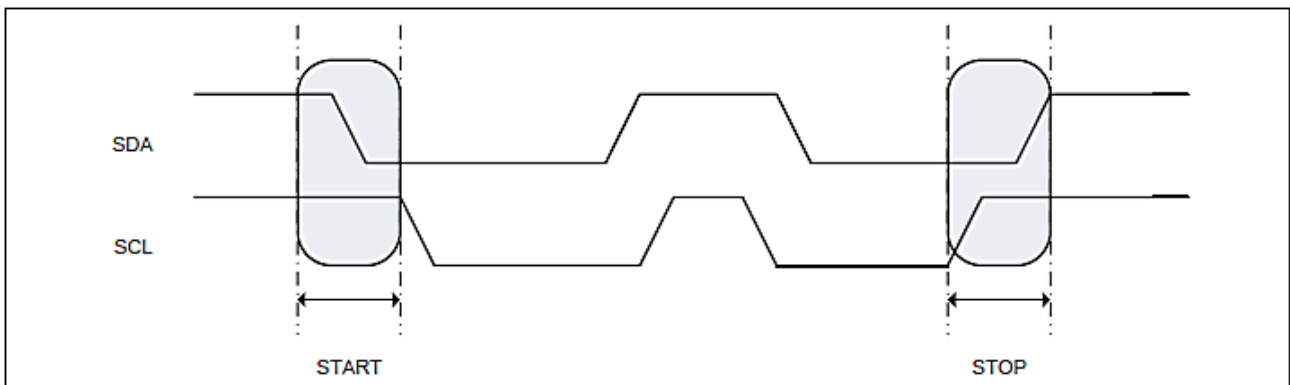
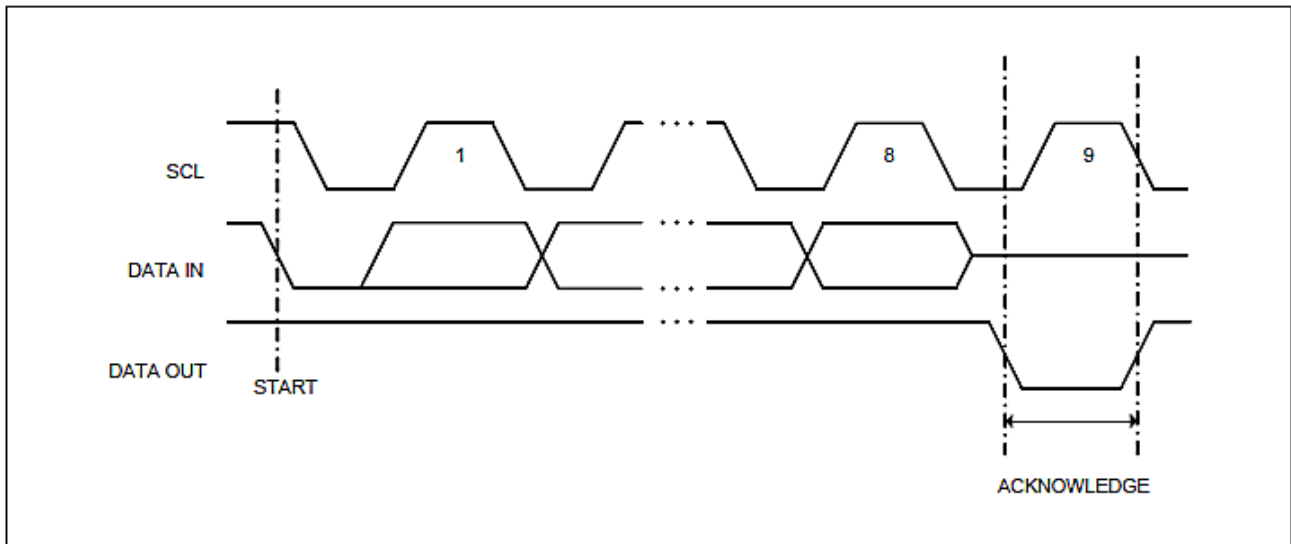


Figure 3: Output Acknowledge



### Device Addressing

The 2K, 4K, 8K and 16K EEPROM devices all require an 8-bit device address word following a start condition to enable the chip for a read or write operation (see to Figure 4).

The device address word consists of a mandatory "1", "0" sequence for the first four most significant bits as shown. This is common to all the Serial EEPROM devices.

The next 3 bits are the A2, A1 and A0 device address bits for the 2K EEPROM. These 3 bits must compare to their corresponding hard-wired input pins.

The 4K EEPROM uses the A2 and A1 device address bits with the third bit being a memory page address bit. The two device address bits must compare to their corresponding hard-wired input pins. The A0 (P0) pin is no connection.

The 8K EEPROM only uses the A2 device address bit with the next 2 bits being for memory page addressing. The A2 bit must compare to its corresponding hard-wired input pin. The A1 (P1) and A0 (P0) pins are no connections.

The 16K does not use any device address bits but instead the 3 bits are used for memory page addressing. These page addressing bits on the 4K, 8K and 16K devices should be considered the most significant bits of the data word address which follows. The A0 (P0), A1 (P1) and A2 (P2) pins are no connections.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon a compare of the device address, the EEPROM will output a "0". If a compare is not made, the chip will return to a standby state.

**DATA SECURITY:** The EC24C02A/04A/08A/16A has a hardware data protection scheme that allows the user to write protect the entire memory when the WP pin is at V<sub>cc</sub>.

### Write Operations

**BYTE WRITE:** A write operation requires an 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a "0" and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a "0" and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally timed write cycle,  $t_{WR}$ , to the nonvolatile memory. All inputs are disabled







Figure 7: Current Address Read

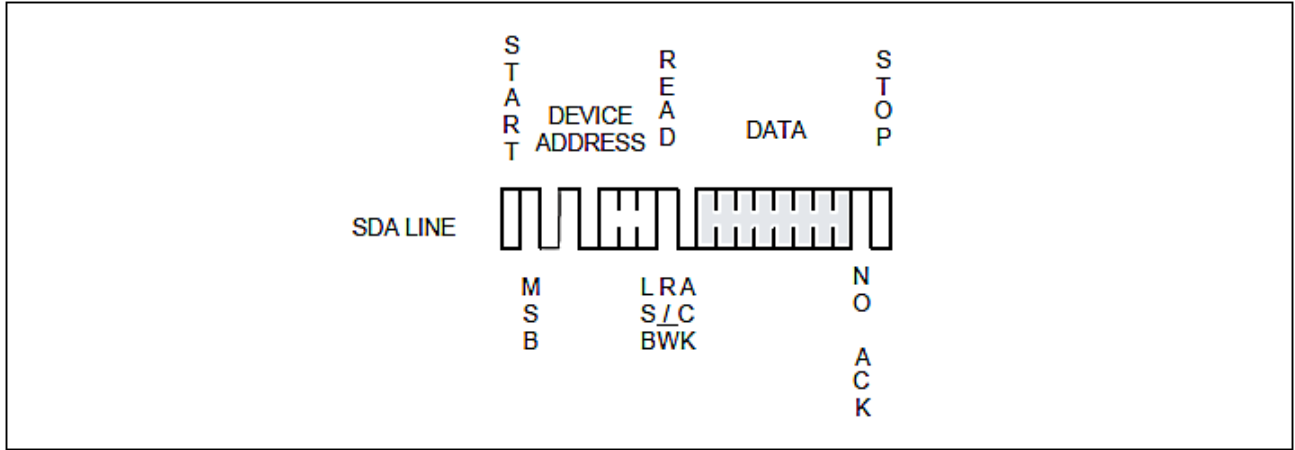


Figure 8: Random Read

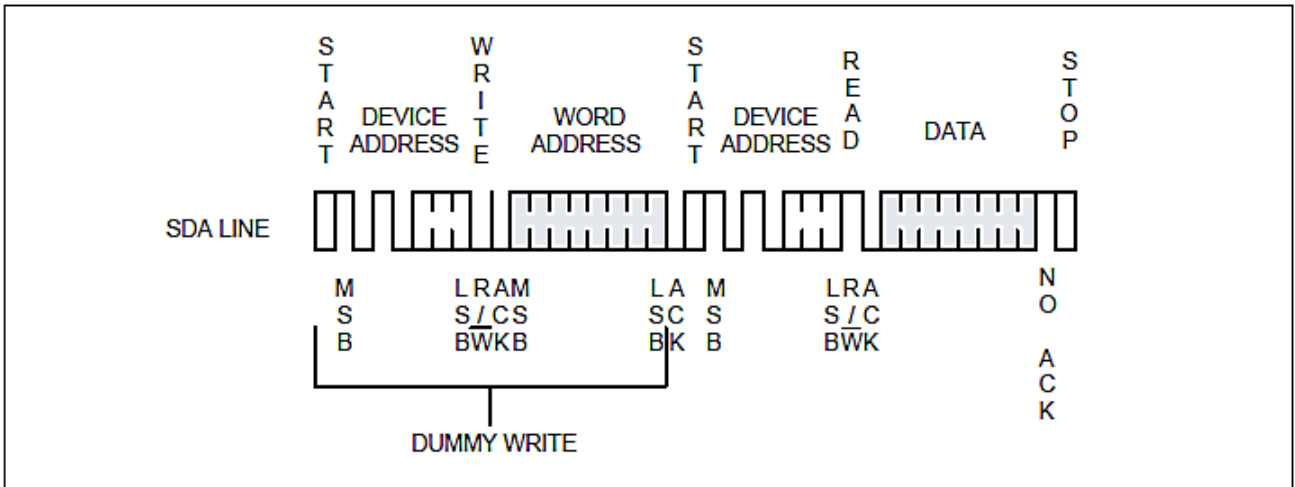
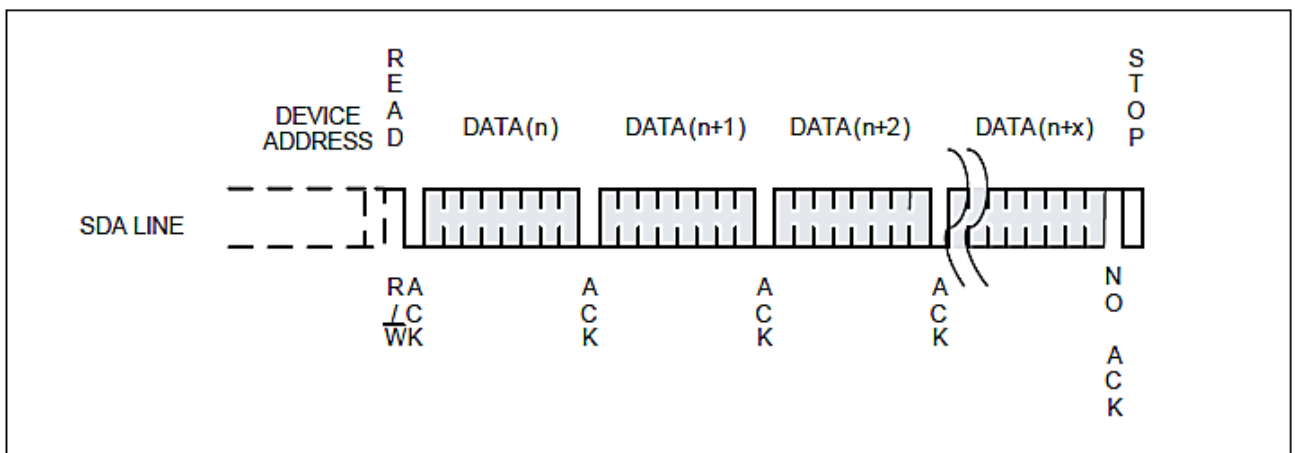


Figure 9: Sequential Read





### Electrical Characteristics

#### Absolute Maximum Stress Ratings

DC Supply Voltage	-0.3V to +6.5V
Input / Output Voltage	GND-0.3V to V <sub>CC</sub> +0.3V
Operating Ambient Temperature	-40°C to +85°C
Storage Temperature	-65°C to +150°C

#### Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

### DC Electrical Characteristics

Applicable over recommended operating range from: T<sub>A</sub> = -40°C to +85°C, V<sub>CC</sub> = +1.7V to +5.5V (unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Supply Voltage	V <sub>CC</sub>	1.7		5.5	V	
Supply Current V <sub>CC</sub> = 5.0V	I <sub>CC1</sub>		0.4	1.0	mA	READ at 400 kHz
Supply Current V <sub>CC</sub> = 5.0V	I <sub>CC2</sub>		2.0	3.0	mA	WRITE at 400 kHz
Standby Current	I <sub>SB</sub>			3.0	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND
Input Leakage Current	I <sub>LI</sub>			3.0	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND
Output Leakage Current	I <sub>LO</sub>		0.05	3.0	μA	V <sub>OUT</sub> = V <sub>CC</sub> or GND
Input Low Level	V <sub>IL1</sub>	-0.3		V <sub>CC</sub> x 0.3	V	V <sub>CC</sub> = 1.8V to 5.5V
Input High Level	V <sub>IH1</sub>	V <sub>CC</sub> x 0.7		V <sub>CC</sub> + 0.3	V	V <sub>CC</sub> = 1.8V to 5.5V
Input Low Level	V <sub>IL2</sub>	-0.3		V <sub>CC</sub> x 0.2	V	V <sub>CC</sub> = 1.7V
Input High Level	V <sub>IH2</sub>	V <sub>CC</sub> x 0.7		V <sub>CC</sub> + 0.3	V	V <sub>CC</sub> = 1.7V
Output Low Level V <sub>CC</sub> =5.0V	V <sub>OL3</sub>			0.4	V	I <sub>OL</sub> = 3.0 mA
Output Low Level V <sub>CC</sub> =3.0V	V <sub>OL2</sub>			0.4	V	I <sub>OL</sub> = 2.1 mA
Output Low Level V <sub>CC</sub> =1.7V	V <sub>OL1</sub>			0.2	V	I <sub>OL</sub> = 0.15 mA

### Pin Capacitance

Applicable over recommended operating range from T<sub>A</sub> = 25°C, f = 1.0 MHz, V<sub>CC</sub> = +1.7V

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Input/Output Capacitance (SDA)	C <sub>I/O</sub>	-	-	8	pF	V <sub>I/O</sub> = 0V
Input Capacitance (A0, A1, A2, SCL)	C <sub>IN</sub>	-	-	6	pF	V <sub>IN</sub> = 0V



### AC Electrical Characteristics

Applicable over recommended operating range from  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{CC} = +1.7\text{V}$  to  $+5.5\text{V}$ ,  $C_L = 1$  TTL Gate and  $100\text{ pF}$  (unless otherwise noted)

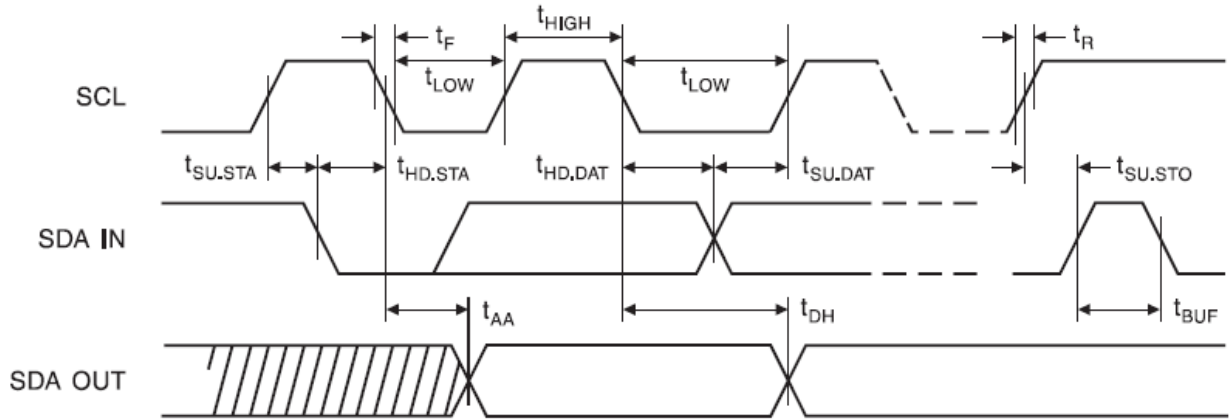
Parameter	Symbol	$1.7\text{V} \leq V_{CC} < 2.5\text{V}$			$2.5\text{V} \leq V_{CC} \leq 5.5\text{V}$			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Clock Frequency, SCL	$f_{SCL}$	-	-	400	-	-	1000	kHz
Clock Pulse Width Low	$t_{LOW}$	1.2	-	-	0.6	-	-	$\mu\text{s}$
Clock Pulse Width High	$t_{HIGH}$	0.6	-	-	0.4	-	-	$\mu\text{s}$
Noise Suppression Time	$t_i$	-	-	50	-	-	40	ns
Clock Low to Data Out Valid	$t_{AA}$	0.05	-	0.9	0.05	-	0.55	$\mu\text{s}$
Time the bus must be free before a new transmission can start	$t_{BUF}$	1.2	-	-	0.5	-	-	$\mu\text{s}$
1Start Hold Time	$t_{HD,STA}$	0.6	-	-	0.25	-	-	$\mu\text{s}$
Start Setup Time	$t_{SU,STA}$	0.6	-	-	0.25	-	-	$\mu\text{s}$
Data In Hold Time	$t_{HD,DAT}$	0	-	-	0	-	-	$\mu\text{s}$
Data In Setup Time	$t_{SU,DAT}$	100	-	-	100	-	-	ns
Inputs Rise Time(1)	$t_R$	-	-	0.3	-	-	0.3	$\mu\text{s}$
Inputs Fall Time(1)	$t_F$	-	-	300	-	-	100	ns
Stop Setup Time	$t_{SU,STO}$	0.6	-	-	0.25	-	-	$\mu\text{s}$
Data Out Hold Time	$t_{DH}$	50	-	-	50	-	-	ns
Write Cycle Time	$t_{WR}$	-	1.5	5	-	1.5	5	ms
5.0V, 25°C, Byte Mode	Endurance	1M	-	-	-	-	-	Write Cycles

#### Note

1. This parameter is characterized and is not 100% tested.
2. AC measurement conditions:
  - RL (connects to  $V_{CC}$ ):  $1.3\text{k}\Omega$  (2.5V, 5V),  $10\text{k}\Omega$  (1.7V)
  - Input pulse voltages:  $0.3 \times V_{CC}$  to  $0.7 \times V_{CC}$
  - Input rise and fall time:  $\leq 50\text{ ns}$
  - Input and output timing reference voltages:  $0.5 \times V_{CC}$
  - The value of RL should be concerned according to the actual loading on the user's system.

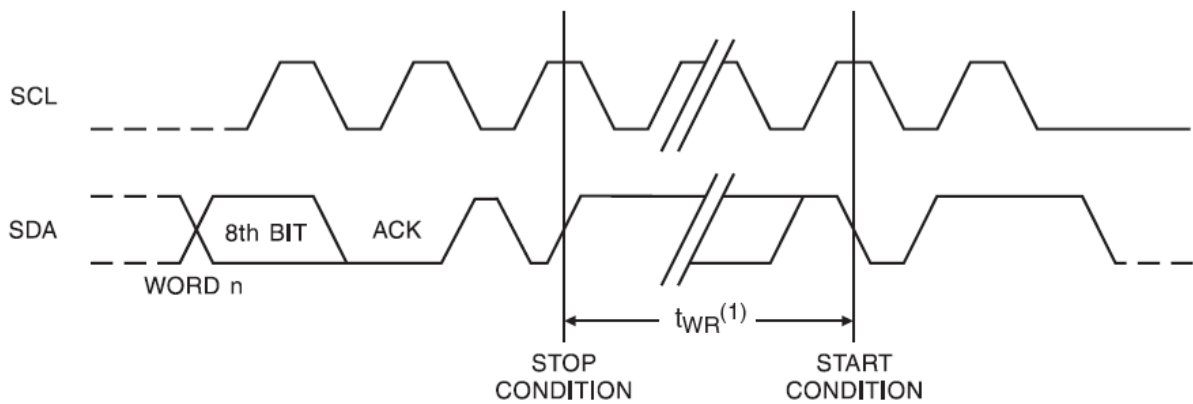
### Bus Timing

Figure 10: SCL: Serial Clock, SDA: Serial Data I/O



### Write Cycle Timing

Figure 11: SCL: Serial Clock, SDA: Serial Data I/O



**Note**

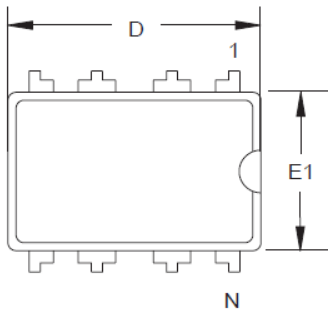
1. The write cycle time  $t_{WR}$  is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

**Mechanical Dimensions**

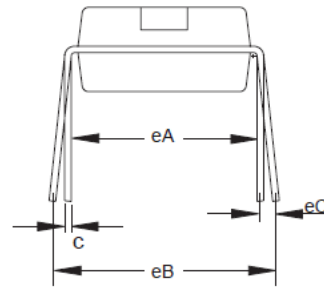
**OUTLINE DRAWING PDIP - 8**

Available package types : EC24C02A/04A/08A/16A

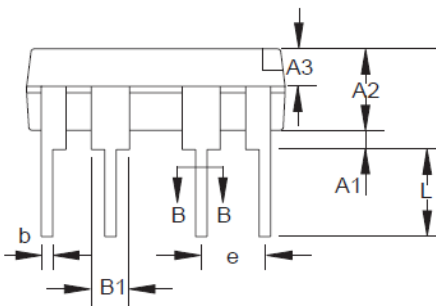
**Top View**



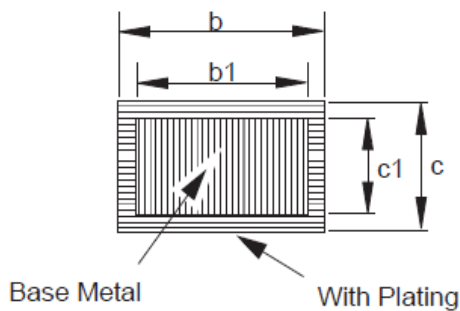
**End View**



**Side View**



**Section B - B**



**COMMON DIMENSIONS**  
(Unit of Measure = mm)

SYMBOL	MIN	MAX
A	3.60	4.00
A1	0.51	-
A2	3.10	3.50
A3	1.50	1.70
b	0.44	0.53
b1	0.43	0.48
B	1.52 BSC	
c	0.25	0.31
c1	0.24	0.26
D	9.05	9.45
E1	6.15	6.55
e	2.54 BSC	
eA	7.62 BSC	
eB	7.62	9.50
eC	0	0.94
L	3.00	-

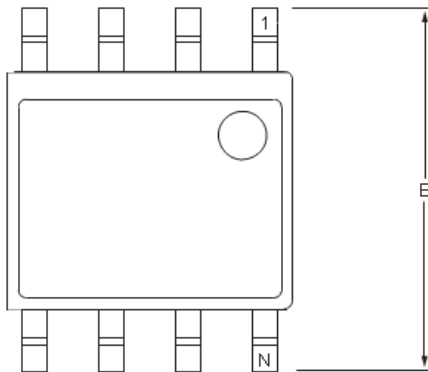
2K/4K/8K/16K-bit 2-WIRE SERIAL CMOS EEPROM

**Mechanical Dimensions**

**OUTLINE DRAWING SOP- 8**

Available package types : EC24C02A/04A/08A/16A

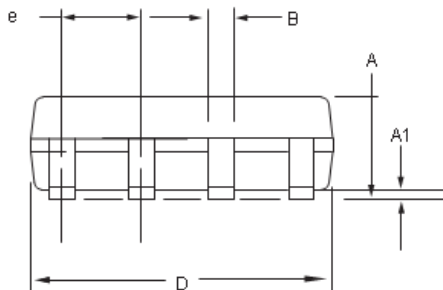
**Top View**



**End View**



**Side View**



**COMMON DIMENSIONS**

(Unit of Measure = mm)

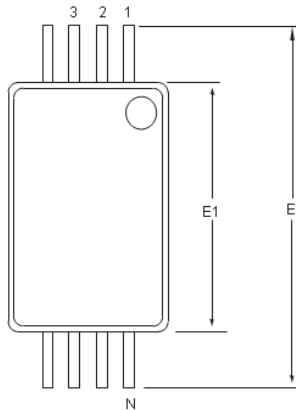
SYMBOL	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.31	0.51
C	0.17	0.25
D	4.70	5.10
E1	3.80	4.00
E	5.79	6.20
e	1.27 BSC	
L	0.40	1.27
θ	0°	8°

**Mechanical Dimensions**

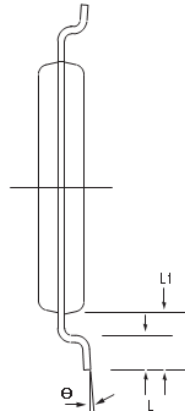
**OUTLINE DRAWING TSSOP-8**

Available package types : EC24C02A/04A/08A/16A

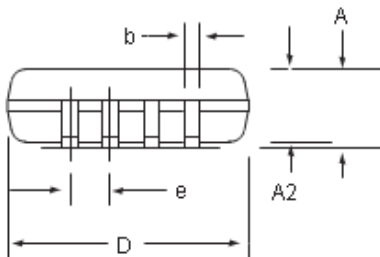
**Top View**



**End View**



**Side View**



**COMMON DIMENSIONS**

(Unit of Measure = mm)

SYMBOL	MIN	MAX
D	2.80	3.20
E	6.20	6.60
E1	4.20	4.60
A	-	1.20
A2	0.80	1.15
b	0.19	0.30
e	0.65 BSC	
L	0.45	0.75
L1	1.00 BSC	
$\theta$	0°	8°



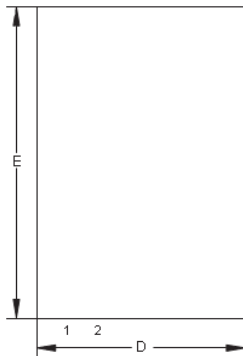
2K/4K/8K/16K-bit 2-WIRE SERIAL CMOS EEPROM

**Mechanical Dimensions**

**OUTLINE DRAWING DFN-8**

Available package types : EC24C02A/04A/08A/16A

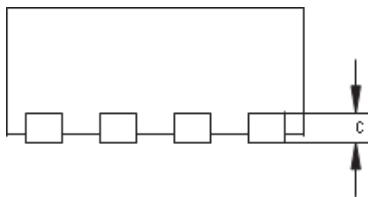
Top View



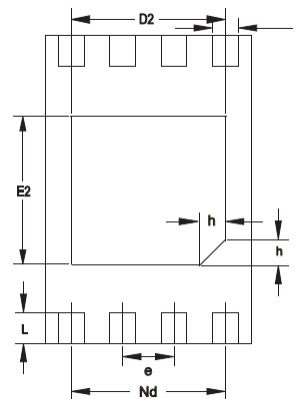
End View



Side View



Bottom View



**COMMON DIMENSIONS**

(Unit of Measure = mm)

SYMBOL	MIN	MAX
A	0.70	0.80
A1	-	0.05
b	0.18	0.30
c	0.18	0.25
D	1.90	2.10
D2	1.50 REF	
e	0.50 BSC	
Nd	1.50 BSC	
E	2.90	3.10
E2	1.60 BSC	
L	0.30	0.50
h	0.20	0.30

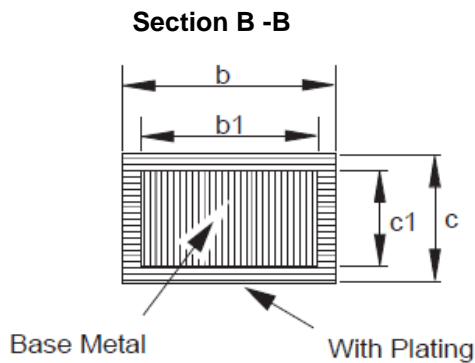
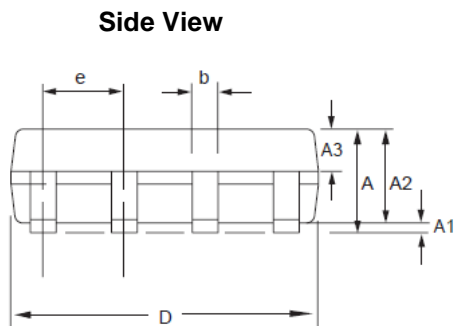
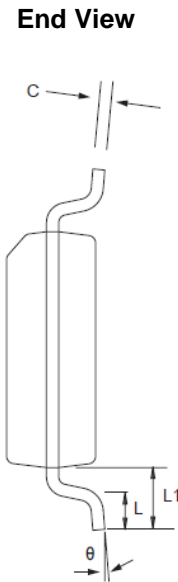
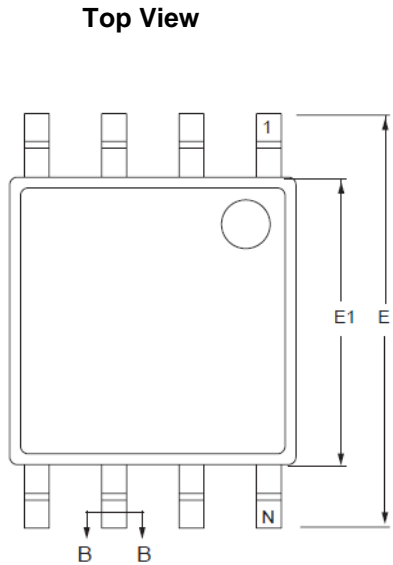


2K/4K/8K/16K-bit 2-WIRE SERIAL CMOS EEPROM

**Mechanical Dimensions**

**OUTLINE DRAWING MSOP-8**

Available package types : EC24C02A/04A/08A/16A



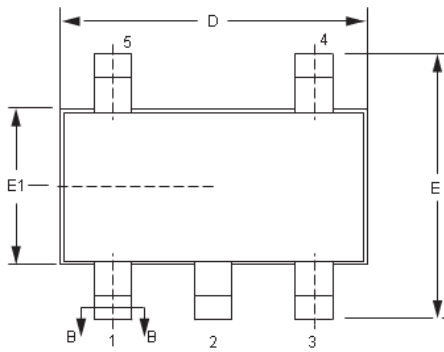
**COMMON DIMENSIONS**  
(Unit of Measure = mm)

SYMBOL	MIN	MAX
A	-	1.10
A1	0.05	0.15
A2	0.75	0.95
A3	0.30	0.40
b	0.29	0.38
b1	0.28	0.33
c	0.15	0.20
c1	0.14	0.16
D	2.90	3.10
E	4.70	5.10
E1	2.90	3.10
e	0.65 BSC	
L	0.40	0.70
L1	0.95 BSC	
$\theta$	0°	8°

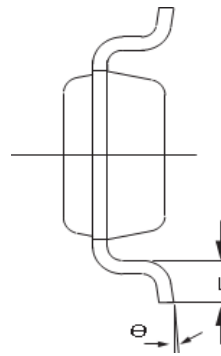
**Mechanical Dimensions**  
**OUTLINE DRAWING SOT23-5**

Available package types : EC24C02A/04A/08A

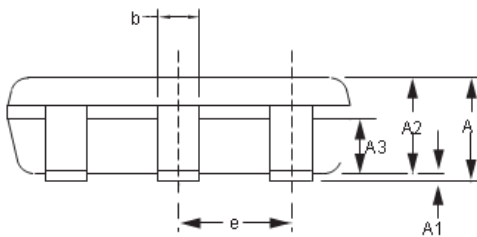
**Top View**



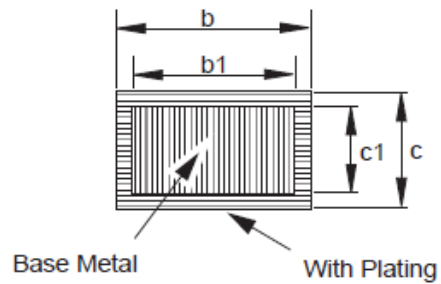
**End View**



**Side View**



**Section B-B**



**COMMON DIMENSIONS**  
 (Unit of Measure = mm)

SYMBOL	MIN	MAX
A	1.05	1.30
A1	0	0.10
A2	1.00	1.20
A3	0.55	0.75
b	0.30	0.50
b1	0.33	0.38
c	0.10	0.21
c1	0.14	0.16
D	2.72	3.12
E	2.60	3.00
E1	1.40	1.80
e	0.95 BSC	
L	0.30	0.60
$\theta$	0°	8°