1A Ultra Low Dropout Voltage Regulator with Internal Soft-Start (60uS)

General Description

The EMP8161/A series can drive 1A of continuous output loading and provide a good performance with a typical dropout voltage as 90mV through an internal n-channel power MOSFETs. The output voltage can be adjustable from 0.8V to Vout that could be very close to VIN.

There are two power supplies pins for the linear regulator. The control circuitry in this linear regulator requires a supply V_{CTRL} and the driver, the n-channel MOSFET, uses another one.

The EMP8161/A series provide a stable output voltage with an output capacitor as low as 10uF. In order to prevent the linear regulator get damage from thermal increasing, the EMP8161/A series provide fold-back over loading protection and over temperature protection features. An internal soft-start or adjustable soft-start by SS pin can minimizes capacitive inrush current on the input power source during start-up. PG stay low until the output reaches 92% of value that is settled during start-up.

The EMP8161/A series are available in E-SOP-8L package.

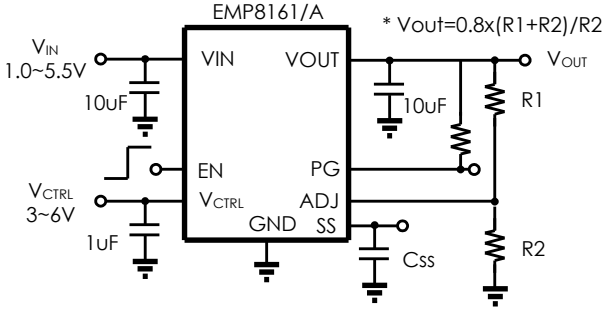
Applications

- High Efficiency Linear Regulators
- DSP Core and I/O Voltage
- Post Regulator for Switching Power

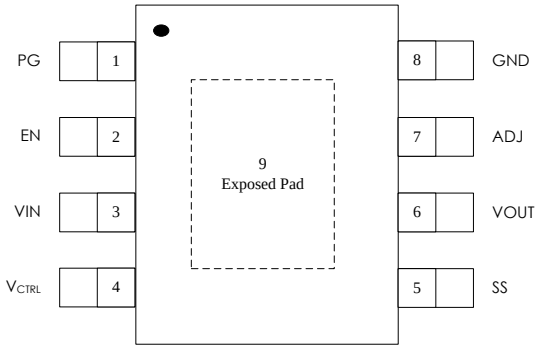
Features

- Input Voltage Range：+1.0V to +5.5V
- Maximum Output Current：1A
- RDS-on: 95mohm
- Dropout Voltage：90mV @ I_{OUT}=1A (Vout=0.8V, V_{CTRL}=5V)
- ±2% Output Voltage Accuracy
- High Ripple Rejection：>80 dB @ I_{OUT}=1A (Vout=0.8V, V_{CTRL}=5V, C_{SS}=10nF)
- Fold back short circuit protection
- Thermal Overload Shutdown Protection
- Under Voltage Protection
- Power Good Indicator (Open-Drain)
- Internal soft-start 60us
- Soft-Start Pin Provides Startup with Ramp Time Set by External Capacitor

Typical Application



Connection Diagrams

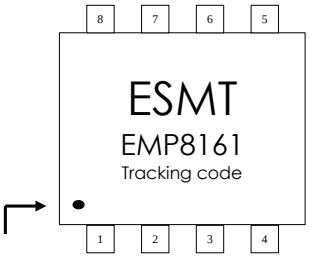
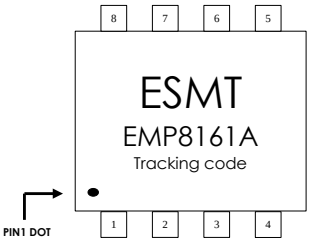


Order Information

EMP8161#-XXSG08NRR

#	Null: EN pin with pull-low resister
	A: EN pin with pull-high resister
XX	Output voltage version
	Example,
	00, Output Voltage adjustable
	12, Output Voltage 1.2V
	33, Output Voltage 3.3V
SG08	E-SOP-8L Package (Package Code)
NRR	RoHS & Halogen free package
	Commercial Grade Temperature
	Rating: -40 to 85°C
	Package in Tape & Reel

Order, Marking & Packing Information

Package	Vout	EN Resister	Product ID.	Marking	Packing
E-SOP-8L	ADJ	Pull-low	EMP8161-00SG08NRR		Tape & Reel 3kpcs
E-SOP-8L	ADJ	Pull-high	EMP8161A-00SG08NRR		Tape & Reel 3kpcs

Note. The product ID. not listed in above, that's by request.

Device comparison table

Product	Iout	EN state in Chip Internally	Soft-Start time in chip internally
EMP8161	**1A**	**With pull low Resistor**	**60uS**
EMP8161A	**1A**	**With pull high Resistor**	**60uS**
EMP8166	1A	With pull low Resistor	600uS
EMP8166A	1A	With pull high Resistor	600uS
EMP8160	2A	With pull low Resistor	60uS
EMP8160A	2A	With pull high Resistor	60uS
EMP8165	2A	With pull low Resistor	600uS
EMP8165A	2A	With pull high Resistor	600uS
EMP8170	3A	With pull low Resistor	60uS
EMP8170A	3A	With pull high Resistor	60uS
EMP8175	3A	With pull low Resistor	600uS
EMP8175A	3A	With pull high Resistor	600uS

Pin Functions

Name	E-SOP-8L	Function
PG	1	**Power Good Indicator.**
EN	2	**Enable Input.** Enable the regulator by pulling the EN pin High. Set the regulator into the disable mode by pulling the EN pin low. The EN pin is with pull low 400kohm resistor internally for EMP8160 (with pull high 400kohm internally for EMP8160A).
VIN	3	**Supply Voltage Input.** Require a minimum input capacitor of close to 10μF to ensure stability and sufficient decupling from the ground pin.
V_{CTRL}	4	**Supply Voltage for Control Circuit.**
SS	5	**Soft-Start.** Connect a 1~10nF capacitor between this pin and GND to reduce inrush current during start-up.
VOUT	6	**Output Voltage.**
ADJ	7	**Adjust Vout.** Feedback input. Connect to resistive voltage-divider network. *** ADJ connected to GND for Fixed Vout.**
GND	8	**Ground Pin.**
Exposed Pad	9	**Thermal Pad** This pin must be connected to ground. The thermal pad with large thermal land area on the PCB will helpful chip power dissipation.

Functional Block Diagram

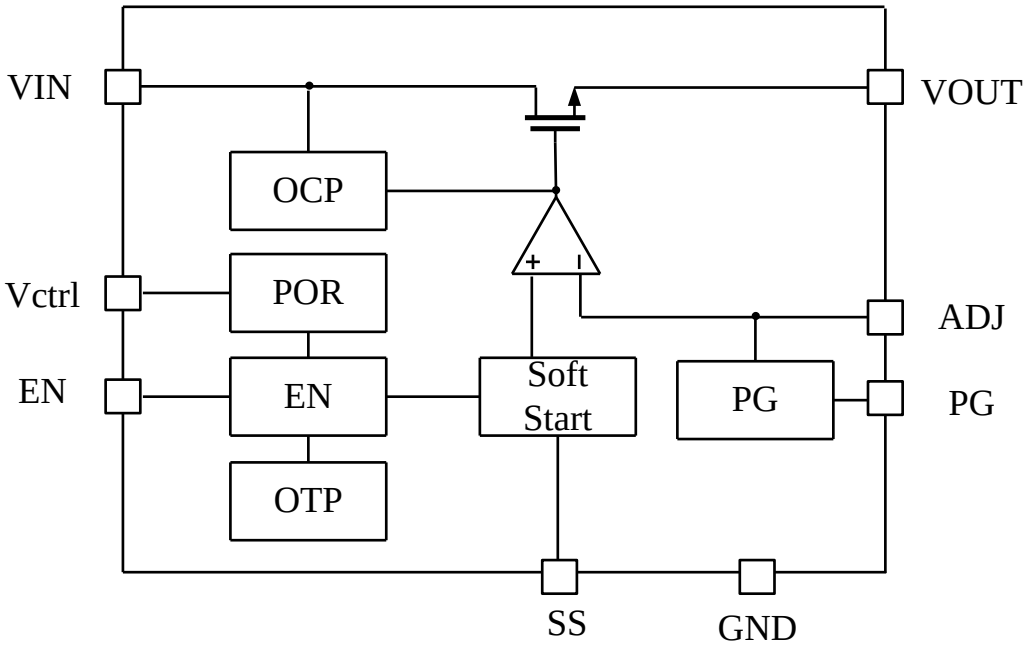


FIG.1. Functional Block Diagram of EMP8161/A

Absolute Maximum Ratings (Notes 1, 2)

Supply voltage (V_{IN} and V_{CTRL})	-0.3V to 7V	Lead Temperature (Soldering, 10 sec.)	260°C
V_{OUT}	-0.3V to 3V	ESD Rating	
I/O pins (PG, EN,ADJ, SS)	-0.3V to VIN+0.3V	- Human Body Model	+-2KV
Power Dissipation	(Note 3)	- Charged device Model	+-500V
Storage Temperature Range	-55°C to 150°C	- Latch-up	+-200mA
Junction Temperature (T_J)	150°C		

Operating Ratings (Note 1, 2)

Supply Voltage (V_{CTRL})	3V to 6V	Operating Temperature Range	-40°C to 85°C
Supply Voltage (VIN)	1V to 5.5V	Junction Operating Temperature	-40°C to 125°C

Note 1: *Absolute Maximum ratings indicate limits beyond which damage may occur. Electrical specifications do not apply when operating the device outside of its rated operating conditions.*

Note 2: *All voltages are with respect to the potential at the ground pin.*

Note 3: *T_J is a function of the ambient temperature T_A and power dissipation P_D ($T_J = T_A + (P_D) * \theta_{JA}$).*

Thermal data

Package	Thermal resistance	Parameter	Value
E-SOP-8L	θ_{JA} (Note 4)	Junction-to-ambient	50°C/W
	$\theta_{JC(top)}$ (Note 5)	Junction-case (top)	39°C/W
	$\theta_{JC(bottom)}$ (Note 6)	Junction-case (bottom)	10°C/W

Note 4: *θ_{JA} is simulated in the natural convection at T_A=25℃ on a highly effective thermal conductivity (thermal land area completed with >3x3cm² area) board (2 layers,2S0P) according to the JEDEC 51-7 thermal measurement standard.*

Note 5: *$\theta_{JC(top)}$ represents the heat resistance between the chip junction and the top surface of package.*

Note 6: *$\theta_{JC(bottom)}$ represents the heat resistance between the chip junction and the center of the exposed pad on the underside of the package.*

Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_A = 25°C, V_{CTRL}=5V, VOUT=0.8V, VIN = VOUT +0.5V, C_{IN} = C_{OUT} =10µF, C_{CTRL}=1µF, C_{SS}=10nF.

Symbol	Parameter	Conditions	Min	Typ (Note7)	Max	Units
V_{CTRL}	Supply voltage for Control Circuit		3.0		6	V
VIN	Supply Voltage Input		1.0		5.5	V
Vout	Vout Range	I_{OUT} = 1A	0.8		V_{CTRL}-1.4V	V
Vref	Reference voltage for ADJ	V_{CTRL}=3V to 5V	0.785	0.8	0.815	V
Vout	Vout accuracy for fixed Vout version	V_{CTRL}=3V to 5V	-2		+2	%

TC	Temperature coefficient	T_A = -40°C~ 125°C, refer to T_A = 25°C	-100	0	100	ppm/°C
I_{OUT}	Maximum Output Current	Average DC Current	1			A
I_{LIMIT}	Output Current Limit	Over-Loading	1.2	1.5		A
I_{Short}	Short Circuit Current			150	500	mA
$I_{Q,VCTRL}$	Supply Current	I_{OUT} = 0.1mA	100	400	550	μA
$I_{SD,VCTRL}$	Shutdown Supply Current (EMP8161)	V_{OUT} = 0V, EN = GND			1	
$I_{SD,VCTRL}$	Shutdown Supply Current (EMP8161A)	V_{OUT} = 0V, EN = GND		14	20	
$I_{Q,VIN}$	Supply Current	I_{OUT} = 0mA, V_{OUT}=0.8V		6.7	12	μA
$I_{SD,VIN}$	Shutdown Supply Current	V_{OUT} = 0V, EN = GND			1	
		V_{OUT} = 0V, EN = GND, T_A=125°C			15	
V_{DO}	Dropout Voltage (Note. 8)	I_{OUT} = 1A, V_{CTRL}=5V, V_{OUT}=0.8V		90	240	mV
ΔV_{OUT}	Line Regulation	I_{OUT} =1mA, (V_{OUT}+0.5V) ≤ V_{CTRL} ≤ 6V		0.1	0.2	%
	Load Regulation	0.1mA ≤ I_{OUT} ≤ 1A		0.5	1	%
V_{EN}	EN Input Threshold	V_{IH}, 3V ≤ V_{CTRL} ≤ 6V	1.2			V
		V_{IL}, 3V ≤ V_{CTRL} ≤ 6V			0.4	
$PSRR_{CVCTRL}$	Power Noise Rejection Ratio	Noise inject on V_{CTRL} at I_{OUT}=1.0A @1kHz		-90		dB
$PSRR_{VIN}$	Power Noise Rejection Ratio	Noise inject on V_{IN} at I_{OUT}=1.0A @1kHz		-80		dB
R_{EN}	EN pull-low resistor	For EMP8161 only	240	400	800	kΩ
	EN pull-high resistor	For EMP8161A only	240	400	800	
T_{SD}	Thermal Shutdown Temperature			170		℃
	Thermal Shutdown Hysteresis			20		
$T_{SS,INT}$	Internal Soft-Start Time	C_{OUT} = 10μF, No C_{SS} V_{OUT} at 95% of Final Value		60		μs
$T_{SS,EXT}$	External Soft-Start Time	C_{OUT} = 10μF, C_{SS}=10nF V_{OUT} at 95% of Final Value	6	10	15	ms
PG_{rising}	Power Good Rising threshold	Vout Rising		92		%
PG_{HYS}	Power Good hysteresis	Vout falling		7		%
PG_{Sink}	Power Good Sink capability	I_{PG}=5mA			0.2	V
PG_{Delay}	Power Good Delay			0.24	1	ms
UV_{CTRL}	Under-Voltage release level	V_{CTRL} Rising	2.6	2.7	2.9	V
$UV_{CTRL,HYS}$	Under-Voltage hysteresis	V_{CTRL} falling		0.2		V
UV_{VIN}	Under-Voltage release level	VIN Rising	0.6	0.75	0.9	V
$UV_{VIN,HYS}$	Under-Voltage hysteresis	VIN falling		0.2		V
R_{DIS}	Vout discharge Resistance		80	130	200	Ω

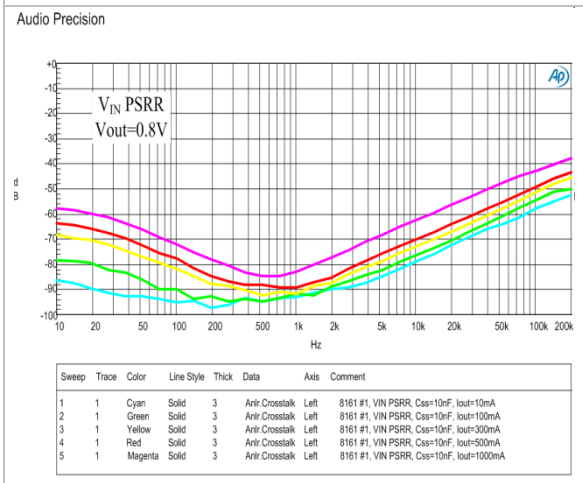
Note 7: *Typical Values represent the most likely parametric norm.*

Note 8: *Dropout voltage is measured by reducing V_{IN} until V_{OUT} drops to 98% its nominal value.*

Typical Performance Characteristics

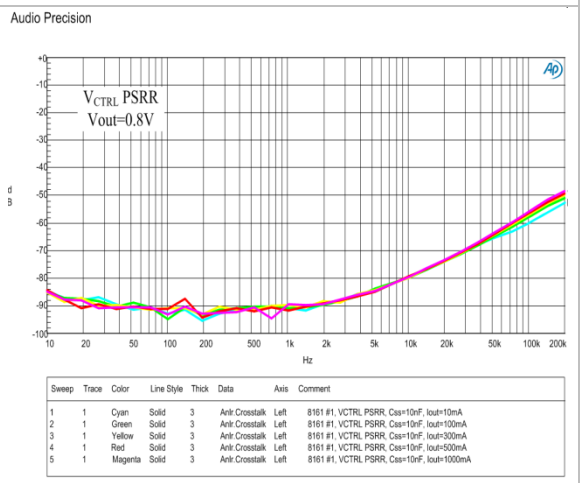
Unless otherwise specified, V_{IN} = $V_{OUT\ (NOM)}$ + 0.5V, V_{CTRL}=5V, Css=10nF, C_{IN} = C_{OUT} = 10μF, C_{CTRL}=1μF, T_A = 25°C.

VIN PSRR vs. Frequency (V_{OUT}=0.8)



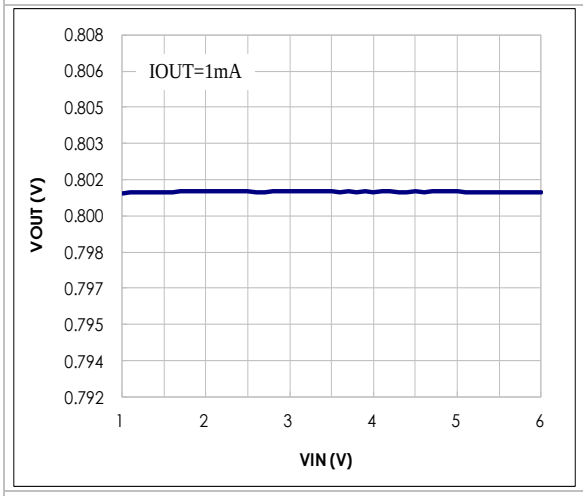
Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Cyan	Solid	3	Anlr.Crosstalk	Left	8161 #1, VIN PSRR, Css=10nF, Iout=10mA
2	1	Green	Solid	3	Anlr.Crosstalk	Left	8161 #1, VIN PSRR, Css=10nF, Iout=100mA
3	1	Yellow	Solid	3	Anlr.Crosstalk	Left	8161 #1, VIN PSRR, Css=10nF, Iout=300mA
4	1	Red	Solid	3	Anlr.Crosstalk	Left	8161 #1, VIN PSRR, Css=10nF, Iout=500mA
5	1	Magenta	Solid	3	Anlr.Crosstalk	Left	8161 #1, VIN PSRR, Css=10nF, Iout=1000mA

VCTRL PSRR vs. Frequency (V_{OUT}=0.8V)

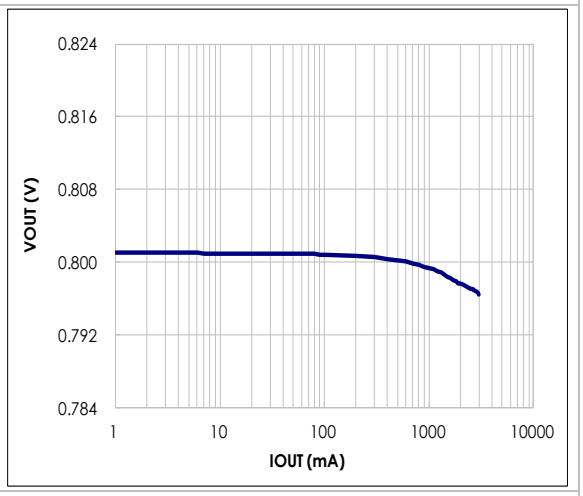


Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Cyan	Solid	3	Anlr.Crosstalk	Left	8161 #1, VCTRL PSRR, Css=10nF, Iout=10mA
2	1	Green	Solid	3	Anlr.Crosstalk	Left	8161 #1, VCTRL PSRR, Css=10nF, Iout=100mA
3	1	Yellow	Solid	3	Anlr.Crosstalk	Left	8161 #1, VCTRL PSRR, Css=10nF, Iout=300mA
4	1	Red	Solid	3	Anlr.Crosstalk	Left	8161 #1, VCTRL PSRR, Css=10nF, Iout=500mA
5	1	Magenta	Solid	3	Anlr.Crosstalk	Left	8161 #1, VCTRL PSRR, Css=10nF, Iout=1000mA

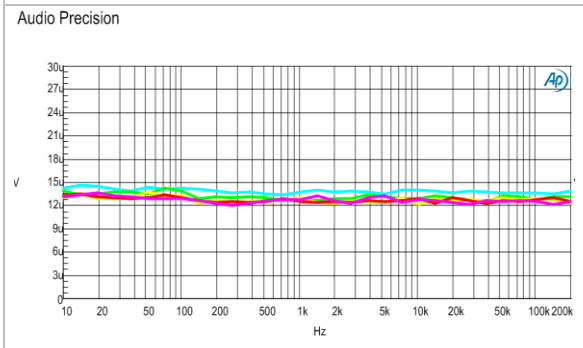
Line Regulation (V_{OUT}=0.8V)



Load Regulation (V_{OUT}=0.8V)

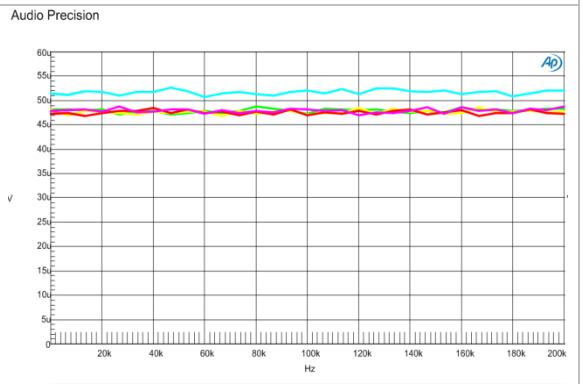


Output Voltage Noise (V_{OUT}=0.8V)



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Cyan	Solid	3	Anlr.Ampl	Left	8161 #1 Noise, Css=10nF, Iout=10mA
2	1	Green	Solid	3	Anlr.Ampl	Left	8161 #1 Noise, Css=10nF, Iout=100mA
3	1	Yellow	Solid	3	Anlr.Ampl	Left	8161 #1 Noise, Css=10nF, Iout=300mA
4	1	Red	Solid	3	Anlr.Ampl	Left	8161 #1 Noise, Css=10nF, Iout=500mA
5	1	Magenta	Solid	3	Anlr.Ampl	Left	8161 #1 Noise, Css=10nF, Iout=1000mA

Output Voltage Noise without C_{SS} (V_{OUT}=0.8V)

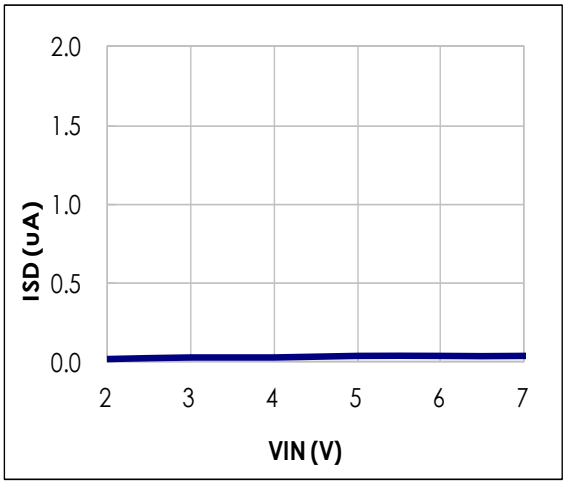


Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Cyan	Solid	3	Anlr.Ampl	Left	8161 #1 Noise, no Css, Iout=10mA
2	1	Green	Solid	3	Anlr.Ampl	Left	8161 #1 Noise, no Css, Iout=100mA
3	1	Yellow	Solid	3	Anlr.Ampl	Left	8161 #1 Noise, no Css, Iout=300mA
4	1	Red	Solid	3	Anlr.Ampl	Left	8161 #1 Noise, no Css, Iout=500mA
5	1	Magenta	Solid	3	Anlr.Ampl	Left	8161 #1 Noise, no Css, Iout=1000mA

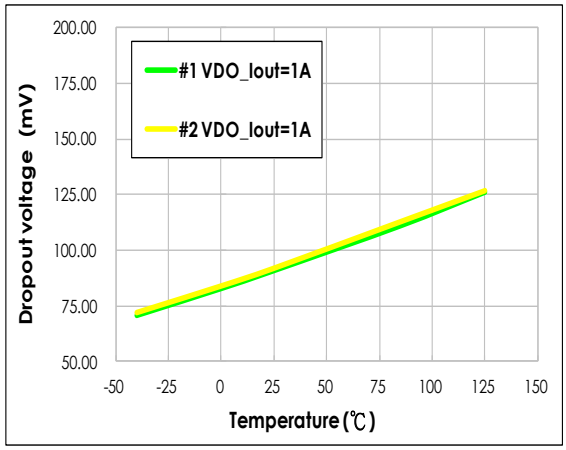
Typical Performance Characteristics (cont.)

Unless otherwise specified, V_{IN} = $V_{OUT\ (NOM)}$ + 0.5V, V_{CTRL}=5V, Css=10nF, C_{IN} = C_{OUT} = 10μF, C_{CTRL}=1μF, T_A = 25°C.

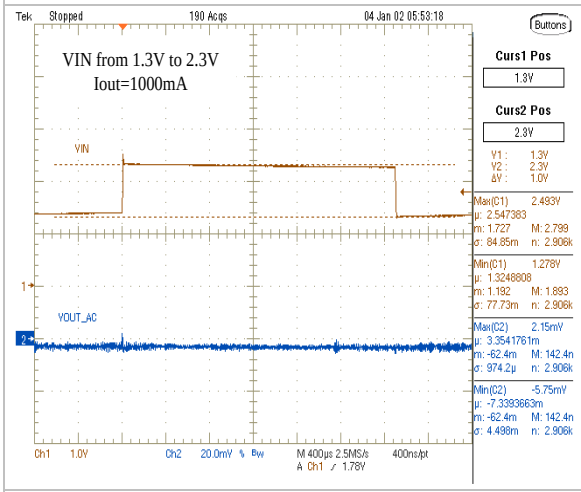
V_{IN} ISD (V_{OUT}=0.8V)



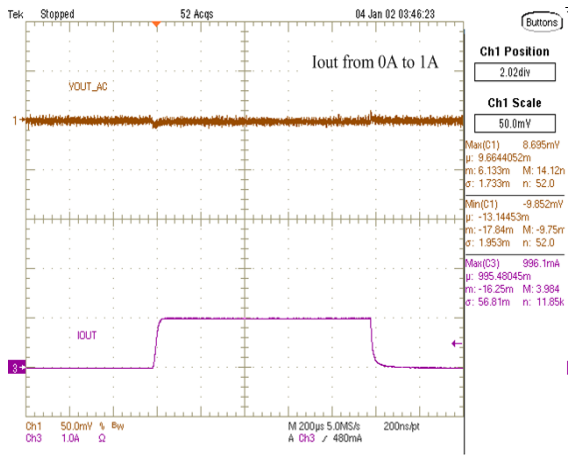
Dropout Voltage (V_{OUT}=0.8V)



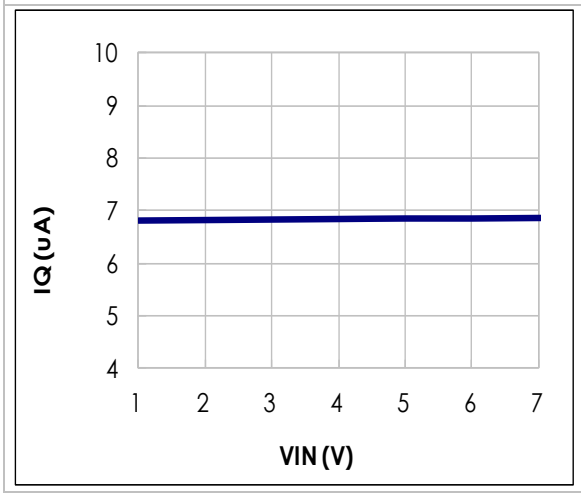
Line transient (Vin=1.3V~2.3V, Iout=1A)



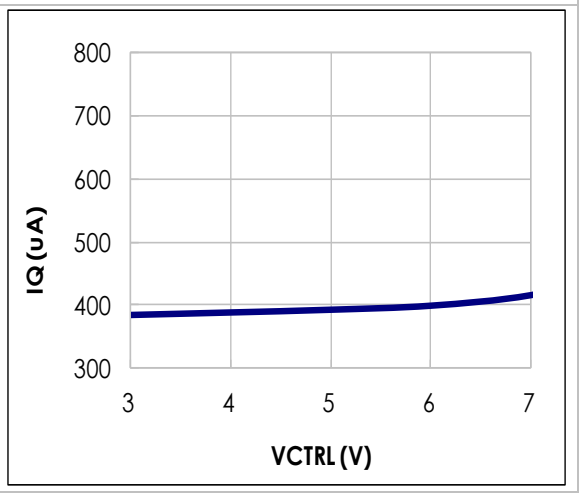
Load transient (V_{OUT}=0.8V, I_{OUT}=0A to 1A)



V_{IN} Iq (V_{OUT}=0.8V)



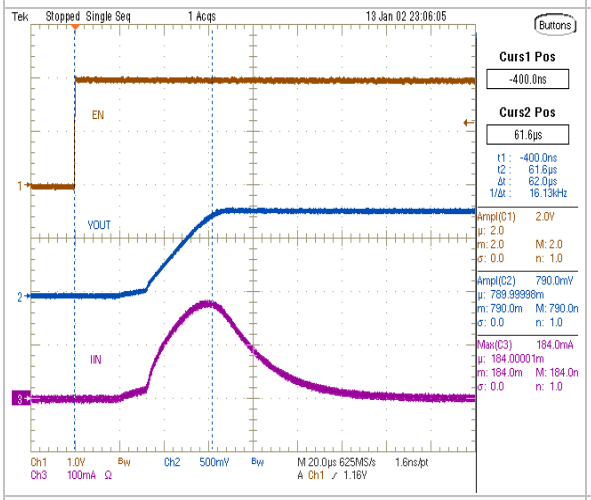
VCRTL Iq (V_{OUT}=0.8V)



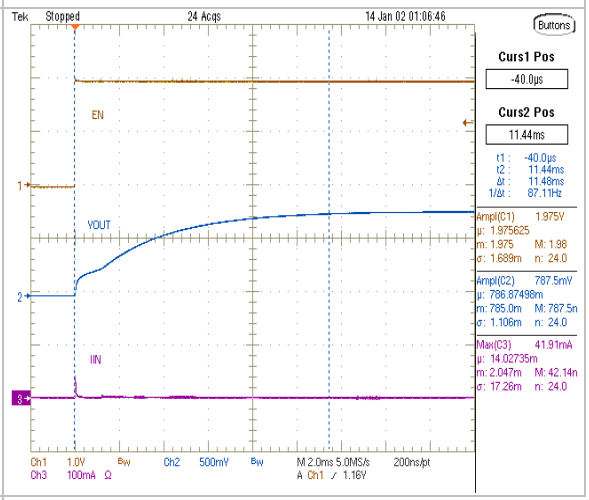
Typical Performance Characteristics (cont.)

Unless otherwise specified, V_{IN} = $V_{OUT\ (NOM)}$ + 0.5V, V_{CTRL}=5V, Css=10nF, C_{IN} = C_{OUT} = 10µF, C_{CTRL}=1µF, T_A = 25°C.

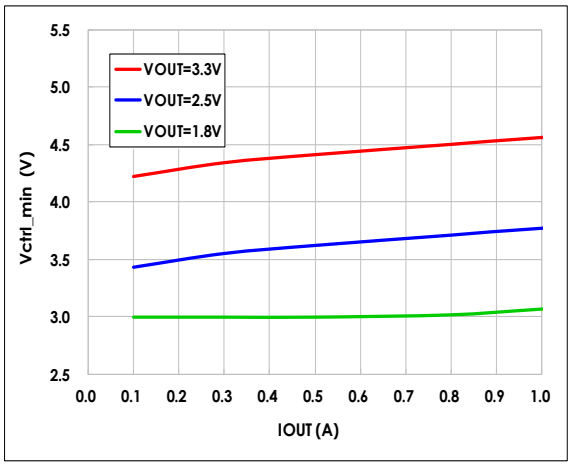
Enable Response, C_{SS}=10nF (V_{OUT}=0.8V)



Enable Response, C_{SS}=10nF (V_{OUT}=0.8V)



Vctrl_min vs. Iout



Application Information

Output Voltage Setting

The output voltage can be calculated by R1 and R2 for ADJ part.

That is given by the following equation:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right) = 0.8 \times \left(1 + \frac{R_1}{R_2}\right)$$

Output Capacitor

The EMP8161/A series are stable with ceramic output capacitors as low as 10uF. Place the capacitor as close as possible to the IC is recommended.

Input Capacitor

The 10uF capacitor from VIN to ground is recommended. And, bypass noise from V_{CTRL} to ground with a 1uF capacitor is for typical operation condition. Place the capacitor as close as possible to the IC is recommended.

Power Dissipation and Thermal Shutdown

The power dissipation is defined as

$$P_D = \left(V_{IN} - V_{OUT}\right) \times I_{OUT} + V_{CTRL} \times I_{Q.VCTRL}$$

The maximum power dissipation depends on the thermal consumption of IC package, PCB material & PCB design (The copper area of thermal pad) and the junction to ambient thermal resistance and the rate of surrounding airflow.

The maximum power dissipation can be calculated by the following formula:

$$P_{D(Max.)} = \frac{\left(T_J - T_A\right)}{\theta_{JA}}$$

Where T_J is the maximum operation junction temperature, 125°C

Enable

The enable pin (EN) of the EMP8161 is pulled down by an internal 400kohm resister. The EN pin is in the logic low when VEN<0.4V or floating, the regulator will be shut down, and the shutdown current is less than 1uA, both for V_{CTRL} and V_{IN}. The EN pin is in the logic high when VEN>1.2V, the regulator will be enabled and restarts a soft-start cycle. The other one option, the enable pin of the EMP8161A is pulled up with a 400kohm resister internally, and the shutdown current of V_{CTRL} is around 14uA.

Power Good indicator

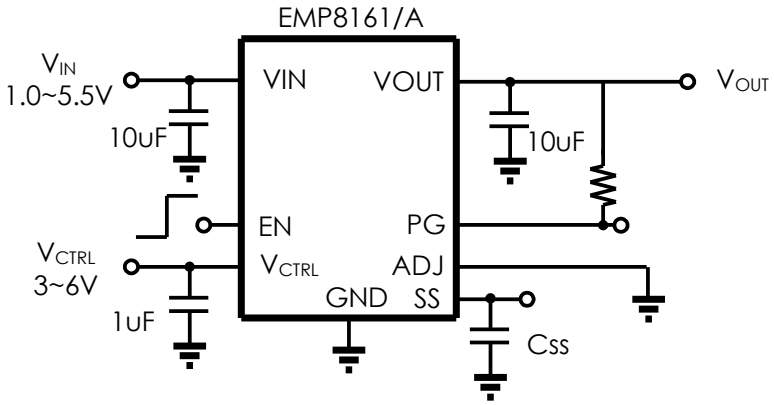
The power good (PG) pin is an open-drain output. Usually, it is connected to Vout or other pin which has ability to drive this pin through an external pull-up resistor. The PG pin will be high if the output is good enough. As the output voltage arrives 92% of the desired value, the PG pin will be high after a 60us delay time. As the output voltage or supply voltages fall lower than the falling threshold respectively, the PG pin will be low immediately.

Soft-start time

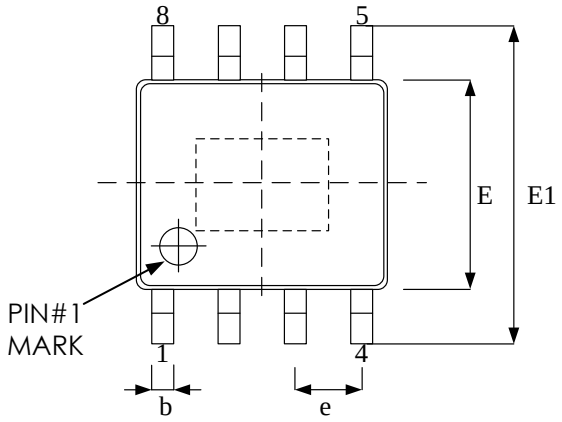
The EMP8161/A series have an internal soft start time is about 60us during the output voltage from 0% to 95% and an external soft start time could be calculated by the function Tss (sec.). The following shows how to choose a soft start capacitor and build an expected start time. The R_{SS} is 220KΩ designed in chip internally. Tss is ~0.95ms if Css is 1nF adopted.

$$T_{SS(\sec.)} \cong 4.3 \times R_{SS} \times C_{SS} \cong 4.3 \times 220K \times C_{SS}$$

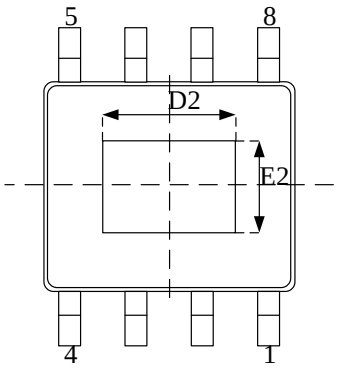
Application Circuit for Fixed output



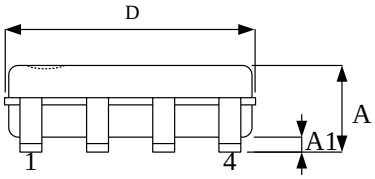
Package Outline Drawing
E-SOP-8L (150 mil)



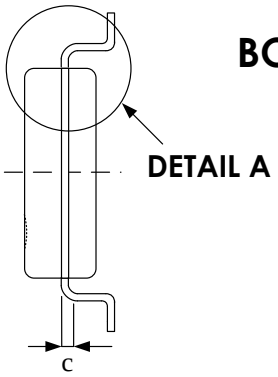
TOP VIEW

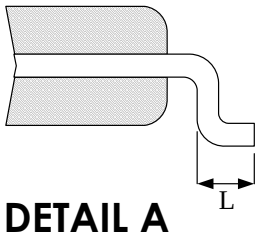


BOTTOM VIEW



SIDE VIEW





DETAIL A

Symbol	Dimension in mm	
	Min	Max
A	-	1.70
A1	0.00	0.15
b	0.31	0.51
c	0.10	0.25
D	4.80	5.00
E	3.81	4.00
E1	5.79	6.20
e	1.27 BSC	
L	0.40	1.27

Exposed pad

	Dimension in mm	
	Min	Max
D2	2.80	3.50
E2	2.00	2.60

Revision History

Revision	Date	Description
0.1	2018.06.13	Initial version.
0.2	2018.09.05	1. $T_{SS,INT}$ change to 60us. 2. PG_{Delay} change to 0.24ms. 3. Add $T_{SS,INT}$ waveform.
0.3	2018.09.14	1. Modify order information description. 2. Remove EMP8161 and EMP8161A E-SOP-8L ADJ version package information.
0.4	2018.10.08	1. Changed the description EMP8161 to EMP8161/A. 2. Title changed to "1A Ultra Low Dropout Voltage Regulator with Internal Soft-Start (60uS)". 3. Added "Note. The product ID. not listed in above, that's by request." Into order information. 4. Added device comparison table. 5. Added application circuit for fixed output.
0.5	2019.01.25	1. Revised the Exposed pad table.
0.6	2019.03.06	1.Add new product ID
0.7	2020.02.18	1.Revise Vout range spec. 2.Add Vctrl_min vs. Iout measurement plot.
1.0	2021.01.15	1.Remove preliminary symbol
1.1	2021.07.13	Modify E-SOP-8 Dimension

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