

3A Ultra Low Dropout Voltage Regulator with Internal Soft-Start (600uS)

General Description

The EMP8175/A series can drive 3A of continuous output loading and provide a good performance with a typical dropout voltage as 280mV through an internal n-channel power MOSFETs. The output voltage can be adjustable from 0.8V to V_{out} that could be very close to V_{in} .

There are two power supplies pins for the linear regulator. The control circuitry in this linear regulator requires a supply V_{CTRL} and the driver, the n-channel MOSFET, uses another one.

The EMP8175/A series provide a stable output voltage with an output capacitor as low as 10uF. In order to prevent the linear regulator get damage from thermal increasing, the EMP8175/A series provide fold-back over loading protection and over temperature protection features. An internal soft-start or adjustable soft-start by SS pin can minimizes capacitive inrush current on the input power source during start-up. PG stay low until the output reaches 92% of value that is settled during start-up.

The EMP8175/A series are available in E-SOP-8L package.

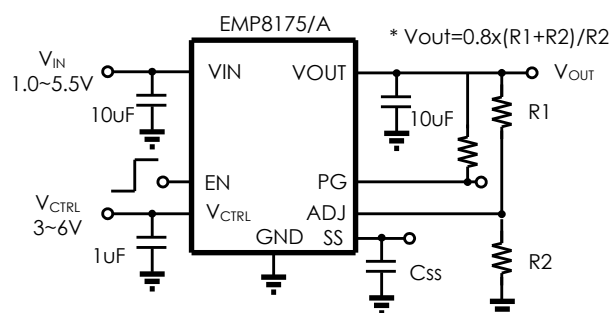
Applications

- High Efficiency Linear Regulators
- DSP Core and I/O Voltage
- Post Regulator for Switching Power

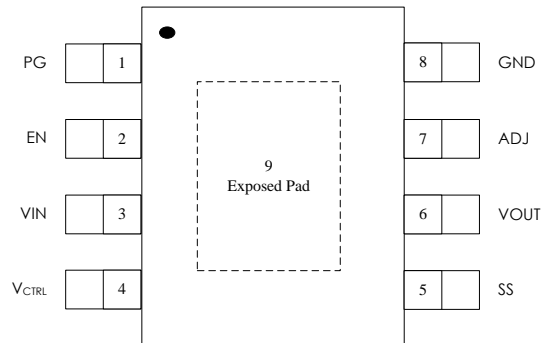
Features

- Input Voltage Range : +1.0V to +5.5V
- Maximum Output Current : 3A
- RDS-on: 95mohm
- Dropout Voltage : 280mV @ $I_{out}=3A$
($V_{out}=0.8V$, $V_{CTRL}=5V$)
- $\pm 2\%$ Output Voltage Accuracy
- High Ripple Rejection : >60 dB @ $I_{out}=1.5A$
($V_{out}=0.8V$, $V_{CTRL}=5V$, $C_{SS}=10nF$)
- Fold back short circuit protection
- Thermal Overload Shutdown Protection
- Under Voltage Protection
- Power Good Indicator (Open-Drain)
- Internal soft-start 600uS
- Soft-Start Pin Provides Startup with Ramp Time Set by External Capacitor

Typical Application



Connection Diagrams



Order Information

EMP8175#-XXSG08NRR

Null: EN pin with pull-low resistor

A: EN pin with pull-high resistor

XX Output voltage version

Example,

00, Output Voltage adjustable

12, Output Voltage 1.2V

33, Output Voltage 3.3V

SG08 E-SOP-8L Package (Package Code)

NRR RoHS & Halogen free package

Commercial Grade Temperature

Rating: -40 to 85°C

Package in Tape & Reel

Order, Marking & Packing Information

Package	Vout	EN Resister	Product ID.	Marking	Packing
E-SOP-8L	ADJ	Pull-low	EMP8175-00SG08NRR		Tape & Reel 3kpcs
E-SOP-8L	ADJ	Pull-high	EMP8175A-00SG08NRR		Tape & Reel 3kpcs

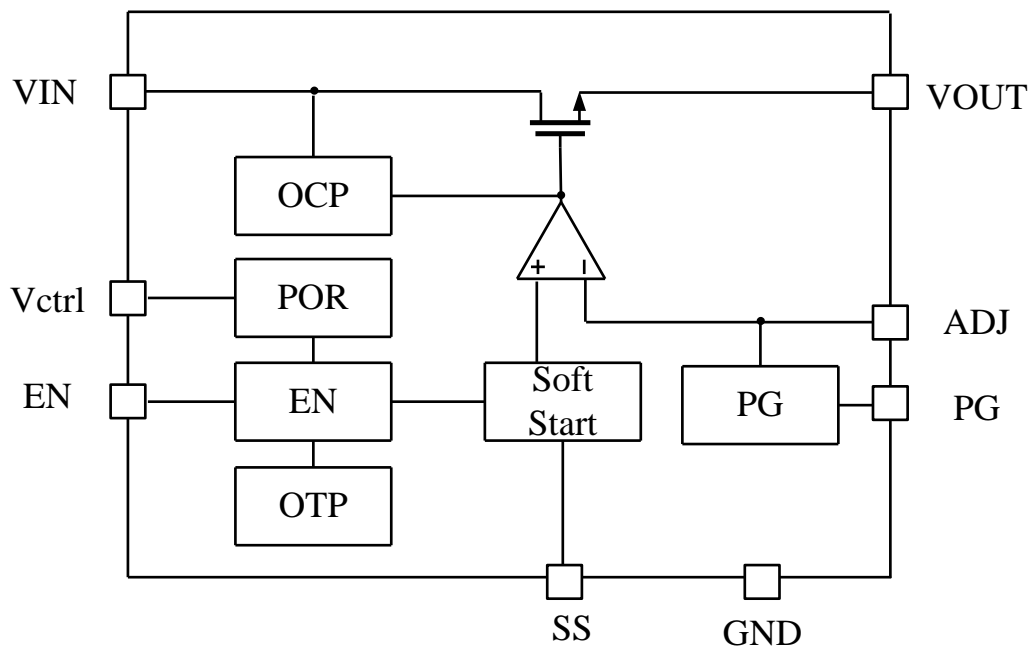
Note. The product ID. not listed in above, that's by request.

Device comparison table

Product	Iout	EN state in Chip Internally	Soft-Start time in chip internally
EMP8161	1A	With pull low Resistor	60uS
EMP8161A	1A	With pull high Resistor	60uS
EMP8166	1A	With pull low Resistor	600uS
EMP8166A	1A	With pull high Resistor	600uS
EMP8160	2A	With pull low Resistor	60uS
EMP8160A	2A	With pull high Resistor	60uS
EMP8165	2A	With pull low Resistor	600uS
EMP8165A	2A	With pull high Resistor	600uS
EMP8170	3A	With pull low Resistor	60uS
EMP8170A	3A	With pull high Resistor	60uS
EMP8175	3A	With pull low Resistor	600uS
EMP8175A	3A	With pull high Resistor	600uS

Pin Functions

Name	E-SOP-8L	Function
PG	1	Power Good Indicator.
EN	2	Enable Input. Enable the regulator by pulling the EN pin High. Set the regulator into the disable mode by pulling the EN pin low. The EN pin is with pull low 400kohm resistor internally for EMP8175 (with pull high 400kohm internally for EMP8175A).
VIN	3	Supply Voltage Input. Require a minimum input capacitor of close to 10 μ F to ensure stability and sufficient decoupling from the ground pin.
V _{CTRL}	4	Supply Voltage for Control Circuit.
SS	5	Soft-Start. Connect a 1~10nF capacitor between this pin and GND to reduce inrush current during start-up.
VOUT	6	Output Voltage.
ADJ	7	Adjust Vout. Feedback input. Connect to resistive voltage-divider network. * ADJ connected to GND for Fixed Vout.
GND	8	Ground Pin.
Exposed Pad	9	Thermal Pad This pin must be connected to ground. The thermal pad with large thermal land area on the PCB will helpful chip power dissipation.

Functional Block Diagram**FIG.1. Functional Block Diagram of EMP8175/A**

Absolute Maximum Ratings (Notes 1, 2)

Supply voltage (V_{IN} and V_{CTRL})	-0.3V to 7V	Lead Temperature (Soldering, 10 sec.)	260°C
V_{OUT}	-0.3V to 3V	ESD Rating	
I/O pins (PG, EN, ADJ, SS)	-0.3V to $V_{IN}+0.3V$	- Human Body Model	+2KV
Power Dissipation	(Note 3)	- Charged device Model	+500V
Storage Temperature Range	-55°C to 150°C	- Latch-up	+200mA
Junction Temperature (T_J)	150°C		

Operating Ratings (Note 1, 2)

Supply Voltage (V_{CTRL})	3V to 6V	Operating Temperature Range	-40°C to 85°C
Supply Voltage (V_{IN})	1V to 5.5V	Junction Operating Temperature	-40°C to 125°C

Note 1: Absolute Maximum ratings indicate limits beyond which damage may occur. Electrical specifications do not apply when operating the device outside of its rated operating conditions.

Note 2: All voltages are with respect to the potential at the ground pin.

Note 3: T_J is a function of the ambient temperature T_A and power dissipation P_D ($T_J = T_A + (P_D) \cdot \theta_{JA}$)).

Thermal data

Package	Thermal resistance	Parameter	Value
E-SOP-8L	θ_{JA} (Note 4)	Junction-to-ambient	50°C/W
	$\theta_{JC(top)}$ (Note 5)	Junction-case (top)	39°C/W
	$\theta_{JC(bottom)}$ (Note 6)	Junction-case (bottom)	10°C/W

Note 4: θ_{JA} is simulated in the natural convection at $T_A=25^\circ\text{C}$ on a highly effective thermal conductivity (thermal land area completed with $>3\times 3\text{cm}^2$ area) board (2 layers, 2S0P) according to the JEDEC 51-7 thermal measurement standard.

Note 5: $\theta_{JC(top)}$ represents the heat resistance between the chip junction and the top surface of package.

Note 6: $\theta_{JC(bottom)}$ represents the heat resistance between the chip junction and the center of the exposed pad on the underside of the package.

Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_A = 25^\circ\text{C}$, $V_{CTRL}=5V$, $V_{OUT}=0.8V$, $V_{IN} = V_{OUT} + 0.5V$, $C_{IN} = C_{OUT} = 10\mu\text{F}$, $C_{CTRL}=1\mu\text{F}$, $C_{SS}=10\text{nF}$.

Symbol	Parameter	Conditions	Min	Typ (Note7)	Max	Units
V_{CTRL}	Supply voltage for Control Circuit		3.0		6	V
V_{IN}	Supply Voltage Input		1.0		5.5	V
V_{out}	V_{out} Range	$I_{OUT} = 3A$	0.8		$V_{CTRL}-2.2V$	V
V_{ref}	Reference voltage for ADJ	$V_{CTRL}=3V$ to $5V$	0.785	0.8	0.815	V
V_{out}	V_{out} accuracy for fixed	$V_{CTRL}=3V$ to $5V$	-2		+2	%

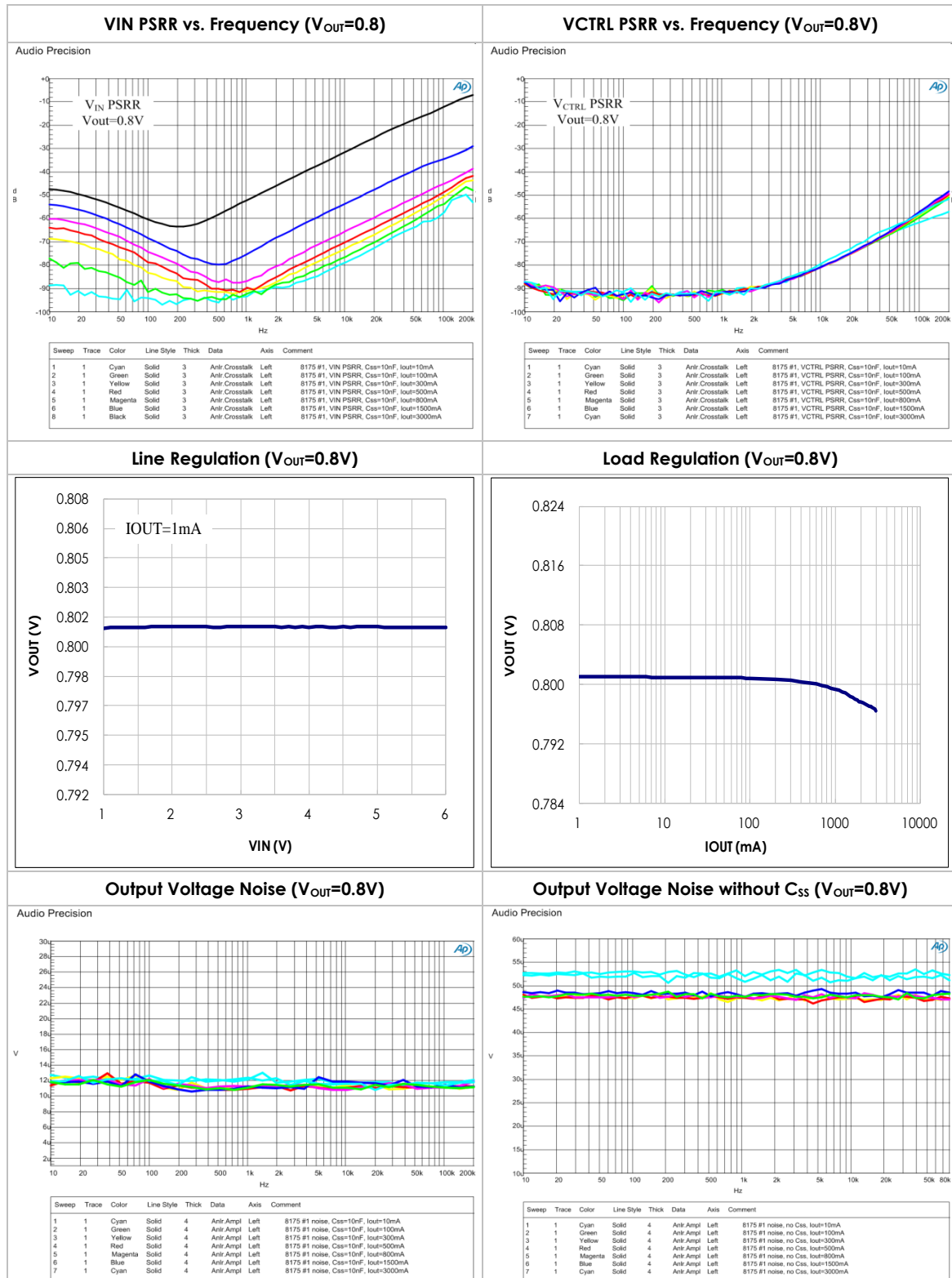
	Vout version					
TC	Temperature coefficient	T _A = -40°C~ 125°C, refer to T _A = 25°C	-100	0	100	ppm/°C
I _{OUT}	Maximum Output Current	Average DC Current	3			A
I _{LIMIT}	Output Current Limit	Over-Loading	3.5	4.2		A
I _{Short}	Short Circuit Current			150	500	mA
I _{SD,VCTRL}	Shutdown Supply Current (EMP8175)	V _{OUT} = 0V, EN = GND			1	μA
I _{SD,VCTRL}	Shutdown Supply Current (EMP8175A)	V _{OUT} = 0V, EN = GND		14	20	
I _{Q,VIN}	Supply Current	I _{OUT} = 0mA, V _{OUT} =0.8V		6.7	12	
I _{Q,VIN}	Supply Current	I _{OUT} = 0mA, V _{OUT} =1.2V		5	10	μA
I _{SD,VIN}	Shutdown Supply Current	V _{OUT} = 0V, EN = GND			1	
		V _{OUT} = 0V, EN = GND, T _A =125°C			15	
V _{DO}	Dropout Voltage (Note. 8)	I _{OUT} = 3A, V _{CTRL} =5V, V _{OUT} =0.8V		280	460	mV
ΔV _{OUT}	Line Regulation	I _{OUT} = 1mA, (V _{OUT} +0.5V) ≤ V _{CTRL} ≤ 6V		0.1	0.2	%
	Load Regulation	0.1mA ≤ I _{OUT} ≤ 3A		0.5	1	%
V _{EN}	EN Input Threshold	V _{IH} , 3V ≤ V _{CTRL} ≤ 6V	1.2			V
		V _{IL} , 3V ≤ V _{CTRL} ≤ 6V			0.4	
PSRR _{VCTRL}	Power Noise Rejection Ratio	Noise inject on V _{CTRL} at I _{OUT} =1.5A @1kHz		-90		dB
PSRR _{VIN}	Power Noise Rejection Ratio	Noise inject on V _{VIN} at I _{OUT} =1.5A @1kHz		-75		dB
R _{EN}	EN pull-low resistor	For EMP8175 only	240	400	800	kΩ
	EN pull-high resistor	For EMP8175A only	240	400	800	
T _{SD}	Thermal Shutdown Temperature			170		°C
	Thermal Shutdown Hysteresis			20		
T _{SS,INT}	Internal Soft-Start Time	C _{OUT} = 10μF, No C _{SS} V _{OUT} at 95% of Final Value		600		μs
T _{SS,EXT}	External Soft-Start Time	C _{OUT} = 10μF, C _{SS} =10nF V _{OUT} at 95% of Final Value	6	10	15	ms
PG _{rising}	Power Good Rising threshold	Vout Rising		92		%
PG _{HYS}	Power Good hysteresis	Vout falling		7		%
PG _{Sink}	Power Good Sink capability	I _{PG} =5mA			0.2	V
PG _{Delay}	Power Good Delay			0.24	1	ms
UV _{CTRL}	Under-Voltage release level	V _{CTRL} Rising	2.6	2.7	2.9	V
UV _{CTRL,HYS}	Under-Voltage hysteresis	V _{CTRL} falling		0.2		V
UV _{VIN}	Under-Voltage release level	V _{VIN} Rising	0.6	0.75	0.9	V
UV _{VIN,HYS}	Under-Voltage hysteresis	V _{VIN} falling		0.2		V
R _{DIS}	Vout discharge Resistance		80	130	200	Ω

Note 7: Typical Values represent the most likely parametric norm.

Note 8: Dropout voltage is measured by reducing V_{VIN} until V_{OUT} drops to 98% its nominal value.

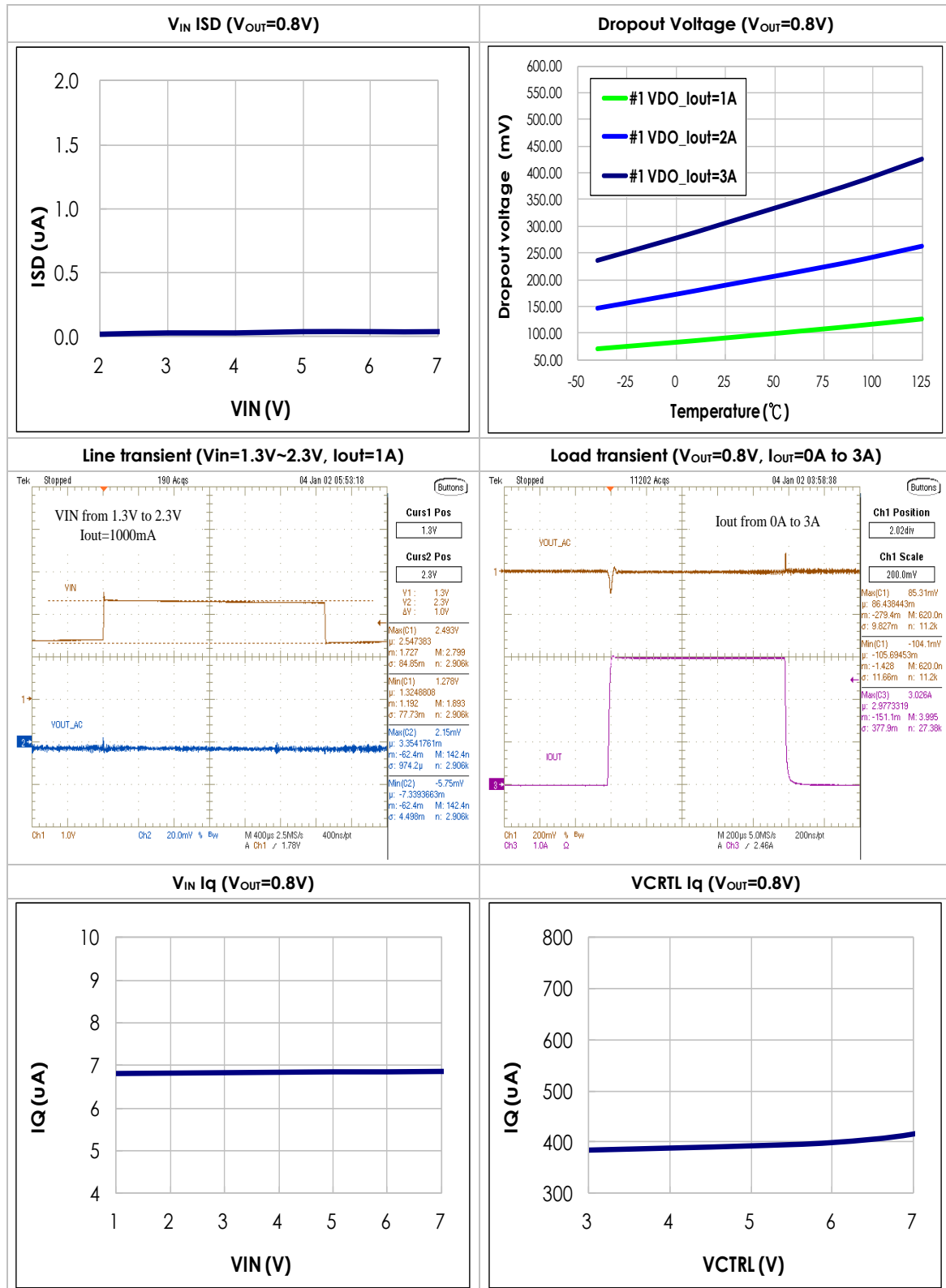
Typical Performance Characteristics

Unless otherwise specified, $V_{IN} = V_{OUT(NOM)} + 0.5V$, $V_{CTRL} = 5V$, $C_{SS} = 10nF$, $C_{IN} = C_{OUT} = 10\mu F$, $C_{CTRL} = 1\mu F$, $T_A = 25^\circ C$.



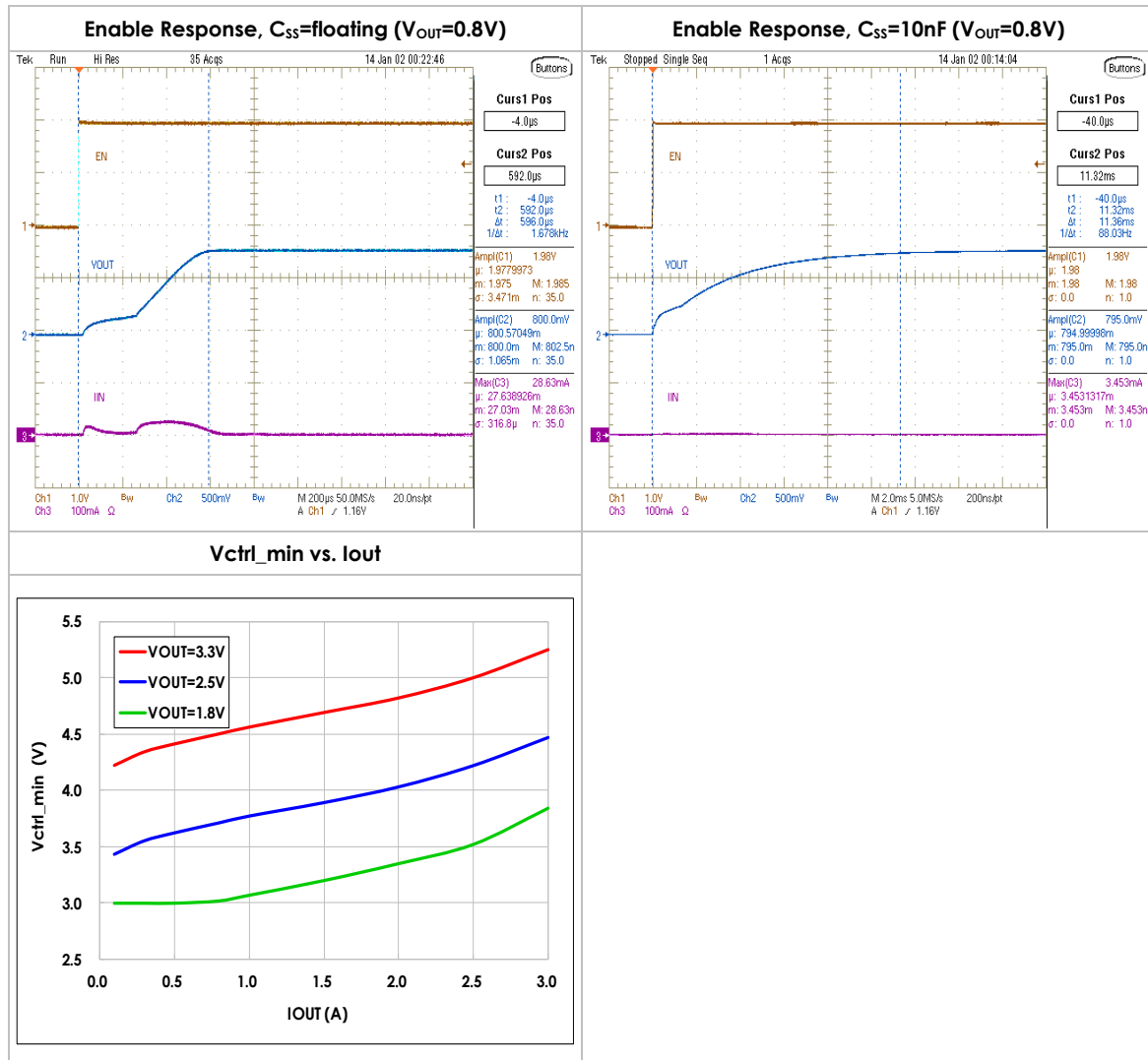
Typical Performance Characteristics (cont.)

Unless otherwise specified, $V_{IN} = V_{OUT(NOM)} + 0.5V$, $V_{CTRL}=5V$, $C_{SS}=10nF$, $C_{IN} = C_{OUT} = 10\mu F$, $C_{CTRL}=1\mu F$, $T_A = 25^\circ C$.



Typical Performance Characteristics (cont.)

Unless otherwise specified, $V_{IN} = V_{OUT(NOM)} + 0.5V$, $V_{CTRL}=5V$, $C_{SS}=10nF$, $C_{IN} = C_{OUT} = 10\mu F$, $C_{CTRL}=1\mu F$, $T_A = 25^\circ C$.



Application Information

Output Voltage Setting

The output voltage can be calculated by R1 and R2 for ADJ part.

That is given by the following equation:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right) = 0.8 \times \left(1 + \frac{R_1}{R_2}\right)$$

Output Capacitor

The EMP8175/A series are stable with ceramic output capacitors as low as 10uF. Place the capacitor as close as possible to the IC is recommended.

Input Capacitor

The 10uF capacitor from VIN to ground is recommended. And, bypass noise from V_{CTRL} to ground with a 1uF capacitor is for typical operation condition. Place the capacitor as close as possible to the IC is recommended.

Power Dissipation and Thermal Shutdown

The power dissipation is defined as

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{CTRL} \times I_{Q.VCTRL}$$

The maximum power dissipation depends on the thermal consumption of IC package, PCB material & PCB design (The copper area of thermal pad) and the junction to ambient thermal resistance and the rate of surrounding airflow.

The maximum power dissipation can be calculated by the following formula:

$$P_{D(Max)} = \frac{(T_J - T_A)}{\theta_{JA}}$$

Where T_J is the maximum operation junction temperature, 125°C

Enable

The enable pin (EN) of the EMP8175 is pulled down by an internal 400kohm resistor. The EN pin is in the logic low when $V_{EN} < 0.4V$ or floating, the regulator will be shut down, and the shutdown current is less than 1uA, both for V_{CTRL} and V_{IN} . The EN pin is in the logic high when $V_{EN} > 1.2V$, the regulator will be enabled and restarts a soft-start cycle. The other one option, the enable pin of the EMP8175A is pulled up with a 400kohm resistor internally, and the shutdown current of V_{CTRL} is around 14uA.

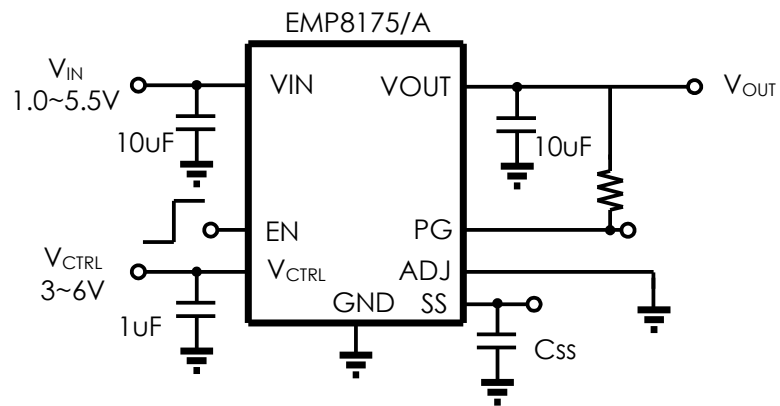
Power Good indicator

The power good (PG) pin is an open-drain output. Usually, it is connected to V_{out} or other pin which has ability to drive this pin through an external pull-up resistor. The PG pin will be high if the output is good enough. As the output voltage arrives 92% of the desired value, the PG pin will be high after a 600uS delay time. As the output voltage or supply voltages fall lower than the falling threshold respectively, the PG pin will be low immediately.

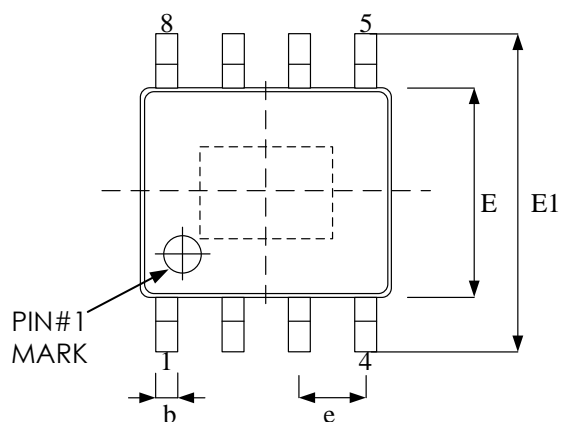
Soft-start time

The EMP8175/A series have an internal soft start time is about 600uS during the output voltage from 0% to 95% and an external soft start time could be calculated by the function T_{ss} (sec.). The following shows how to choose a soft start capacitor and build an expected start time. The R_{ss} is 220KΩ designed in chip internally. T_{ss} is ~0.95ms if C_{ss} is 1nF adopted.

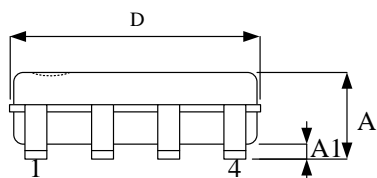
$$T_{ss(\text{sec.})} \cong 4.3 \times R_{ss} \times C_{ss} \cong 4.3 \times 220K \times C_{ss}$$

Application Circuit for Fixed output

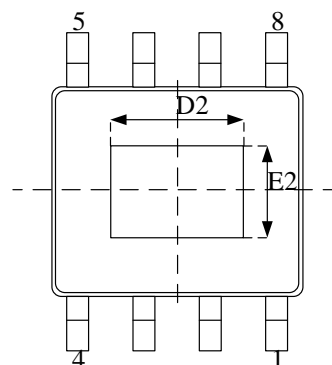
Package Outline Drawing E-SOP-8L (150 mil)



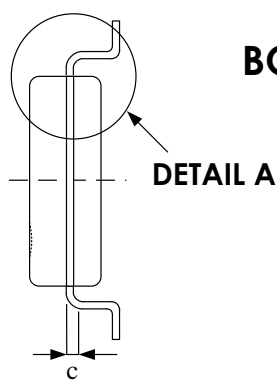
TOP VIEW



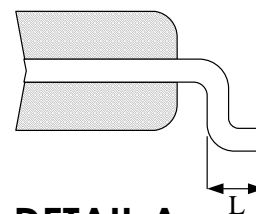
SIDE VIEW



BOTTOM VIEW



DETAIL A



DETAIL A

Symbol	Dimension in mm	
	Min	Max
A	-	1.70
A1	0.00	0.15
b	0.31	0.51
c	0.10	0.25
D	4.80	5.00
E	3.81	4.00
E1	5.79	6.20
e	1.27 BSC	
L	0.40	1.27

Exposed pad

	Dimension in mm	
	Min	Max
D2	2.80	3.50
E2	2.00	2.60

Revision History

Revision	Date	Description
0.1	2018.06.06	Initial version.
0.2	2018.07.09	1. EN PIN description modify. 2. Add ISD_{VCTRL} spec for EMP8175 and EMP8175A. 3. Modify I_{QVIN} target and spec high. 4. Add EMP8175A mean of ISD_{VCTRL} description.
0.3	2018.09.05	1. $T_{SS,INT}$ change to 600us. 2. PG_{Delay} change to 0.24ms. 3. Modify $T_{SS,INT}$ waveform.
0.4	2018.09.07	1. Modify order information description - Page.2. 2. Remove EMP8175 and EMP8175A E-SOP-8L ADJ version package information - Page.3.
0.5	2017.10.25	1. Changed the description EMP8175 to EMP8175/A. 2. Title changed to "3A Ultra Low Dropout Voltage Regulator with Internal Soft-Start (600uS)". 3. Added "Note. The product ID. not listed in above, that's by request." Into order information. 4. Added device comparison table. 5. Added application circuit for fixed output.
0.6	2019.01.31	1. Revised the Exposed pad table.
0.7	2019.03.06	1 Add new product ID
0.8	2020.03.03	1.Revise V_{out} range spec. 2.Add V_{ctrl_min} vs. I_{out} measurement plot.
1.0	2021.01.15	1.Remove preliminary symbol
1.1	2021.07.14	Modify E-SOP-8 Dimension

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