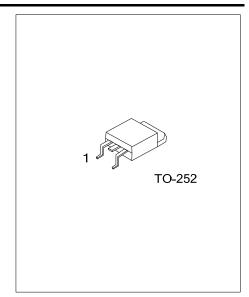
F5N50K-TC Power MOSFET

5.0A, 500V N-CHANNEL POWER MOSFET

■ DESCRIPTION

The UTC **F5N50K-TC** is a N-channel power MOSFET adopting UTC's advanced technology to provide customers with DMOS, planar stripe technology. This technology is designed to meet the requirements of the minimum on-state resistance and perfect switching performance. It also can withstand high energy pulse in the avalanche and communication mode.

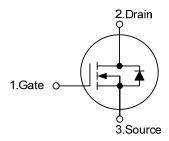
The UTC **F5N50K-TC** can be used in applications, such as active power factor correction, high efficiency switched mode power supplies, electronic lamp ballasts based on half bridge topology.



■ FFATURES

- * $R_{DS(ON)} \le 1.8\Omega$ @ $V_{GS}=10V$, $I_{D}=2.5A$
- * 100% avalanche tested
- * High switching speed

■ SYMBOL



■ ORDERING INFORMATION

Note: Pin Assignment: G: Gate

Ordering Number		Doolsons	Pin Assignment			Docking	
Lead Free	Halogen Free	Package	1	2	3	Packing	
F5N50KL-TN3-R	F5N50KG-TN3-R	TO-252	G	D	S	Tape Reel	

S: Source

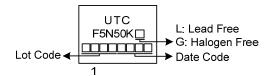
D: Drain

F5N50KG-TN3-R
(1)Packing Type
(1) R: Tape Reel
(2) TN3: TO-252
(3) G: Halogen Free and Lead Free, L: Lead Free

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F5N50K-TC **Power MOSFET**

MARKING





F5N50K-TC **Power MOSFET**

ABSOLUTE MAXIMUM RATINGS (T_C=25°C, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	500	V
Gate-Source Voltage		V_{GSS}	±30	V
Drain Current	Continuous	I _D 5		Α
	Pulsed (Note 2)	I_{DM}	20	Α
Avalanche Energy	anche Energy Single Pulsed (Note 3)		104	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	6.3	V/ns
Power Dissipation		P_D	54	W
Junction Temperature		T_J	+150	°C
Storage Temperature		T_{STG}	-55 ~ + 150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

- 2. Repetitive Rating: Pulse width limited by maximum junction temperature
- 3. L = 16mH, I_{AS} = 3.6A, V_{DD} = 50V, R_G = 25 Ω , Starting T_J = 25 $^{\circ}$ C
- 4. $I_{SD} \le 5.0A$, di/dt $\le 200A/\mu s$, $V_{DD} \le BV_{DSS}$, Starting $T_J = 25^{\circ}C$

THERMAL DATA

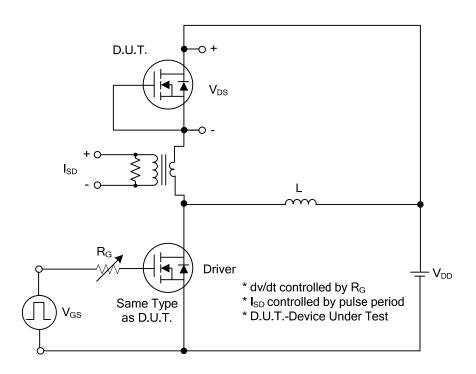
PARAMETER	SYMBOL	RATINGS	UNIT	
Junction to Ambient	θ_{JA}	110	°C/W	
Junction to Case	θ _{JC}	2.3	°C/W	

ELECTRICAL CHARACTERISTICS (T_J =25°C, unless otherwise specified)

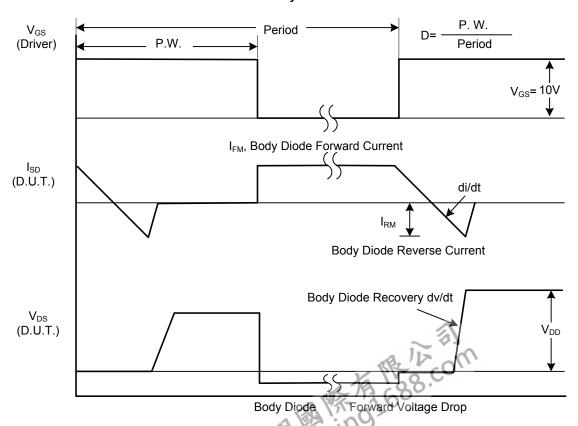
PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV_{DSS}	$I_D=250\mu A, V_{GS}=0V$	500			V
Drain-Source Leakage Current		I_{DSS}	V _{DS} =500V, V _{GS} =0V			1	μΑ
Gate- Source Leakage Current	Forward		V_{GS} =30V, V_{DS} =0V			100	nA
	Reverse	I _{GSS}	V_{GS} =-30V, V_{DS} =0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		$V_{GS(TH)}$	$V_{DS}=V_{GS}$, $I_D=250\mu A$			4.0	V
Static Drain-Source On-State Resistance		R _{DS(ON)}	V _{GS} =10V, I _D =2.5A			1.8	Ω
DYNAMIC PARAMETERS							
Input Capacitance		C _{ISS})/)/ -0)/)/ -25)/		585		pF
Output Capacitance		Coss	V V _{GS} =0V,V _{DS} =25V, -f=1.0MHz		58		pF
Reverse Transfer Capacitance		C_{RSS}	1-1.01011 12		7.0		pF
SWITCHING PARAMETERS							
Total Gate Charge (Note 1)		Q_G	V _{DS} =200V, V _{GS} =10V, I _D =5.0A		5.2		nC
Gate to Source Charge		Q_GS	I_{G} =1mA (Note 1, 2)		2.8		nC
Gate to Drain Charge		Q_GD	IG-IIIA (Note 1, 2)		1.1		nC
Turn-ON Delay Time (Note 1)		$t_{D(ON)}$			7.6		ns
Rise Time		t_R	V_{DD} =30V, V_{GS} =10V, $_{D}$ =0.75A,		18.6		ns
Turn-OFF Delay Time		t _{D(OFF)}	$R_G = 25\Omega$ (Note 1, 2)		36		ns
Fall-Time		t_{F}			18		ns
SOURCE- DRAIN DIODE RATI	NGS AND CH	ARACTERIST	ics				
Maximum Body-Diode Continuous Current		I _S	~ 43			5	Α
Maximum Body-Diode Pulsed Current		I _{SM}	THE COL	/ ,		20	Α
Drain-Source Diode Forward Voltage (Note 1)		V_{SD}	I _S =5.0A, V _{GS} =0V			1.4	V
Body Diode Reverse Recovery Time (Note 1)		t _{rr}	I _S =5.0A, V _{GS} =0V,		102		ns
Body Diode Reverse Recovery Charge		Q _{rr}	dl _F /dt=100A/µs		0.33		μC

2. Essentially independent of operating temperature. Notes: 1. Pulse Test: Pulse width ≤ 300µs, Duty cycle ≤ 2%

■ TEST CIRCUITS AND WAVEFORMS



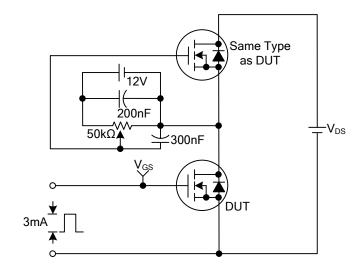
Peak Diode Recovery dv/dt Test Circuit

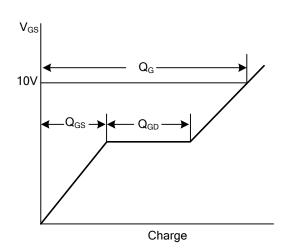


Peak Diode Recovery dwdt Waveforms

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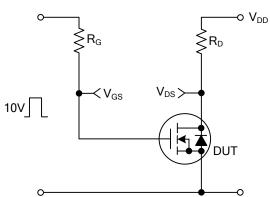
■ TEST CIRCUITS AND WAVEFORMS



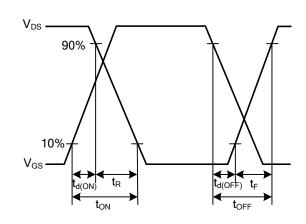


Gate Charge Test Circuit

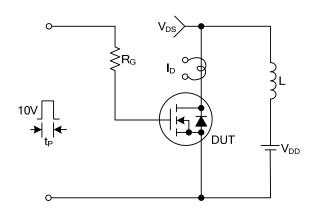
Gate Charge Waveforms



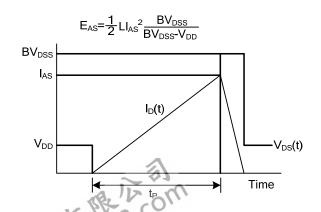




Resistive Switching Waveforms



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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