



L16B45B

Advance

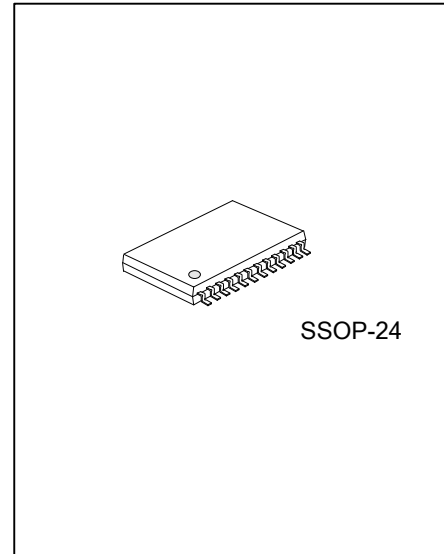
CMOS IC

16-BIT CONSTANT CURRENT LED SINK DRIVER

DESCRIPTION

The UTC **L16B45B** is designed for LED displays. UTC **L16B45B** contains a serial buffer and data latches which convert serial input data into parallel output format. at UTC **L16B45B** output stage, sixteen regulated current ports are designed to provide uniform and constant current sinks for driving LEDs within a large range of V_F variations.

UTC **L16B45B** provides users with great flexibility and device performance while using UTC **L16B45B** in their system design for LED display applications, e.g. LED panels. Users may adjust the output current from 0.6mA to 45mA through an external resistor, R-EXT, which gives users flexibility in controlling the light intensity of LEDs. UTC **L16B45B** guarantees to endure maximum 11V at the output port. The high clock frequency, 35MHz, also satisfies the system requirements of high volume data transmission.

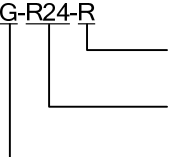


FEATURES

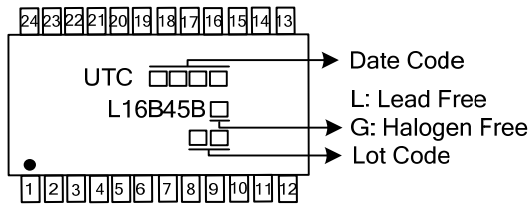
- * 16 constant-current output channels
- * Constant output current invariant to load voltage change:
 - Constant output current range:
 - 0.6~45mA @ $V_{DD}=5V$
 - 0.6~35mA @ $V_{DD}=3.3V$
- * Output current adjusted through an external resistor
- * Fast response of output current, \overline{OE} : 20ns @ $V_{DD}=3.3V$
- * Schmitt trigger input
- * 3.3V, 5V supply voltage

ORDERING INFORMATION

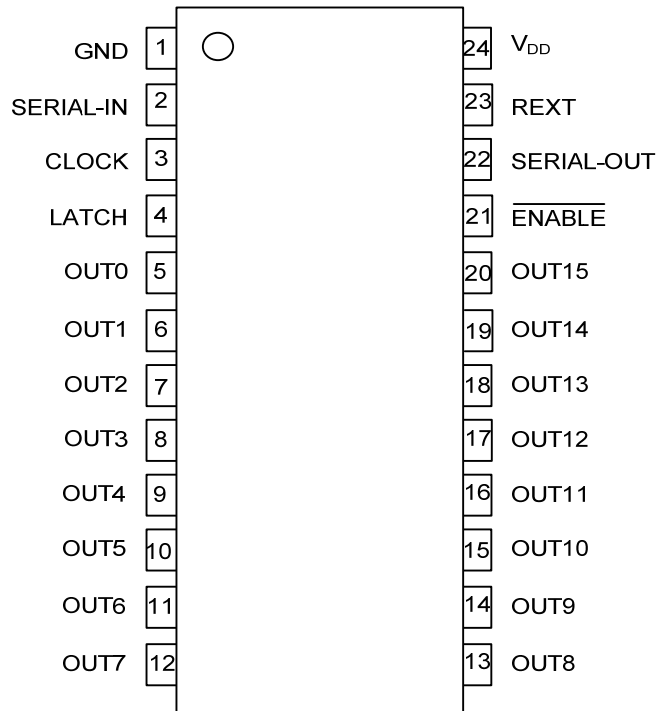
Ordering Number		Package	Packing
Lead Free	Halogen Free		
L16B45BL-R24-R	L16B45BG-R24-R	SSOP-24	Tape Reel

<p>L16B45BG-R24-R</p>  <ul style="list-style-type: none"> (1) Packing Type (2) Package Type (3) Green Package 	<ul style="list-style-type: none"> (1) R: Tape Reel (2) R24: SSOP-24 (3) G: Halogen Free and Lead Free, L: Lead Free
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MARKING



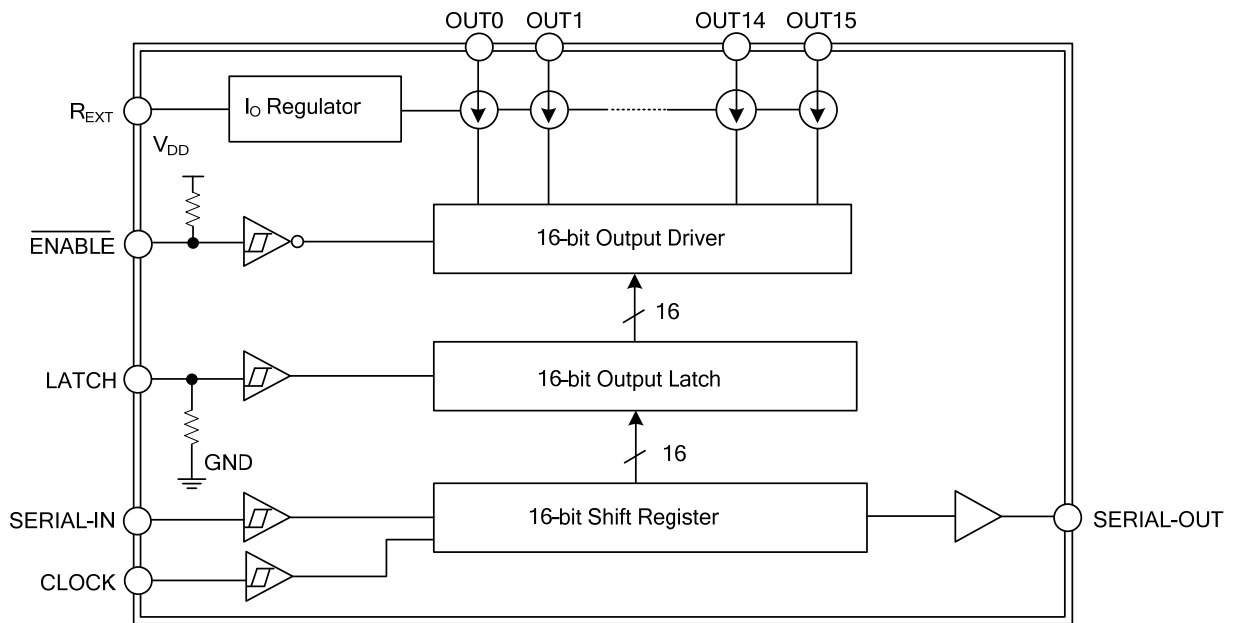
PIN CONFIGURATION



PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	GND	Ground terminal for control logic and current sink
2	SERIAL-IN	Serial-data input to the shift register
3	CLOCK	Clock input terminal for data shift on rising edge
4	LATCH	Data strobe input terminal Serial data is transferred to the output latch when LE is high. The data is latched when LE goes low.
5~20	OUT0~15	Constant current output terminals
21	$\overline{\text{ENABLE}}$	Output enable terminal When (active) low, the output drivers are enabled; when high, all output drivers are turned OFF (blanked).
22	SERIAL-OUT	Serial-data output to the following SDI of next driver IC
23	R _{EXT}	Input terminal used to connect an external resistor for setting up output current for all output channels
24	V _{DD}	3.5V/5V supply voltage terminal

■ BLOCK DIAGRAM



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■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}	0~7.0	V
Input Voltage	V_{IN}	-0.4 ~ $V_{DD}+0.4$	V
Output Current	I_{OUT}	45	mA
Output Voltage	V_{OUT}	-0.5 ~ +11	V
Clock Frequency	F_{CLK}	35	MHz
GND Terminal Current	I_{GND}	720	mA
Power Dissipation ($T_A=25^{\circ}C$)	P_D	0.9	W
Storage Temperature	T_{STG}	-55 ~ +150	$^{\circ}C$

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ DC ELECTRICAL CHARACTERISTICS ($V_{DD}=5.0V$, $T_A=25^{\circ}C$)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage	"H" Level	V_{IH}	$0.7 \times V_{DD}$		V_{DD}	V
	"L" Level	V_{IL}	GND		$0.3 \times V_{DD}$	
Output Leakage Current	I_{OH}	$V_{OH}=9V$			0.2	μA
Output Voltage (S-OUT)	V_{OL}	$I_{OL}=1.0mA$			0.4	V
	V_{OH}	$I_{OH}=-1.0mA$	4.6			
Output Current (Bit to Bit)	I_{OL1}	$V_{OUT}=1V$, $R_{EXT}=910\Omega$		± 2		%
	I_{OL2}	$V_{OUT}=1V$, $R_{EXT}=420\Omega$		± 2		
Output Current (chip to chip)	I_{OL3}	$V_{OUT}=1V$, $R_{EXT}=910\Omega$		± 4		%
	I_{OL4}	$V_{OUT}=1V$, $R_{EXT}=420\Omega$		± 4		
Output Current vs. Supply Voltage Regulation	$\%V_{DD}$	$R_{EXT}=420\Omega$, $T_A=-40\sim 85^{\circ}C$		± 1		$\%/V$
Output Current vs. Output Voltage Regulation	$\%V_{DS}$	$R_{EXT}=420\Omega$, $T_A=-40\sim 85^{\circ}C$		± 0.1		$\%/V$
Pull-Up Resistor	$R_{IN (up)}$			500		$K\Omega$
Pull-Down Resistor	$R_{IN (down)}$			500		$K\Omega$
Supply Current	"OFF"	$I_{DD (off) 1}$	$R_{EXT}=OPEN$, $OUT0\sim 15=off$	5	8	mA
		$I_{DD (off) 2}$	$R_{EXT}=420\Omega$, $OUT0\sim 15=off$	10	15	
	"ON"	$I_{DD (on) 1}$	$R_{EXT}=420\Omega$, $OUT0\sim 15=on$	10	15	

■ DC ELECTRICAL CHARACTERISTICS ($V_{DD}=3.3V$, $T_A=25^{\circ}C$)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage	"H" Level	V_{IH}		$0.7 \times V_{DD}$		V_{DD}	V
	"L" Level	V_{IL}		GND		$0.3 \times V_{DD}$	
Output Leakage Current		I_{OH}	$V_{OH}=9V$			0.2	μA
Output Voltage (S-OUT)		V_{OL}	$I_{OL}=1.0mA$			0.5	V
		V_{OH}	$I_{OH}=-1.0mA$	2.8			
Output Current (Bit to Bit)		I_{OL1}	$V_{OUT}=1V$, $R_{EXT}=2720\Omega$		± 2		%
		I_{OL2}	$V_{OUT}=1V$, $R_{EXT}=910\Omega$		± 2		
Output Current (chip to chip)		I_{OL3}	$V_{OUT}=1V$, $R_{EXT}=2720\Omega$		± 4		%
		I_{OL4}	$V_{OUT}=1V$, $R_{EXT}=910\Omega$		± 4		
Output Current vs. Supply Voltage Regulation		$\%V_{DD}$	$R_{EXT}=910\Omega$, $T_A=-40\sim 85^{\circ}C$		± 1		$\%/V$
Output Current vs. Output Voltage Regulation		$\%V_{DS}$	$R_{EXT}=910\Omega$, $T_A=-40\sim 85^{\circ}C$		± 0.1		$\%/V$
Pull-Up Resistor		$R_{IN (up)}$			500		K Ω
Pull-Down Resistor		$R_{IN (down)}$			500		K Ω
Supply Current	"OFF"	$I_{DD (off) 1}$	$R_{EXT}=OPEN$, $OUT0\sim 15=off$		4	6	mA
		$I_{DD (off) 2}$	$R_{EXT}=910\Omega$, $OUT0\sim 15=off$		6	10	
	"ON"	$I_{DD (on) 1}$	$R_{EXT}=910\Omega$, $OUT0\sim 15=on$		6	10	

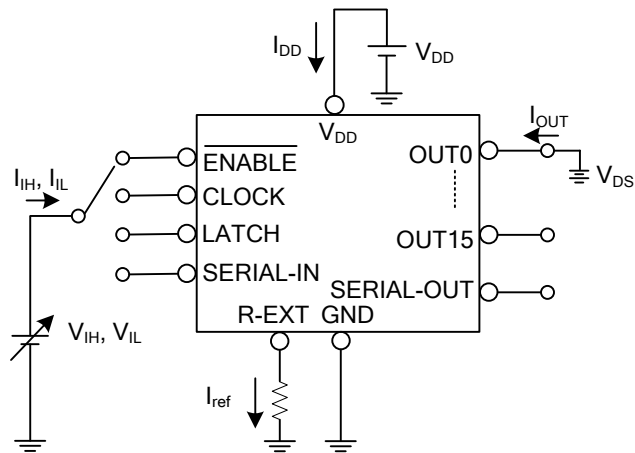
■ SWITCHING CHARACTERISTICS ($V_{DD}=5V$, $T_A=25^{\circ}C$)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
Propagation Delay Time ("L" to "H")	CLOCK-OUT0	t_{pLH}	$V_{DD}=5V$, $V_{IH}=V_{DD}$ $V_{IL}=GND$, $R_{EXT}=1K\Omega$ $V_L=4.5V$, $R_L=150\Omega$ $C_L=10pF$		20		ns	
	LATCH-OUT0				20			
	ENABLE-OUT0				20			
	CLOCK-SERIAL_OUT				10			
Propagation Delay Time ("H" to "L")	CLOCK-OUT0	t_{pHL}				30		ns
	LATCH-OUT0					30		
	ENABLE-OUT0					30		
	CLOCK-SERIAL_OUT					10		
Setup Time for SDI		t_{setup}				5		ns
Hold Time for SDI		t_{hold}				8		ns
Setup Time for LE		$t_{setup (L)}$				15		ns
Hold Time for LE		$t_{hold (L)}$				10		ns
Propagation Delay Time	Group1-Group2	t_{GD1}			2		ns	
	Group1-Group3	t_{GD2}			4		ns	
	Group1-Group4	t_{GD3}			6		ns	
Pulse Width	CLOCK	t_{wCLK}			15		ns	
	LATCH	t_{wLATCH}			15		ns	
	ENABLE	t_{wEN}			20		ns	
Output Rise Time of I_{OUT}		t_{or}			10		ns	
Output Fall Time of I_{OUT}		t_{of}			10		ns	

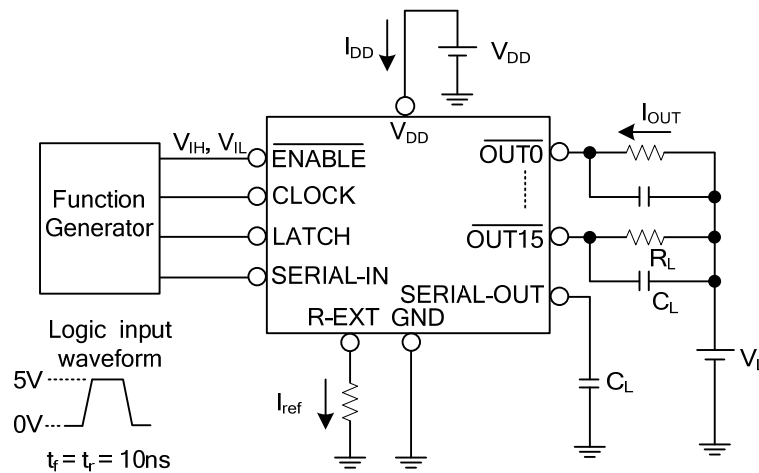
■ SWITCHING CHARACTERISTICS ($V_{DD}=3.3V$, $T_A=25^{\circ}C$)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation Delay Time ("L" to "H")	CLOCK-OUT0	t_{pLH}	$V_{DD}=3.3V$, $V_{IH}=V_{DD}$, $V_{IL}=GND$, $R_{EXT}=1K\Omega$, $V_L=3V$, $R_L=100\Omega$, $C_L=10pF$		20		ns
	LATCH-OUT0				20		
	ENABLE-OUT0				20		
	CLOCK-SERIAL_OUT				10		
Propagation Delay Time ("H" to "L")	CLOCK-OUT0	t_{pHL}			30		ns
	LATCH-OUT0				30		
	ENABLE-OUT0				30		
	CLOCK-SERIAL_OUT				10		
Setup Time for SDI		t_{setup}			5		ns
Hold Time for SDI		t_{hold}			8		ns
Setup Time for LE		$t_{setup(L)}$			15		ns
Hold Time for LE		$t_{hold(L)}$			15		ns
Propagation Delay Time	Group1-Group2	t_{GD1}			2		ns
	Group1-Group3	t_{GD2}			4		ns
	Group1-Group4	t_{GD3}			6		ns
Pulse Width	CLOCK	t_{WCLK}			20		ns
	LATCH	t_{WLATCH}		20		ns	
	ENABLE	t_{WEN}		40		ns	
Output Rise Time of I_{OUT}		t_{or}		20		ns	
Output Fall Time of I_{OUT}		t_{of}		20		ns	

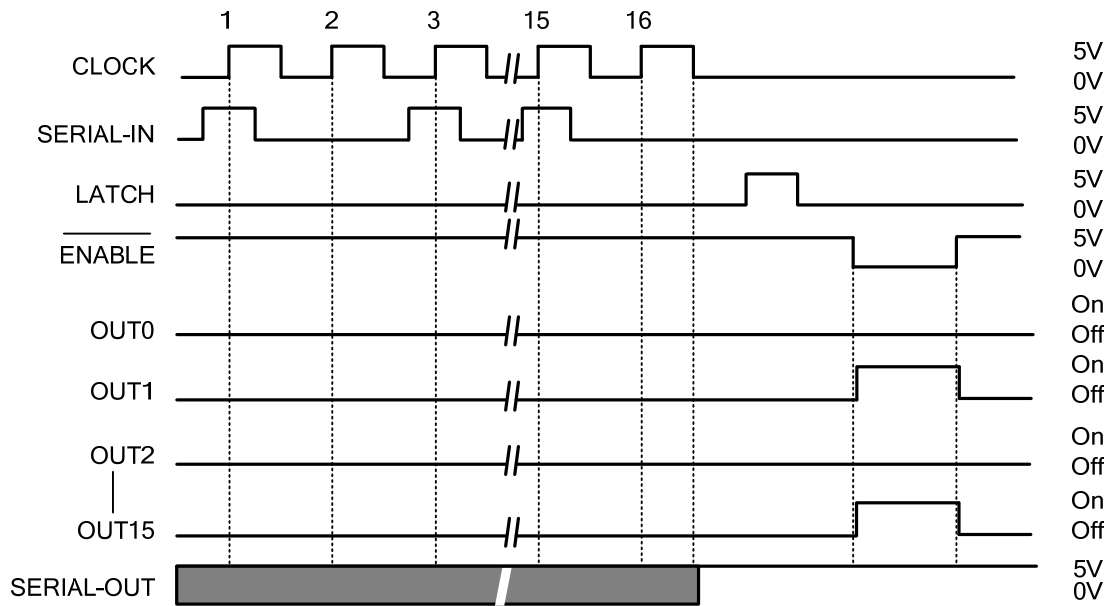
■ TEST CIRCUIT FOR DC ELECTRICAL CHARACTERISTICS



■ TEST CIRCUIT FOR SWITCHING ELECTRICAL CHARACTERISTICS

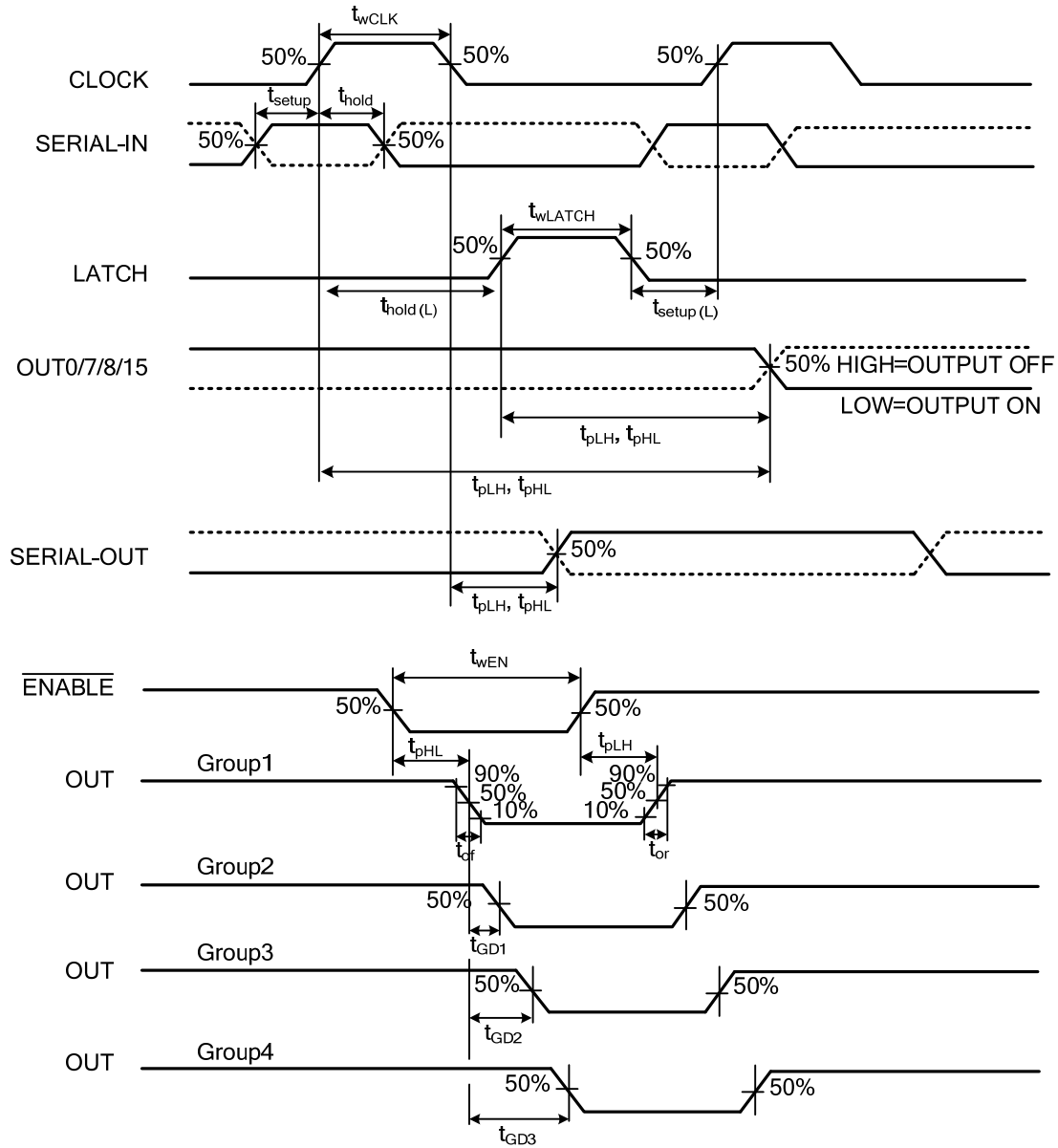


■ TIMING DIAGRAM

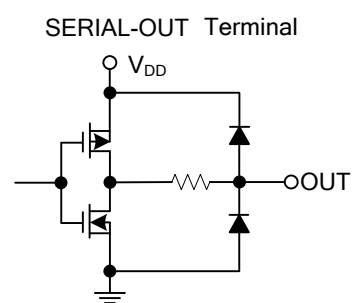
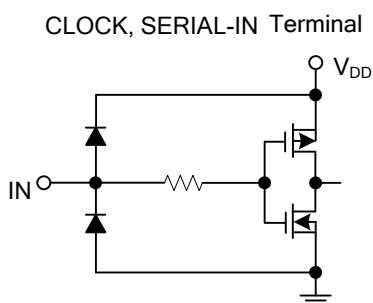
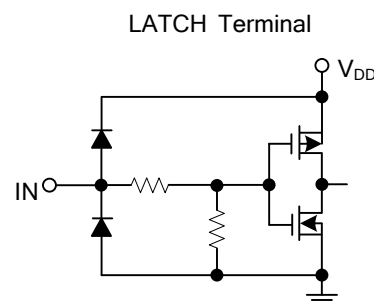
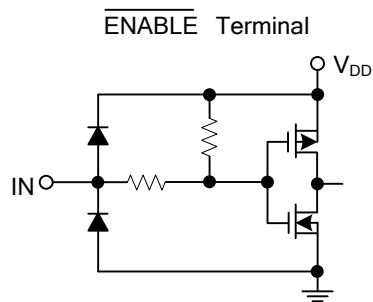


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■ TIMING WAVEFORM



■ EQUIVALENT CIRCUITS OF INPUTS AND OUTPUTS



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