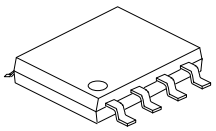
HIGH PERFORMANCE POWER FACTOR CORRECTION CONTROLLER IN CONTINUOUS CONDUCTION MODE



SOP-8

■ DESCRIPTION

The UTC **L8565** is a wide input range controller integrated circuit for active power factor correction. The circuit is designed for boost PFC application, and requires reduced external component count. Its power supply is recommended to be provided by an external auxiliary supply which will switch on and off the IC.

The circuit operates in the continuous conduction mode under average current, and in discontinuous conduction mode only in light load condition. The switching frequency can be set with the external resistor at pin 4. Both current and voltage loop compensations are done externally to allow full user control.

There are many kinds of protection features incorporated to make sure of safe system operation conditions, such as brown-out protection, output under voltage detection and peak current limitation. The inside reference is adjusted (5V±2%) to make sure control level and precise protection. There is a particular soft-start function to limit the start up current and thus reduces the stress on the boost diode.

■ FEATURES

* Supports wide input range
* Average current control
* Ease of use with few external components
* External current and voltage loop compensation
* Trimmed internal reference voltage (5V±2%)
* Programmable operating/switching frequency (50kHz ~ 250kHz)
* Max duty cycle of 95% (typ) at 125kHz
* Under voltage lockout
* Cycle by cycle peak current limiting
* Over-voltage protection
* Open loop detection
* Output under-voltage detection
* Brown-out protection
* Soft Over current Protection
* Enhanced dynamic response

■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
L8565L-S08-R	L8565G-S08-R	SOP-8	Tape Reel
L8565L-S08-T	L8565G-S08-T	SOP-8	Tube

L8565L-S08-T (1)Packing Type (2)Package Type (3)Lead Free	(1) T: Tube, R: Tape Reel (2) S08: SOP-8 (3) L: Lead Free, G: Halogen Free

■ PIN CONFIGURATION

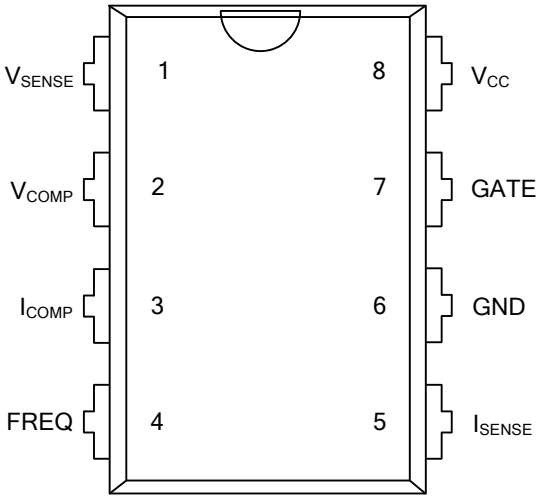
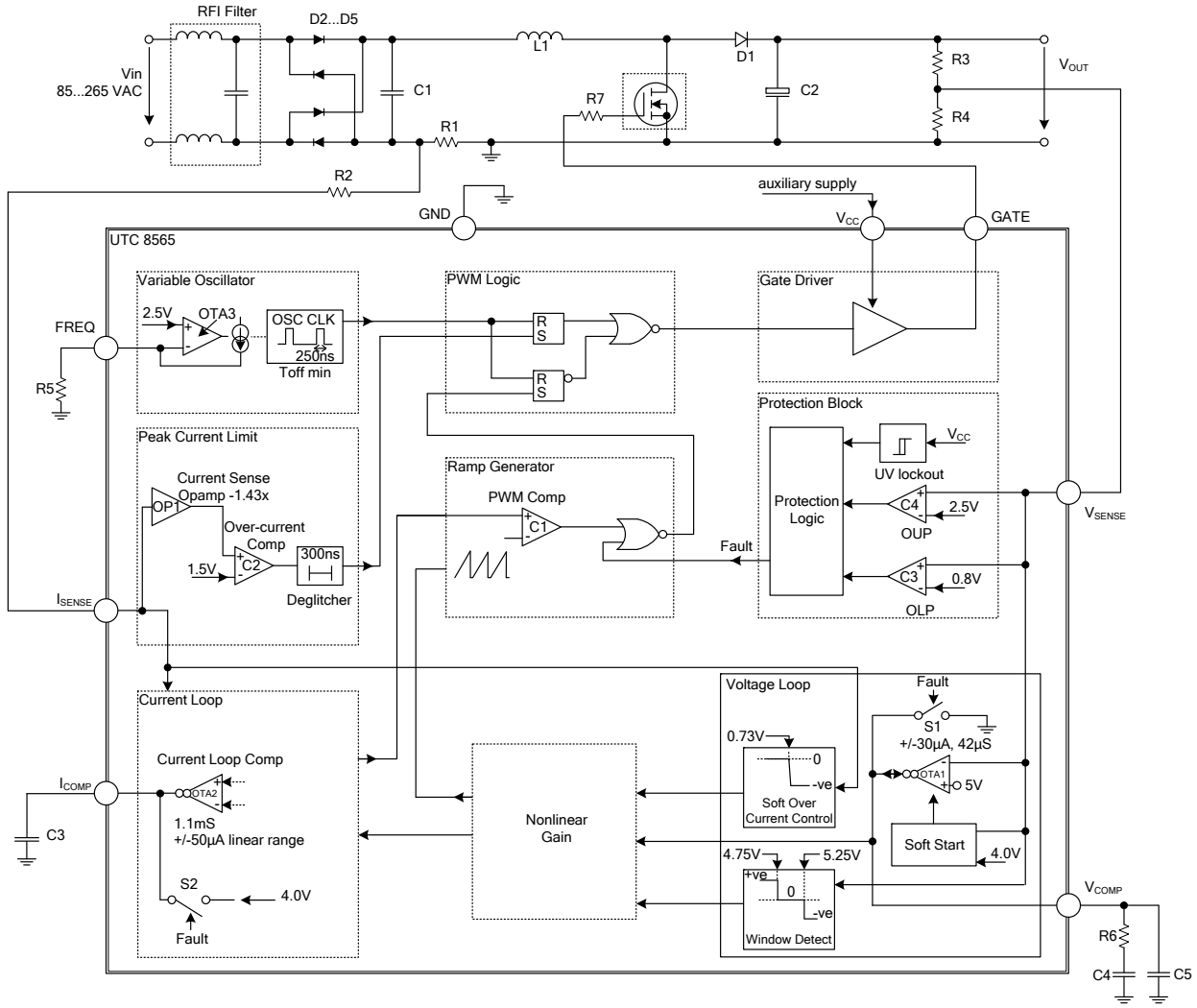


Figure 1. Pin Configuration (top view)

■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	V_{SENSE}	The output bus voltage of the boost converter is sensed at this pin via a resistive divider. The reference voltage for this pin is 5V.
2	V_{COMP}	This V_{COMP} Pin provides the compensation of the output voltage loop with a compensation network to ground (see Figure 2). This also gives the soft start function which controls an increasing AC input current during start-up.
3	I_{COMP}	At this pin the compensation components of the current loop are connected. The capacitor which is connected at this pin integrates the output current of OTA2 and averages the current sense signal.
4	FREQ	A resistor connected to this pin sets the fixed switching frequency. The frequency range is from 50kHz to 250kHz.
5	I_{SENSE}	The pin senses the negative voltage drop at the external sense resistor (R1). This is the input signal for the average current regulation in the current loop. It is also fed to the peak current limitation block. During power up time, high inrush currents cause high voltage drop at R1, driving currents into pin 5 which could be beyond the absolute maximum ratings. Therefore a series resistor (R2) of around 220Ω is recommended in order to limit this current into the IC.
6	GND	This is the Ground pin.
7	GATE	The GATE pin is the output of the internal driver stage, which has a capability of 1.5A source and sink current. Its gate drive voltage is clamped at 11.5V (typically).
8	V_{CC}	The V_{CC} pin is the positive supply of the IC and should be connected to an external auxiliary supply. The operating range is between 10V and 21V. The turn-on threshold is at 11.2V and under voltage occurs at 10.2V.

■ BLOCK DIAGRAM



Representative Block diagram

■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNIT
V_{CC} Supply Voltage	V_{CC}	-0.3 ~ 22	V
FREQ Voltage	V_{FREQ}	-0.3 ~ 7	V
I_{COMP} Voltage	V_{ICOMP}	-0.3 ~ 7	V
I_{SENSE} Voltage	V_{ISENSE}	-24 ~ 7	V
I_{SENSE} Current	I_{ISENSE}	±1	mA
V_{SENSE} Voltage	V_{VSENSE}	-0.3 ~ 7	V
V_{SENSE} Current	I_{VSENSE}	±1	mA
V_{COMP} Voltage	V_{VCOMP}	-0.3 ~ 7	V
GATE Voltage	V_{GATE}	-0.3 ~ 22	V
Junction Temperature	T_J	-40 ~ 150	°C
Storage Temperature	T_{STG}	-55 ~ 150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	90	K/W

■ ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPERATING RANGE (Note 1)						
V_{CC} Supply Voltage	V_{CC}		V_{CCUVLO}		21	V
Junction Temperature	$T_{J(CON)}$		-40		125	°C
SUPPLY SECTION (Note 2)						
V_{CC} Turn-On Threshold	V_{CCON}		10.5	11.2	11.9	V
V_{CC} Turn-Off Threshold/ Under Voltage Lock Out	V_{CCUVLO}		9.4	10.2	10.8	V
V_{CC} Turn-On/Off Hysteresis	V_{CCHY}		0.8	1	1.3	V
Start Up Current Before V_{CCON}	$I_{CCSTART}$	$V_{VCC}=V_{VCC(ON)}$-0.1V	50	100	200	μA
Operating Current With Active GATE	I_{CCHG}	R5=33kΩ, C_L=4.7nF	13.5	18	22.5	mA
Operating Current During Standby	$I_{CCSTDBY}$	R5 = 33kΩ, V_{VSENSE}=0.5V	2.0	2.6	3.2	mA
VARIABLE FREQUENCY SECTION						
Switching Frequency (Typical)	F_{SWNOM}	R5=33kΩ	106	133	161	kHz
Switching Frequency (Min.)	$F_{SW(MIN)}$	R5=82kΩ	40	56	70	kHz
Switching Frequency (Max.)	$F_{SW(MAX)}$	R5=15kΩ	200	250	320	kHz
Voltage At FREQ Pin	V_{FREQ}		2.40	2.50	2.60	V
PWM SECTION						
Max. Duty Cycle	D_{MAX}	$F_{SW}=F_{SWNOM}$ (R5=33kΩ)	92	95	98	%
Min. Duty Cycle	D_{MIN}	V_{VCOMP}=0V, V_{VSENSE}=5V, V_{ICOMP}=6.4V			0	%
Min. Off Time	$T_{OFF(MIN)}$	V_{VCOMP}=5V, V_{VSENSE}=5V, V_{ISENSE}=0.1V	150	250	350	ns

■ ELECTRICAL CHARACTERISTICS(Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYSTEM PROTECTION SECTION						
Open Loop Protection (OLP) V_{SENSE} Threshold	V_{OLP}		0.77	0.81	0.86	V
Peak Current Limitation (PCL) I_{SENSE} Threshold	V_{PCL}		-1.15	-1.08	-1.00	V
Soft Over Current Control (SOC) I_{SENSE} Threshold	V_{SOC}		-0.79	-0.73	-0.66	V
Output Under Voltage Detection (OUV) V_{SENSE} Threshold	V_{OUV}		2.45	2.55	2.65	V
Output Over-Voltage Protection (OVP)	V_{OVP}		5.12	5.25	5.38	V
CURRENT LOOP SECTION						
OTA2 Transconductance Gain	Gm_{OTA2}	At Temp=25°C	0.9	1.1	1.3	mS
OTA2 Output Linear Range	I_{OTA2}	Guaranteed by design		±50		μA
I_{COMP} Voltage during OLP	V_{ICOMPF}	V_{VSENSE}=0.5V	3.6	4.0		V
VOLTAGE LOOP SECTION						
OTA1 Reference Voltage	V_{OTA1}		4.90	5.00	5.10	V
OTA1 Transconductance Gain	Gm_{OTA1}		31.5	42	52.5	μS
OTA1 Max. Source Current Under Normal Operation	I_{OTA1SO}	V_{VSENSE}=4.25V, V_{VCOMP}=4V	21	30	38	μA
OTA1 Max. Sink Current Under Normal Operation	I_{OTA1SK}	V_{VSENSE}=6V, V_{VCOMP}=4V	21	30	38	μA
Soft Start End	V_{SOFT}		3.80	4.00	4.20	V
OTA1 Source Current Under Soft Start	I_{OTA1SS}	V_{VSENSE}=2V, V_{VCOMP}=0V	8.0	10.8	13.4	μA
Enhanced Dynamic Response — V_{SENSE} High	V_{Hi}		5.12	5.25	5.38	V
Enhanced Dynamic Response — V_{SENSE} Low	V_{Lo}		4.63	4.75	4.87	V
V_{SENSE} Input Bias Current At 5V	I_{VSEN5V}	V_{VSENSE}=5V	0		1.5	μA
V_{SENSE} Input Bias Current at 1V	I_{VSEN1V}	V_{VSENSE}=1V	0		1	μA
V_{COMP} Voltage during OLP	V_{VCOMPF}	V_{VSENSE}= 0.5V, I_{VCOMP}=0.5mA	0	0.2	0.4	V
DRIVER SECTION						
GATE Low Voltage	V_{GATEL}	V_{CC}=5V, I_{GATE}=5mA			1.2	V
		V_{CC}=5V, I_{GATE}=20mA			1.5	V
		I_{GATE}=0A		0.8		V
		I_{GATE}=20mA		1.6	2.0	V
		I_{GATE}=-20mA	-0.2	0.2		V
GATE High Voltage	V_{GATEH}	V_{CC}=20V, C_L=4.7nF		11.5		V
		V_{CC}=11V, C_L =4.7nF		10.5		V
		V_{CC}=$V_{VCC(OFF)}$+0.2V, C_L=4.7nF		7.5		V
GATE Rise Time	t_R	V_{GATE}=2V...9V, C_L=4.7nF		20		ns
GATE Fall Time	t_F	V_{GATE}=9V...2V, C_L=4.7nF		20		ns
GATE Current, Peak, Rising Edge	I_{GATE}	C_L=4.7nF (Note 3)	-1.5			A
GATE Current, Peak, Falling Edge	I_{GATE}	C_L=4.7nF (Note 3)			1.5	A

Notes: 1. Within the operating range the IC operates as described in the functional description.
2. The electrical characteristics involve the spread of values within the specified supply voltage and junction temperature range T_J from -40°C to 125°C. Typical values represent the median values, which are related to 25°C. If not otherwise stated, a supply voltage of V_{CC}=15V is assumed for test condition.
3. Design characteristics (not meant for production testing).

■ FUNCTIONAL DESCRIPTION

1. General

The UTC **L8565** is an active power factor correction controller for boost PFC application. The IC comes in DIP package and is suitable for wide input range applications from 85 to 265 V_{AC}. The IC is usually realized with boost converters and it operates in continuous conduction mode with average current control.

The UTC **L8565** operates with a cascaded control; the inner current loop and the outer voltage loop. The inner current loop of the IC controls the sinusoidal profile for the average input current. It uses the dependency of the PWM duty cycle on the line input voltage to determine the corresponding input current. This means the average input current follows the input voltage as long as the device operates in CCM. Under light load condition, depending on the choke inductance, the system may enter into discontinuous conduction mode (DCM). In DCM, the average current waveform will be distorted but the resultant harmonics are still low enough to meet the Class D requirement of IEC 1000-3-2. The outer loop controls the output voltage. Depending on the load condition, OTA1 establishes an appropriate voltage at V_{COMP} pin which controls the amplitude of the average input current.

The UTC **L8565** provides several protection features to ensure safe operating condition for both the system and device. Important protection features are namely Brown-out protection, Current Limitation and Output Under-voltage Protection.

2. Power Supply

The operating voltage range of the V_{CC} is from 10V to 21V. An internal under voltage lockout (UVLO) block monitors the V_{CC} power supply. As soon as it exceeds 11.2V and the voltage at pin 1 (V_{SENSE}) is >0.8V, the IC begins operating its gate drive and performs its Soft-Start as shown in Fig. 3.

If V_{CC} drops below 10.2V, the IC is off. The IC will then be consuming typically 200μA, whereas consuming 18mA during normal operation.

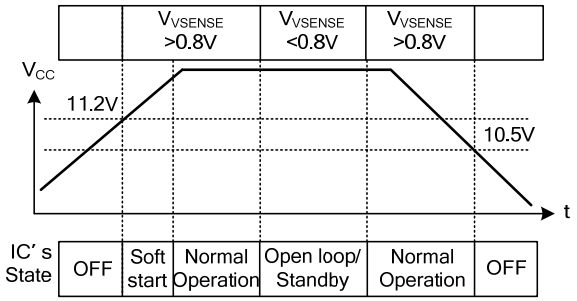


Fig. 3. State of Operation Respect to V_{CC}

The IC can be turned off and forced into standby mode by pulling down the voltage at pin 1 (V_{SENSE}) to lower than 0.8V. The current consumption is reduced to 3mA in this mode.

■ FUNCTIONAL DESCRIPTION(Cont.)

3. Start-up (Soft-Start)

The operation of OTA1 during startup is shown in Fig. 4 and 5.

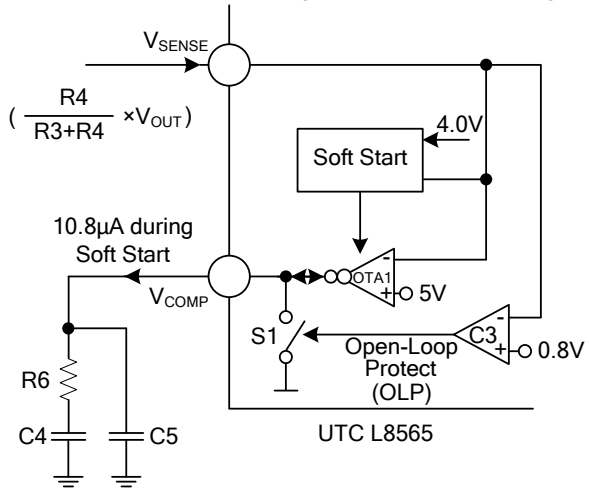


Fig. 4 Soft Start Circuit

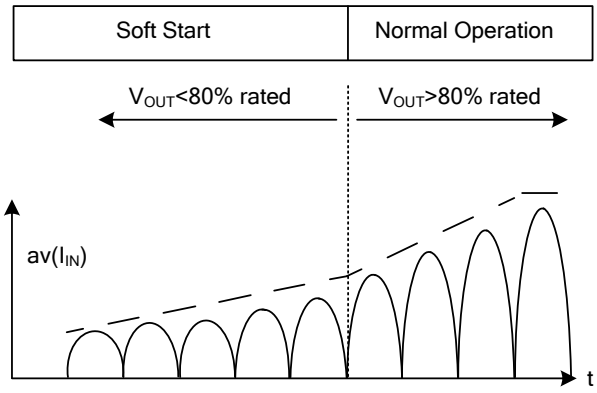


Fig. 5 Soft Start With Controlled Current

It sources a constant 10.8μA into the compensation network at pin 2 (V_{COMP}). The voltage at this pin rises linearly and so does the amplitude of the input current. As soon as the output voltage V_{OUT} reaches 80% of its rated level, the startup procedure is finished and the normal voltage control takes over. In normal operation, the IC operates with a higher maximum current at OTA1 and therefore with a higher voltage loop gain in order to improve the dynamic behavior of the device.

The advantage of this technique is a soft-start function with lower stress for the boost diode but without the risk of audible noise.

4. System Protection

The IC is equipped with various protection features to ensure the PFC system in safe operating range. Depending on the input line voltage (V_{IN}) and output bus voltage (V_{OUT}), When these protections are active the conditions are shown in Fig. 6 and 7.

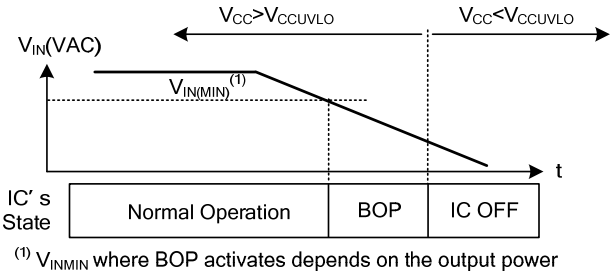


Fig. 6 V_{IN} Related Protection Features

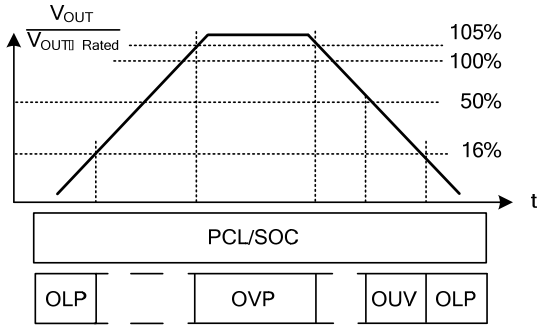


Fig. 7 V_{OUT} Related Protection Features

The following sections describe the functionality of these protection features.

■ FUNCTIONAL DESCRIPTION(Cont.)

4.1 Brown-Out Protection (BOP)

Input Brown-out occurs if the input voltage V_{IN} falls below the minimum input voltage of the design (i.e. 85V for universal input voltage range) and the V_{CC} has not entered into the V_{CC} under voltage lockout level yet. For a system without BOP, the boost converter will increasingly draw a higher current from the mains at a given output power which may exceed the maximum design values of the input current. The UTC **L8565** limits internally the current drawn from the mains and therefore also limits the input power. The difference of input and output power will result in decreasing output voltage. If the condition prolongs, the decreasing V_{OUT} will terminate in output under voltage condition (OUV, 50% of rated), and the IC will be shut down (See section 4.5).

Fig. 8 shows the occurrence of BOP in respect to the I_{SENSE} voltage.

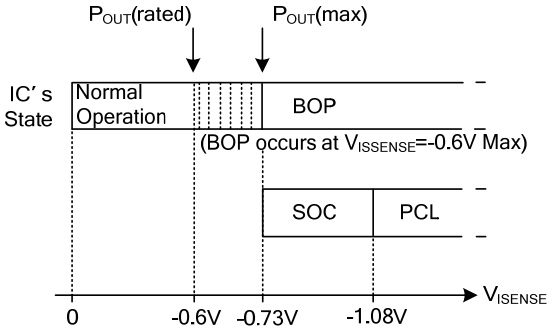


Fig. 8 BOP, SOC and PCL Protection as Function of V_{ISENSE}

The V_{IN} threshold for BOP to occur is dependent on the voltage at I_{SENSE} and thus the output power. The rated output power with a minimum V_{IN} ($V_{IN(MIN)}$) is

$$P_{OUT}(rated) = V_{INMIN} \times \frac{0.6}{R1\times\sqrt{2}}$$

Due to the internal parameter tolerance, the maximum power with $V_{IN(MIN)}$ before BOP occurs is

$$P_{OUT}(max) = V_{INMIN} \times \frac{0.73}{R1\times\sqrt{2}}$$

And the BOP takes over the normal operation under rated output power latest at an input voltage of

$$V_{BOPMAX} = P_{OUT}(rated) \times \frac{R1\times\sqrt{2}}{0.73}$$

4.2 Soft Over Current Control (SOC)

The UTC **L8565** is designed not to support any output power that corresponds to a voltage lower than -0.73V at the I_{SENSE} pin. A further increase in the inductor current, which results in a lower I_{SENSE} voltage, will activate the Soft Over Current Control (SOC). This is a soft control as it does not directly switch off the gate drive like the PCL. It acts on the nonlinear gain block to result in a reduced PWM duty cycle.

4.3 Peak Current Limit (PCL)

The UTC **L8565** is equipped with a cycle by cycle peak current protection feature. It is active when the voltage at pin 5 (I_{SENSE}) reaches -1.08V. This voltage is amplified by OP1 with a factor of -1.43 and connected to comparator C2 with a reference voltage of 1.5V as shown in Fig. 9. A deglitcher with 300ns after the comparator improves noise immunity to the activation of this protection.

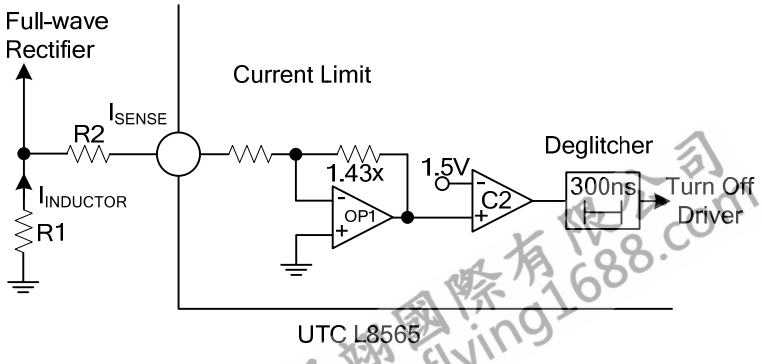


Fig. 9 Peak Current Limit (PCL)

■ FUNCTIONAL DESCRIPTION(Cont.)

4.4 Open Loop Protection / Input Under Voltage Protect (OLP)

Whenever V_{SENSE} voltage falls below 0.8V, or equivalently V_{OUT} falls below 16% of its rated value, it indicates an open loop condition (i.e. V_{SENSE} pin not connected) or an insufficient input voltage V_{IN} for normal operation. In this case, most of the blocks within the IC will be shutdown. The function is implemented using comparator C3 with a threshold of 0.8V as shown in the IC block diagram in Fig. 2.

4.5 Output Under Voltage Detection (OUV)

In the event of main interrupt or brown-out condition, the PFC system is not able to deliver the rated output power. This will cause the output voltage V_{OUT} to drop below its rated value. The IC provides an output under voltage detection that checks if V_{OUT} is falling below 50% of its rated value. Comparator C4 as shown in the device block diagram (Fig. 2) senses the voltage at pin 1 (V_{SENSE}) with a reference of 2.5V. If comparator C4 trips, the IC will be shut down as in OLP. The IC will be ready to restart if there is sufficient V_{IN} to pull V_{OUT} out of OLP.

4.6 Over-Voltage Protection (OVP)

Whenever V_{OUT} exceeds the rated value by 5%, the over-voltage protection OVP is active as shown in Fig. 7. This is implemented by sensing the voltage at pin V_{SENSE} with respect to a reference voltage of 5.25V. A V_{SENSE} voltage higher than 5.25V will immediately reduce the output duty cycle, bypassing the normal voltage loop control. This results in a lower input power to reduce the output voltage V_{OUT}.

5. Frequency Setting

The switching frequency of the PFC controller is fixed and can be set by an external resistor R5 at FREQ pin. The pin voltage V_{FREQ} is typically 2.5V. The corresponding capacitor for the oscillator is integrated in the device and the R5/frequency relationship is given at the “Electrical Characteristic” section. The recommended operating frequency range is from 50kHz to 250kHz. As an example, a R5 of 33kΩ at pin FREQ will set a switching frequency F_{SW} of 133kHz typically.

6. Average Current Control

6.1 Complete Current Loop

Fig. 10 show the complete system current loop. It consists of the current loop block which averages the voltage at pin I_{SENSE}, resulted from the inductor current flowing across R1. The averaged waveform is compared with an internal ramp in the ramp generator and PWM block. Once the ramp crosses the average waveform, the comparator C1 turns on the driver stage through the PWM logic block. The Nonlinear Gain block defines the amplitude of the inductor current. The following sections describe the functionality of each individual blocks.

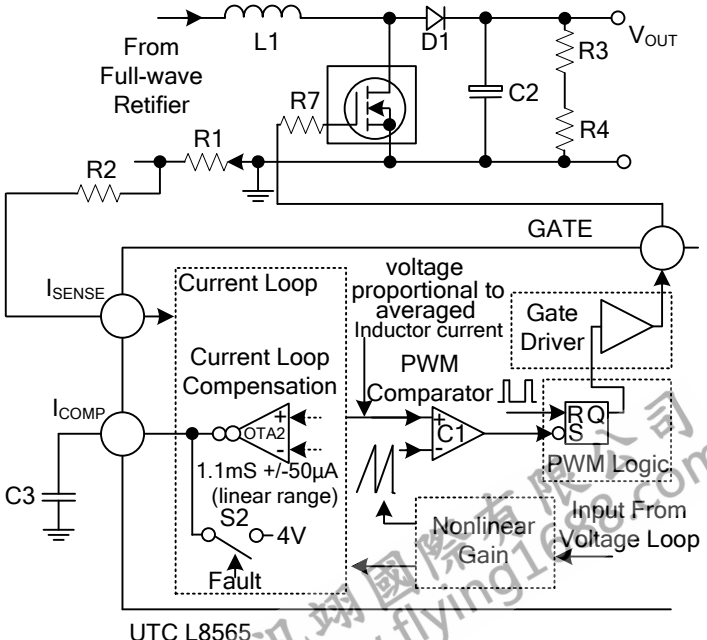


Fig. 10 Complete System Current Loop

■ FUNCTIONAL DESCRIPTION(Cont.)

6.2 Current Loop Compensation

The compensation of the current loop is done at the ICOMP pin. This is the OTA2 output and a capacitor C3 has to be installed at this node to ground (see Fig. 10). Under normal mode of operation, this pin gives a voltage which is proportional to the averaged inductor current. This pin is internally shorted to 5V in the event of IC shuts down when OLP and UVLO occur.

6.3 Pulse Width Modulation (PWM)

The IC employs an average current control scheme in continuous conduction mode (CCM) to achieve the power factor correction.

Assuming the voltage loop is working and output voltage is kept constant, the off duty cycle D_{OFF} for a CCM PFC system is given as

$$D_{OFF} = \frac{V_{IN}}{V_{OUT}}$$

From the above equation, D_{OFF} is proportional to V_{IN}. The objective of the current loop is to regulate the average inductor current such that it is proportional to the off duty cycle D_{OFF}, and thus to the input voltage V_{IN}. Fig. 11 shows the scheme to achieve the objective.

The PWM is performed by the intersection of a ramp signal with the averaged inductor current at pin 3 (I_{COMP}). The PWM cycle starts with the Gate turn off for a duration of $T_{OFF(MIN)}$ (250ns typ.) and the ramp is kept discharged. The ramp is then allowed to rise after $T_{OFF(MIN)}$ expires. The off time of the boost transistor ends at the intersection of the ramp signal and the averaged current waveform. This results in the proportional relationship between the average current and the off duty cycle D_{OFF}.

Fig. 12 shows the timing diagrams of $T_{OFF(MIN)}$ and the PWM waveforms.

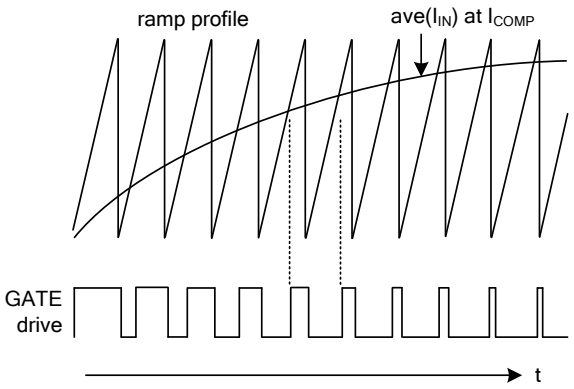


Fig. 11 Average Current Control in CCM

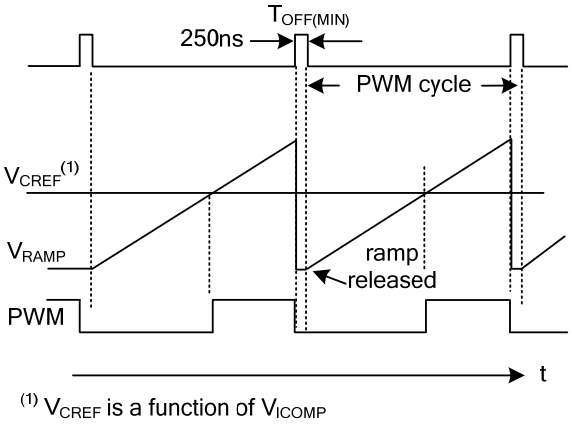


Fig. 12 Ramp and PWM Waveforms

6.4 Nonlinear Gain Block

The nonlinear gain block controls the amplitude of the regulated inductor current. The input of this block is the voltage at pin V_{COMP}. This block has been designed to support the wide input voltage range (85-265V_{AC}).

■ FUNCTIONAL DESCRIPTION(Cont.)

7. PWM Logic

The PWM logic block prioritizes the control input signals and generates the final logic signal to turn on the driver stage. The speed of the logic gates in this block, together with the width of the reset pulse $T_{OFF(MIN)}$, are designed to meet a maximum duty cycle D_{MAX} of 95% at the GATE output under 133kHz of operation.

In case of high input currents which result in Peak Current Limitation, the GATE will be turned off immediately and maintained in off state for the current PWM cycle. The signal T_{OFFMIN} resets (highest priority, overriding other input signals) both the current limit latch and the PWM on latch as illustrated in Fig. 13.

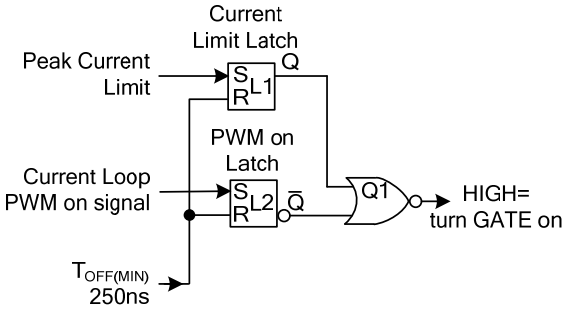


Fig. 13 PWM Logic

8. Voltage Loop

The voltage loop is the outer loop of the cascaded control scheme which controls the PFC output bus voltage V_{OUT}. This loop is closed by the feedback sensing voltage at V_{SENSE} which is a resistive divider tapping from V_{OUT}. The pin V_{SENSE} is the input of OTA1 which has an internal reference of 5V. Fig. 14 shows the important blocks of this voltage loop.

8.1 Voltage Loop Compensation

The compensation of the voltage loop is installed at the V_{COMP} pin (see Fig. 14). This is the output of OTA1 and the compensation must be connected at this pin to ground. The compensation is also responsible for the soft start function which controls an increasing AC input current during start-up.

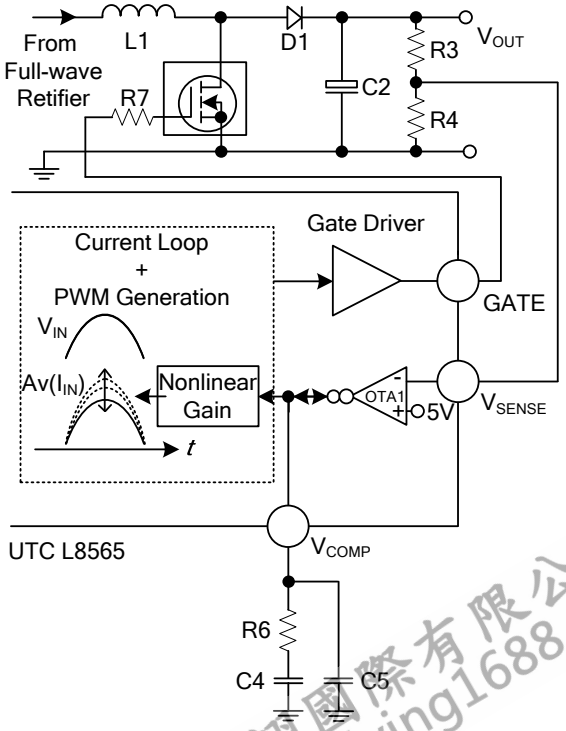


Fig. 14 Voltage Loop

■ FUNCTIONAL DESCRIPTION(Cont.)

8.2 Enhanced Dynamic Response

Due to the low frequency bandwidth of the voltage loop, the dynamic response is slow and in the range of about several 10ms. This may cause additional stress to the bus capacitor and the switching transistor of the PFC in the event of heavy load changes.

The IC provides therefore a “window detector” for the feedback voltage V_{VSENSE} at pin 1 (V_{SENSE}). Whenever V_{VSENSE} exceeds the reference value (5V) by ±5%, it will act on the nonlinear gain block which in turn affect the gate drive duty cycle directly. This change in duty cycle is bypassing the slow changing V_{COMP} voltage, thus results in a fast dynamic response of V_{OUT}.

9. Output Gate Driver

The output gate driver is a fast totem pole gate drive. It has an in-built cross conduction currents protection and a Zener diode Z1 (see Fig. 15) to protect the external transistor switch against undesirable over voltages. The maximum voltage at pin 7 (GATE) is typically clamped at 11.5V.

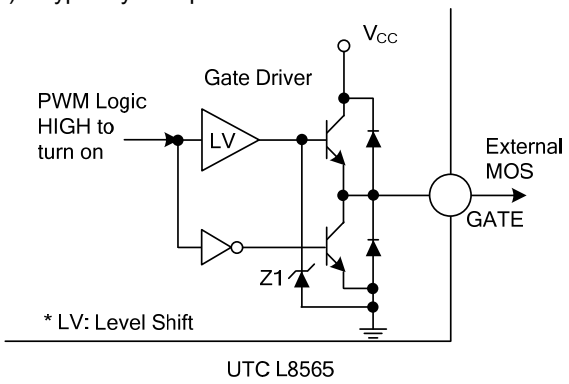


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Fig. 15 Gate Driver

The output is active HIGH and at V_{CC} voltages below the under voltage lockout threshold V_{CCUVLO}, the gate drive is internally pull low to maintain the off state.

■ TYPICAL APPLICATION CIRCUIT