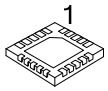
LOW POWER 6 STAGE FET LNA AND MIXER BIAS CONTROLLER



QFN-20(4×4)

■ DESCRIPTION

The UTC **L8602** is a programmable low power depletion mode FET bias and mixer controller intended primarily for satellite Low Noise Blocks (LNBs).

Designed to provide system flexibility the UTC **L8602** can be programmed to bias six low noise amplifier (LNA) stages or four LNA and two active mixer stages, allowing the UTC **L8602** to be used in several system designs.

Combining an advanced IC process and packaging techniques, the UTC **L8602** helps minimize power consumption, component cost and PCB area whilst enhancing overall reliability.

■ FEATURES

* Low quiescent supply current, 1.6mA typical
* Six stage FET bias controller, two configurable as mixer stages
* Operating range of 3.0V to 8.0V
* Amplifier FET drain voltages set at 2.0V, mixer drain voltage set at 0.25V
* Amplifier FET drain current selectable from 0 to 15mA, mixer current from 0 to 7.5mA
* Switchable FET's for power management
* FET drain voltages and currents held stable over temperature and V_{CC} variations
* FETs protected against overstress during power-up and power-down.
* Internal negative supply generator allowing single supply operation (available for external use)
* Low external component count

■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
L8602G-Q20-4040-R	L8602G-Q20-4040-R	QFN-20(4×4)	Tape Reel

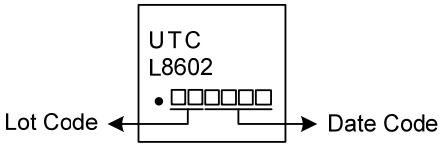
L8602G-Q20-4040-R

(1)Packing Type — (1) R: Tape Reel

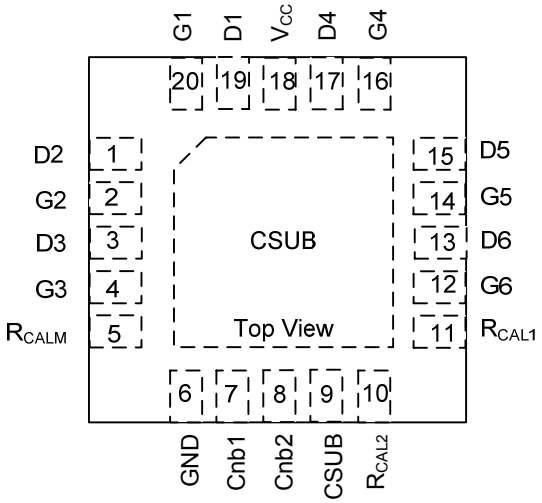
(2)Package Type — (2) Q20-4040: QFN-20(4×4)

(3)Green Package — (3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



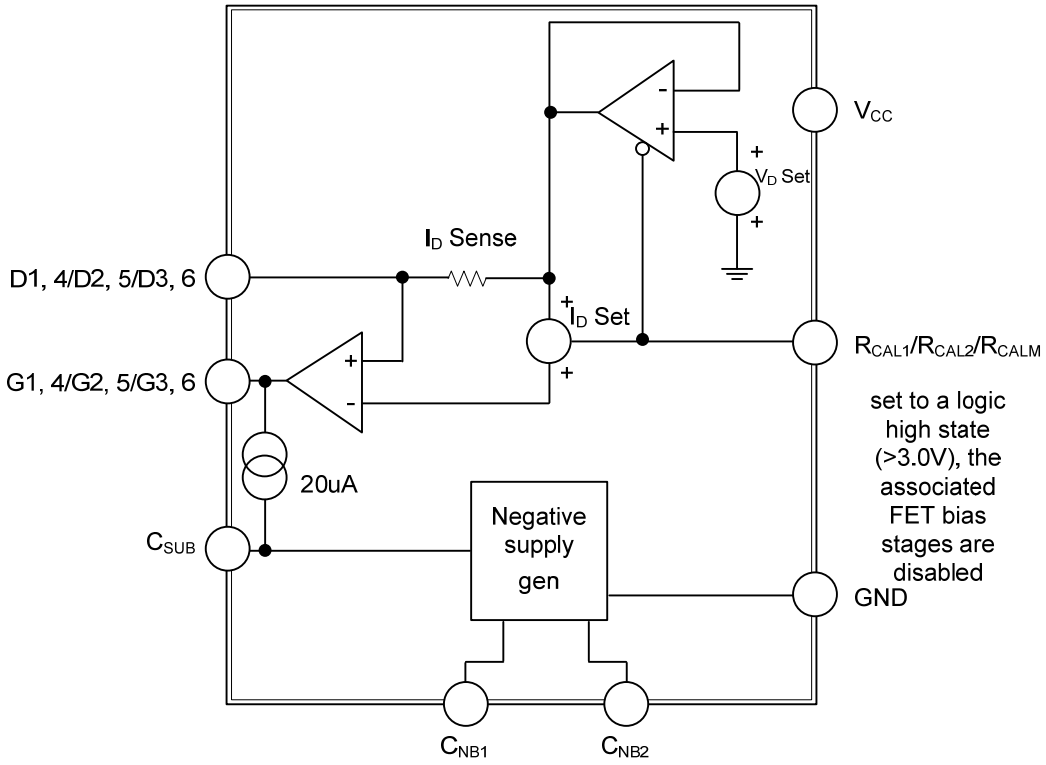
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	D2	To D of fet 2
2	G2	To G of fet 2
3	D3	To D of fet 3
4	G3	To G of fet 3
5	R_{CALM}	Connect 68kohm to set Id3/6 to 5mA
6	GND	Ground
7	Cnb1	connect an external cap to cnb2
8	Cnb2	connect an external cap to cnb1
9	CSUB	connect an external cap to produce -2.5V
10	R_{CAL2}	Connect 36kohm to set Id2/5 to 10mA
11	R_{CAL1}	Connect 36kohm to set Id1/4 to 10mA
12	G6	To G of fet 6
13	D6	To D of fet 6
14	G5	To G of fet 5
15	D5	To D of fet 5
16	G4	To G of fet 4
17	D4	To D of fet 4
18	V_{CC}	Power supply
19	D1	To D of fet 1
20	G1	To G of fet 1

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.6 ~ +10	V
Supply Current	I_{CC}	100	mA
Power Dissipation	P_D	600	mW
Operating Temperature Range	T_{OPR}	-40 ~ +85	°C
Storage Temperature Range	T_{STG}	-40 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ ELECTRICAL CHARACTERISTICS

(Measured at T_A=25°C, V_{CC}=3.3V(Note 1), R_{CAL1}=R_{CAL2}=36KΩ (setting ID1/2/4/5 to 10mA), R_{CALM}=68KΩ (setting ID3/6 to 5mA) unless otherwise stated)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range	V_{CC}		3.0		8.0	V
Supply Current	I_{CC}	I_{D1-6}=0		1.6	4.0	mA
	$I_{CC(L)}$	I_{D1-6}=10mA, no R_{CALM}		62	64	mA
Substrate Voltage	V_{CSUB}	I_{CSUB}=0	-3.0	-2.65	-2.0	V
	$V_{CSUB(L)}$	I_{CSUB}=-200uA		-2.55	-2.0	V
Oscillator Frequency	F_{OSC}		100	260	600	kHz
Gate Characteristics						
Gate (G1 to G6, resistor R_{CALM} ot present)						
Current Range	I_G		-100		+500	uA
Voltage Low	$V_{G(L)}$	I_D=12mA, I_G=-10uA	-3.0	-2.5	-2.0	V
Voltage High	$V_{G(H)}$	I_D=8mA, I_G= 0	0	0.7	1.0	V
Voltage Disabled (Note 1)	$V_{G(DIS)}$	I_D=0, I_G=-10uA, $V_{RCAL1-2}$=3.0V	-3.0	-2.5	-2.0	V
Gate (G3 and G6, resistor R_{CALM} present)						
Current Range	I_G		-100		+500	uA
Voltage Low	$V_{G(L)}$	I_D=6mA, I_G=-10uA	-3.0	-2.5	-2.0	V
Voltage High	$V_{G(H)}$	I_D=4mA, I_G=0	0	0.7	1.0	V
Voltage Disabled (Note 1)	$V_{G(DIS)}$	I_D=0, I_G=-10uA, V_{RCAL2}=V 3.0V	-3.0	-2.5	-2.0	V
Drain Characteristics						
Drain (D1 to D6, resistor R_{CALM} not present)						
Current Range	I_D		0		15	mA
Current Operating	$I_{D(OP)}$	Standard Application Circuit	8	10	12	mA
Current Disabled (Note 1)	$I_{D(DIS)}$	V_D=0, V_{RCAL}=3.0V			10	uA
Voltage Operating	$V_{D(OP)}$	I_D=10mA	1.8	2.0	2.2	V
Drain Characteristics						
Drain (D3 and D6, resistor R_{CALM} present)						
Current Range	I_{DM}		0.5		7.5	mA
Current Operating	$I_{DM(OP)}$	Standard Application Circuit	4	5	6	mA
Current Disabled (Note 1)	$I_{DM(DIS)}$	V_D=0, V_{RCAL}=3.0V, R_{CALM} not present			10	uA
Voltage Operating	$V_{DM(OP)}$	I_D=5mA	0.15	0.3	0.45	V

■ ELECTRICAL CHARACTERISTICS (Cont.)

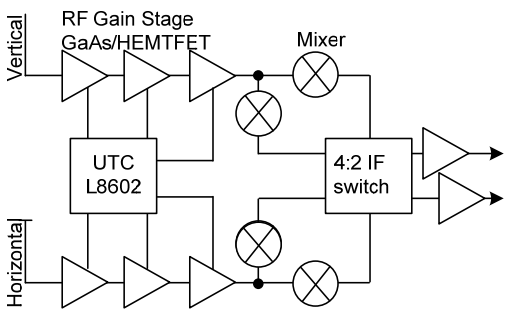
(Measured at T_A=25°C, V_{CC}=3.3V(Note 1), R_{CAL1}=R_{CAL2}=36KΩ (setting ID1/2/4/5 to 10mA), R_{CALM}=68KΩ (setting ID3/6 to 5mA) unless otherwise stated)

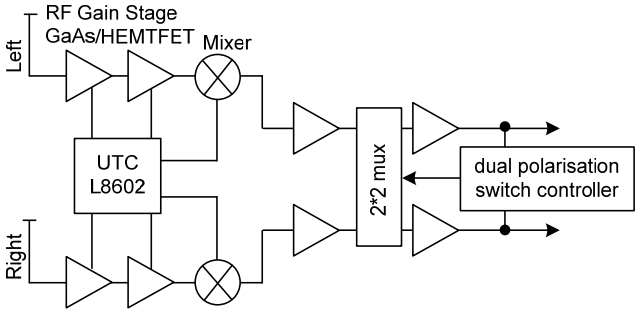
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{CAL} (1 and 2)						
Disable Threshold (Note 1)	$V_{RCAL(DIS)}$		1.8	2.7	3.0	V
Input Current	$I_{RCAL(DIS)}$	V_{RCAL}=3.0V		1.7	10	uA
R_{CALM}						
Disable Threshold (Note 1)	$R_{CALM(DIS)}$		1.5M	3.3M	5.0M	Ω
R_{CALM} Range	R_{CALM}		39k		390k	Ω
Voltage and Temperature dependence (R_{CALM} not present)						
delta I_D vs. V_{CC}	dI_D/dV_{CC}	V_{CC}=3.3 to 8.0V		1.2		%/V
delta I_D vs. T_{OP}	dI_D/dT_{OP}	T_{OP}=-40°C to +85°C		0.05		%/°C
delta V_D vs. V_{CC}	dV_D/dV_{CC}	V_{CC}=3.3 to 8.0V		0.05		%/V
delta V_D vs. T_{OP}	dV_D/dT_{OP}	T_{OP}=-40°C to +85°C		50		ppm/°C
Output Noise						
Drain Voltage	$V_{D(NOISE)}$	$C_{GATE-GND}$=10nF, $C_{DRAIN-GND}$=10nF			0.02	Vpk-pk
Gate Voltage	$V_{G(NOISE)}$	$C_{GATE-GND}$=10nF, $C_{DRAIN-GND}$=10nF			0.005	Vpk-pk

Notes: 1. To disable FET stages 3 and 6, pin R_{CAL2} must be set to 3V or above and pin R_{CALM} should be open circuit.

2. The characteristics are measured using up to three external reference resistors, R_{CAL1}, R_{CAL2} and R_{CALM}, wired from pins $R_{CAL1/2/M}$ to ground. Resistor R_{CAL1} sets the drain current of FETs 1 and 4. If R_{CALM} is not present, resistor R_{CAL2} sets the drain currents of FETs 2, 3, 5 and 6. If R_{CALM} is present, resistor R_{CAL2} sets the drain currents of FETs 2 and 5 and R_{CALM} sets the drain currents of FETs 3 and 6.
3. The negative bias voltages are generated on-chip using an internal oscillator. Two external capacitors, CNB and CSUB of value 47nF are required for this purpose.
4. The QFN-20(4×4) package exposed pad must either be connected to Csub or left open circuit.
5. Noise voltage measurements are made with FETs and gate and drain capacitors of value 10nF in place. Noise voltages are not measured in production.
6. ESD sensitive, handling precautions are recommended.

■ LNB SYSTEM DIAGRAM





■ TYPICAL APPLICATION CIRCUIT

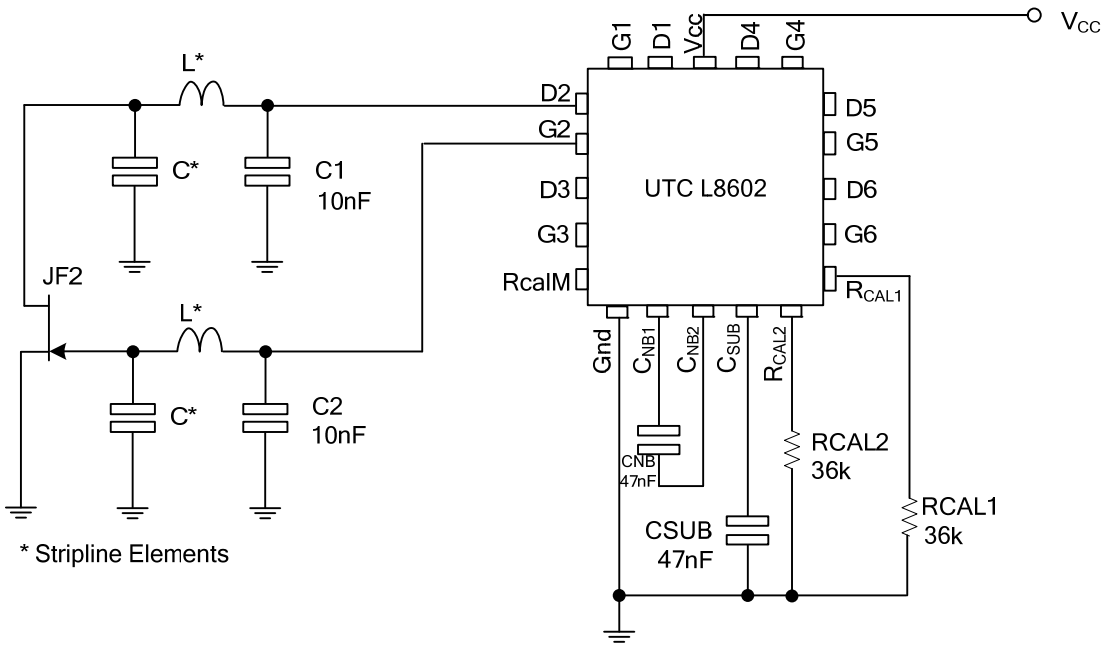
The UTC **L8602** series of devices are designed to meet the bias requirements of GaAs and HEMT FETs commonly used in satellite receiver LNBs with a minimum of external components whilst operating from a minimal voltage supply and using minimal current.

The truth table below shows the function of UTC **L8602**'s features.

L8602 truth table

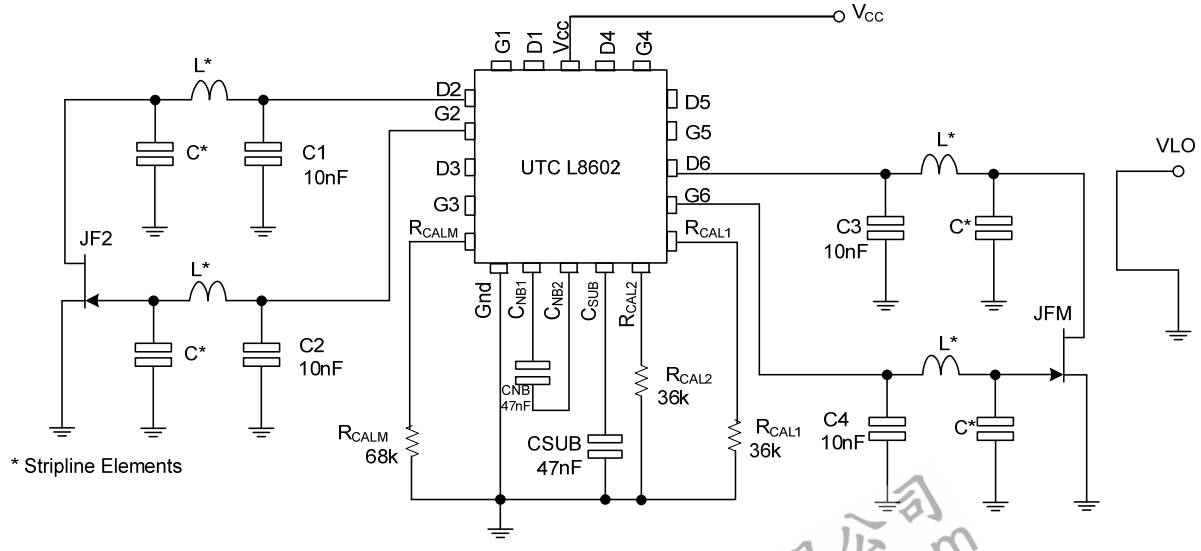
FEATURE	R_{CAL} Pin Resistor Termination			1st LNA Stages		FET Stage 2nd LNA Stages		3rd LNA/ Mixer Stages	
	R_{CAL1}	R_{CAL2}	R_{CALM}	Bias 1	Bias 4	Bias 2	Bias 5	Bias 3	Bias 6
6 LNA stages to provide standard bias to the GaAs or HEMT FET's	GND	GND	OPEN	on	on	on	on	on	on
	3V	GND	OPEN	off	off	on	on	on	on
	GND	3V	OPEN	on	on	off	off	off	off
Power down FET groups for LNA switching or power saving.	3V	3V	OPEN	off	off	off	off	off	off
4 LNA stages to provide standard bias to the GaAs or HEMT FET's plus 2 active mixer stages	GND	GND	GND	on	on	on	on	mixer	mixer
	GND	3V	GND	on	on	off	off	mixer	mixer
	3V	GND	GND	off	off	on	on	mixer	mixer
	3V	3V	GND	off	off	off	off	mixer	mixer

■ TYPICAL APPLICATION CIRCUIT (Cont.)



UTC L8602 in 6 LNA mode

The bias stages are split up into two groups, with the drain current of each group set by an external R_{CAL} resistor. R_{CAL1} sets the drain currents of stages 1 and 4, whilst R_{CAL2} sets the drain currents of stages 2, 3, 5 and 6. To ensure that the mixer function is disabled the R_{CALM} pin should be left open circuit.



UTC L8602 in 4 LNA and 2 active mixer mode

The bias stages are split up into three groups, with the drain current of each group set by an external R_{CAL} resistor. R_{CAL1} sets the LNA drain currents of stages 1 and 4, and R_{CAL2} sets the drain currents of LNA stages 2 and 5. R_{CALM} sets the mixer drain currents of stages 3 and 6.