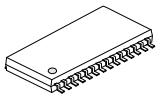
LAG665F

LINEAR INTEGRATED CIRCUIT

IC FOR HEADPHONE STEREOS



SOP-28

■ DESCRIPTION

The LAG665 is a monolithic integrated circuit, designed for was use in headphone stereos, and incorporates dual preamp, power amp, electronic VR and motor control circuits.

It can be used in a simple circuit configuration which requires very few external components.

■ FEATURES

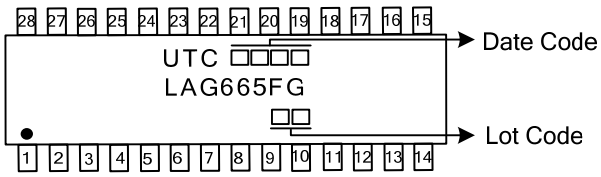
*1-Chip stereo tape recorder with motor speed controller.
*Operating supply voltage range: V_{CC}=2~5V
*Good volume control

■ ORDERING INFORMATION

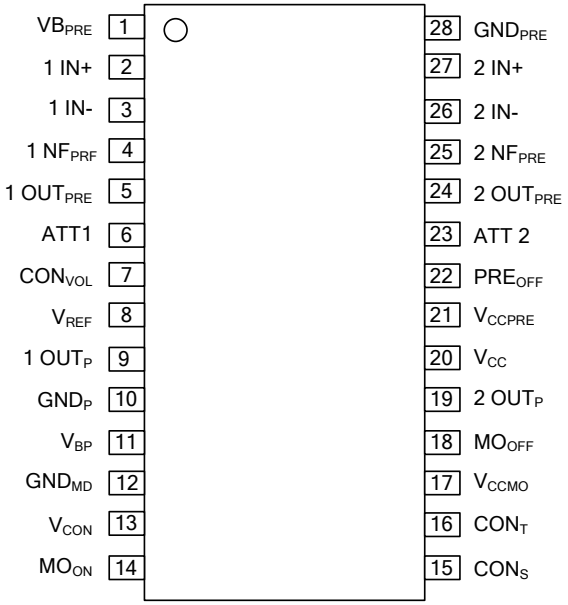
Ordering Number	Package	Packing
LAG665FG-S28-R	SOP-28	Tape Reel

LAG665FG-S28-R (1)Packing Type (2)Package Type (3)Green Package	(1) R: Tape Reel (2) S28: SOP-28 (3) G: Halogen Free and Lead Free

■ MARKING



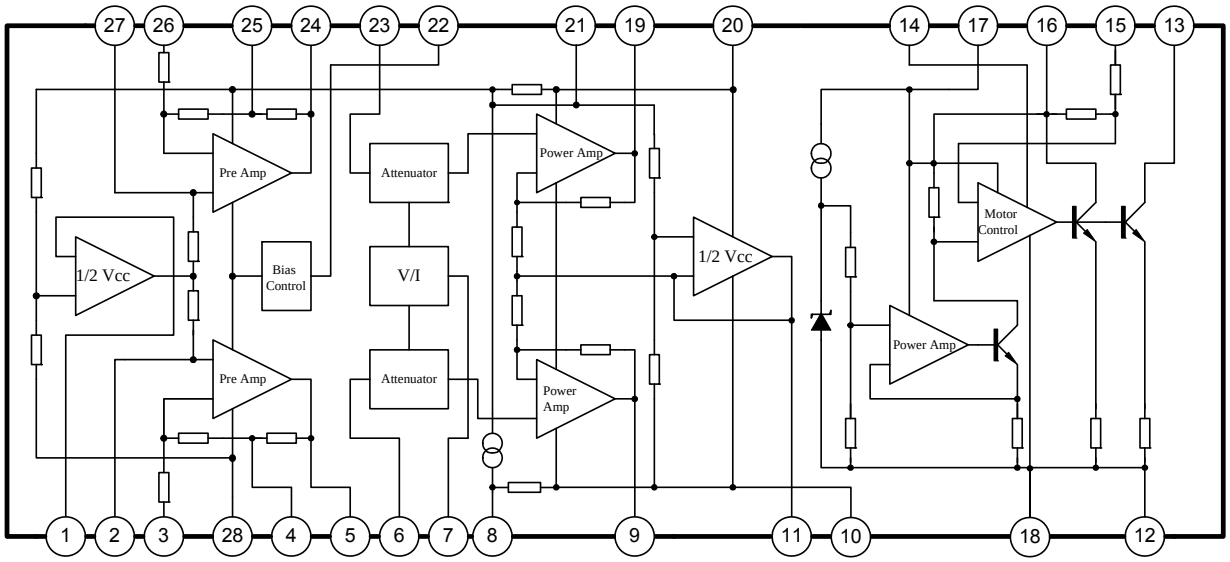
■ PIN CONFIGURATION



■ PIN FUNCTION DESCRIPTIONS

PIN NO.	SYMBOL	DESCRIPTION
1	VB_{PRE}	Pre Amp Bias Voltage
2	1 IN+	Channel 1 “+” Input
3	1 IN -	Channel 1 “-” Input
4	$1\ NF_{PRE}$	Feedback 1
5	$1\ OUT_{PRE}$	Pre Amp Output 1
6	ATT 1	Attenuator 1
7	CON_{VOL}	Volume Control
8	V_{REF}	Reference Voltage
9	$1\ OUT_{P}$	Power Amp Output 1
10	GND_{P}	Power GND
11	V_{BP}	Power Amp Bias Voltage
12	GND_{MD}	Motor GND
13	V_{CON}	Motor Control Voltage
14	MO_{ON}	Motor Forced Start
15	CON_{S}	Speed Control
16	CON_{T}	Torqul Control
17	V_{CCMO}	Motor Power Control
18	MO_{OFF}	Motor Forced Stop
19	$2\ OUT_{P}$	Power Amp Output 2
20	V_{CC}	Supply Voltage
21	V_{CCPRE}	Supply Voltage
22	PRE_{OFF}	Pre Amp Off
23	ATT 2	Attenuator 2
24	$2\ OUT_{PRE}$	Pre Amp Output 2
25	$2\ NF_{PRE}$	Feedback 2
26	2 IN-	Channel 2 “-” Input
27	2 IN+	Channel 2 “+” Input
28	GND_{PRE}	Pre GND

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	-0.3~+7.5	V
Power Dissipation	P_D	450	mW
Operating Voltage	V_{OP}	2~5	V
Operating Temperature	T_{OPR}	-20~+65	°C
Storage Temperature	T_{STG}	-40~+125	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ ELECTRICAL CHARACTERISTICS (V_{CC}=6V,T_A=25°C, unless otherwise specified)

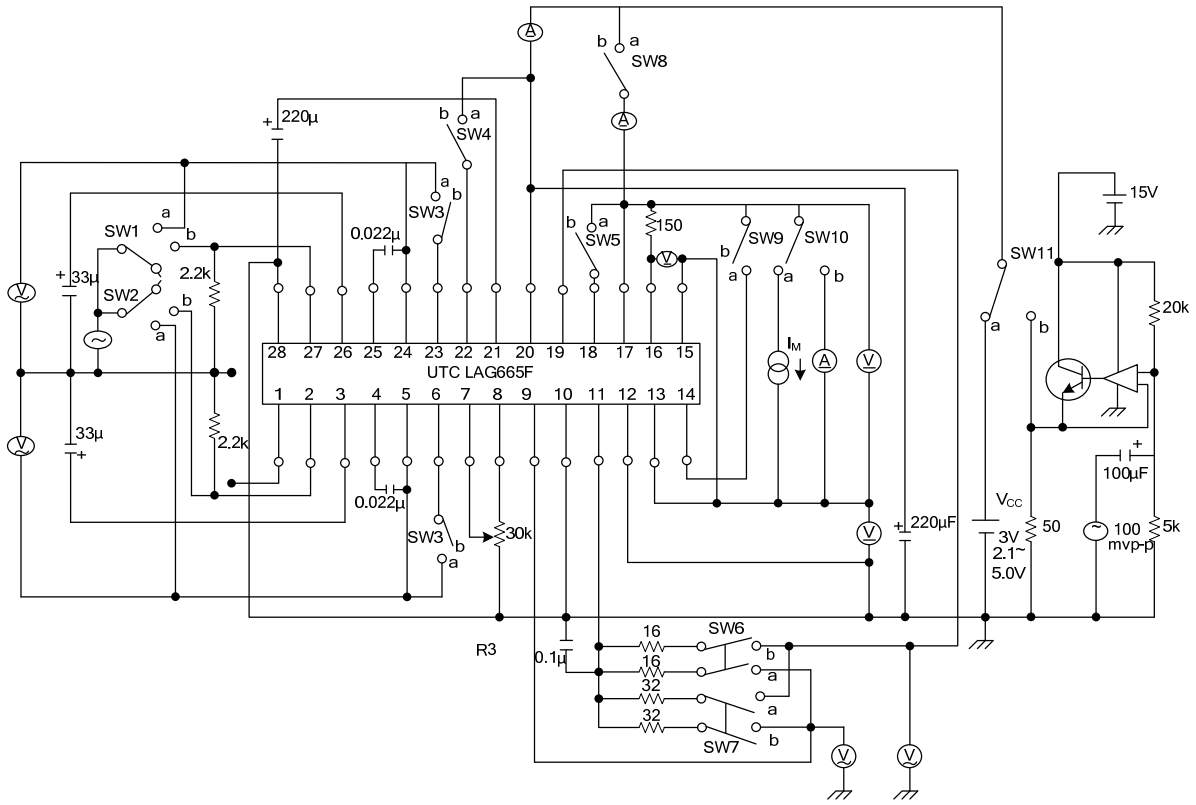
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Current	I_{CC}	V_{IN}=0V, I_M=0mA		18	25	mA
PRE-AMPLIFIER (V_{CC}=3.0V, f=1kHz)						
Open Loop Gain	G_{VO}	V_O=-10dBm, R_L=∞		72		dB
Close Loop Gain	G_{VC}	V_O=-10dBm	40	42	44	dB
Maximum Output Voltage	V_{OM}	THD=10%	0.45	0.6		V_{RMS}
Total Harmonic Distortion	THD	V_{OUT}=400mV_{Rms}		0.05	0.5	%
Output Noise Voltage	V_{ON}	V_{IN}=0, R_G=2.2k, BPF(30~20kHz)		150	300	μV_{RMS}
Input Impedance	Z_{IN}	V_{OUT} =-10dBm	18	22		kΩ
Cross Talk between CH	CT	R_G=2.2k, V_{OUT}=-10dBm	30			dB
Output Voltage when Pre-Off	V_{O_OFF}	V_{IN}=100mV_{Rms}			-50	dB
Output Impedance when Pre-Off	R_{O_OFF}			10		kΩ
Input Impedance when Pre-Off	R_{I_OFF}			10		KΩ
Attenuator (V_{CC}=3.0V, f=1kHz, R_L=16Ω)						
Maximum Input Voltage	V_{I_MAX}		0.2			V_{RMS}
Maximum Attenuation	V_{A_MAX}	V_{CONT}=Min	66			dB
Attenuation Error	V_{AERR}	V_{CONT}=Max		0		dB
Input Impedance	Z_{IA}		15	20		kΩ
Control Ternimal Input Impedance	Z_{ICOT}		100			kΩ
Power Amplifier (V_{CC}=3.0V, f=1kHz, R_L=16Ω)						
Voltage Gain	GV	P_{OUT}=5mW	26	28	30	dB
Channel Voltage Difference	ΔGV	V_{CONT}=Max		0	3	dB
Maximum Output Power I	P_{OM} 1	THD=10%, R_L=32Ω	20	28		mW
Maximum Output Power II	P_{OM} 2	THD=10%, R_L=16Ω	30			mW
Total Harmonic Distortion	THD	P_{OUT}=5mW		0.2	2	%
Cross Talk between CH	C_T	P_{OUT}=5mW	20	30		dB
Output Noise Voltage	V_{ON}	R_G=2.2k, V_{CONT}=Min		0.25	1.0	mV_{RMS}
Ripple Rejection	RR	V_{CC}=3V, 100Hz, 100mVp-p	34	40		dB
Pre + Pulse Boost + Power Noise	V_{NTO}	V_{IN}=0V, R_G=2.2k, V_{CONT}=Max		6	9	mV_{RMS}

■ ELECTRICAL CHARACTERISTICS (V_{CC}=6V,T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Motor Comtrol (V_{CC}=3V, I_M=100mA)						
Current Consumption	IMC			3	5	mA
Starting Current	IMS		500			mA
Reference Voltage	V_{REF}	Pin 15~Pin 16	0.72	0.8	0.87	V
Reference Voltage Change I	V_{REF} 1	V_{CC}=2.1~5V (Note)		0.05		%/V
Reference Voltage Change II	V_{REF} 2	I_M=25~250mA		0.01		%/mA
Reference Voltage Change III	V_{REF} 3	T_A=-10~50°C		0.01		%/°C
Current Factor	K		32	38	43	
Current Factor Change I	K1	V_{CC}=2.1~5V		0.5		%/V
Current Factor Change II	K2	I_M=25~250mA		0.05		%/mA
Current Factor Change III	K3	T_A=-10~50°C		0.02		%/°C
Saturation Voltage at Forced ON	V_{CESA}	I_M=200mA, Pin 14=V_{CC}			0.6	V
Input Impedance at Forced ON Pin	R_{ION}			5.6		KΩ
Leakage Current at Forced OFF	IML				200	μA
Input Impedance at Forced OFF Pin	R_{ICON}			33		KΩ

Note: Voltage across pins 13 and 19 (motor pins) fluctuates.

■ TEST CIRCUIT



■ SWITCH MATRIX

ITEM	SYMBOL	SW No.											TEST CONDITION
		1	2	3,3'	4	5	6	7	8	9	10	11	V_{CC}=3V, f=1kHz, R_L=16Ω
AMP													
Supply Current	I_{CC}	c	c	a	b	b	a	b	b	b	a	a	I_M=0mA, V_R=max
Close Loop Gain	G_{VC}	b	b	b	b	b	a	b	b	b	a	a	V_O=-10dBM
Maximum Output Voltage	V_{OM}	b	b	b	b	b	a	b	b	b	a	a	THD=10%
Total Harmonic Distortion	THD	b	b	b	b	b	a	b	b	b	a	a	V_O=400mV
Output Noise Voltage	V_{ON}	c	c	b	b	b	a	b	b	b	a	a	B.P.F.(20~30kHz)
Cross Talk between CH	C_T	b/c	c/b	b	b	b	a	b	b	b	a	a	V_O=244mV, V_O=-10dBM
Output Voltage when Preamp Off	V_{O_OFF}	b	b	b	a	b	a	b	b	b	a	a	V_{IN}=100mV_{RMS}
Attenuator													
Maximum Input Voltage	V_{I_MIX}	a	a	a	a	b	a	b	b	b	a	a	V_R=Mid, THD=10%
Maximum Attenuation	V_{A_MAX}	a	a	a	a	b	a	b	b	b	a	a	Difference in V_O output when V_R=max. and output voltage when V_R=min
Power AMP													
Voltage Gain	GV	a	a	a	a	b	a	b	b	b	a	a	P_{OUT}=5mV
Channel Voltage Difference	ΔGV	a	a	a	a	b	a	b	b	b	a	a	Channel output difference at V_R=max
Maximum Output Power I	P_{OM} 1	a	a	a	a	b	b	a	b	b	a	a	R_L=32Ω, THD=10%
Maximum Output Power II	P_{OM} 2	a	a	a	a	b	a	b	b	b	a	a	R_L=16Ω, THD=10%
Total harmonic distortion ratio	THD	a	a	a	a	b	a	b	b	b	a	a	P_{OUT}=5mW
Crosstalk between channels	C_T	a/c	c/a	a	a	b	a	b	b	b	a	a	P_{OUT}=5mW measured with channels swapped output voltage when V_R=min
Output noise voltage	V_N	c	c	a	b	b	a	b	b	b	a	a	V_R=min
Ripple Rejection	RR	c	c	b	a	b	a	b	b	b	a	b	V_R=max
Pre+power noise	V_{NTO}	c	c	a	b	b	a	b	b	b	a	a	V_R=max
Consumption current	I_{MC}	c	c	a	a	b	a	b	a	b	a	a	I_M=0mA
Startup current	I_{MS}	c	c	a	a	b	a	b	a	b	b	a	
Reference voltage	VREF	c	c	a	a	b	a	b	a	b	a	a	I_M=100mA (15~16 Pin)
Reference voltage fluctuation I	V_{REF1}	c	c	a	a	b	a	b	a	b	a	a	I_M=100mA, V_{CC}=2.1~5.0V (13~17 Pin)
Reference voltage fluctuation II	V_{REF2}	c	c	a	a	b	a	b	a	b	a	a	V_{CC}=3.0V, I_M=25~250mA

■ SWITCH MATRIX (Cont.)

ITEM	SYMBOL	SW No.											TEST CONDITION
		1	2	3,3'	4	5	6	7	8	9	10	11	V_{CC}=3V, f_{OSC}=1kHz, R_L=16Ω
Output voltage on forced on	V_{CESA}	c	c	a	a	a	a	b	a	b	a	a	I_M=200mA
Leakage current on forced off	IML	c	c	a	a	b	a	b	a	a	b	a	