



## LR1965

Preliminary

CMOS IC

### 1.5A, LOW DROPOUT REGULATOR WITH POWER GOOD

#### DESCRIPTION

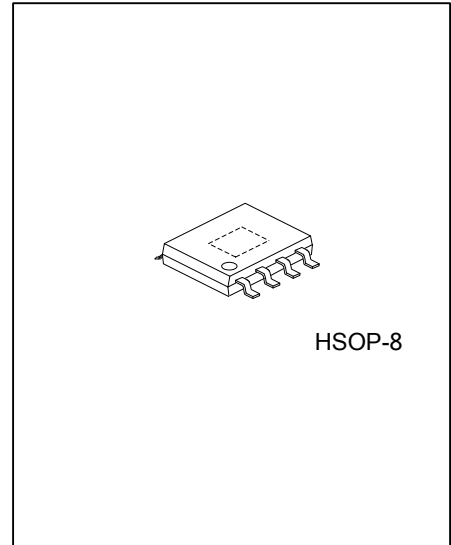
The **UTC LR1965** is CMOS-based positive voltage and a very low dropout regulator IC that minimum input voltage is 2.5V and is capable of delivering the continuous output load current up to 1.5A.

It has features of low dropout (maximum 300mV at 1A), a very low quiescent current (typically 300uA at 0.1A) and very high PSRR up to 86dB at 1A load current.

The output voltage can be set from 0.8V to ( $V_{IN} - V_{DRP}$ ) with an external resistor divider and it has  $\pm 2\%$  accuracy through all temperature ranges include the line as well as load variations. It is allowed to use a small 4.7 $\mu$ F MLCC input and output capacitor to deliver the current with the stable operation.

Built-in Soft-Start function reduces the inrush current and the other features are include over current protection (OCP), short-circuit protection (SCP), and thermal shut down protection (TSD).

The **UTC LR1965** is available in 8-SOP-EP package with exposed pad for optimal power dissipation and 8-TDFN (3x3mm).



#### FEATURES

- \* Input Voltage Range: 2.5V~6.0V
- \* Supply Current : Typ. 300uA
- \* Current limit : Min. 1.8A
- \* Adjustable Output from 0.8V
- \* LR1965: Typ 0.4V Dropout @  $I_{OUT}=1.5A$
- \* Compatible with MLCC Capacitors
- \* Built-in Soft-Start Limits Inrush Current
- \* Built-in Thermal Shutdown Protection
- \* Built-in Over Current & Short Circuit Protection

#### ORDERING INFORMATION

| Ordering Number  |                  | Package | Packing   |
|------------------|------------------|---------|-----------|
| Lead Free        | Halogen Free     |         |           |
| LR1965L-xx-SH2-R | LR1965G-xx-SH2-R | HSOP-8  | Tape Reel |

Note: xx: Output Voltage, refer to Marking Information.

|                  |  |  |
|------------------|--|--|
| LR1965G-xx-SH2-R | (1) Packing Type<br>(2) Package Type<br>(3) Output Voltage Code<br>(4) Green Package | (1) R: Tape Reel<br>(2) SH2: HSOP-8<br>(3) xx: refer to Marking Information<br>(4) G: Halogen Free and Lead Free, L: Lead Free |
|------------------|--|--|

| PACKAGE | VOLTAGE CODE | MARKING  |
|---------|--------------|--|
| HSOP-8  | AD: ADJ      | <p>Diagram illustrating the marking on the HSOP-8 package. The package is shown with pins numbered 1 through 8. The marking includes:</p> <ul style="list-style-type: none"> <li>Date Code (pins 8, 7, 6, 5)</li> <li>UTC (pins 4, 3, 2, 1)</li> <li>LR1965 (pins 4, 3, 2, 1)</li> <li>Lot Code (pins 4, 3, 2, 1)</li> </ul> <p>Output Voltage is indicated by an arrow pointing to the package.</p> |

OUT 1

OUT 2

FB 3

GND 4

8  $V_{IN}$

7  $V_{IN}$

6 EN

5 PG

GND

| PIN NO. | PIN NAME        | DESCRIPTION   |
|---------|-----------------|---|
| 1, 2    | OUT             | Voltage Regulator Output Pin  |
| 3       | FB              | Feedback Pin. Connect to output through a voltage-divider to set the output.<br>Recommended that the tolerance of feedback resistors is below 1%. |
| 4       | GND             | Ground Pin  |
| 5       | PG              | Open Drain Power-Good (PG) Output.  |
| 6       | EN              | Chip Enable Pin   |
| 7, 8    | V <sub>IN</sub> | Input Supply Voltage Pin.   |

The block diagram illustrates the control system for the DC-DC converter. The input voltage  $V_{IN}$  is connected to the positive input of the Error AMP. The output of the Error AMP drives the gate of the power MOSFET. The MOSFET's source is connected to ground, and its drain is connected to the output terminal OUT. The feedback signal is taken from OUT and connected to the FB pin. The FB pin is also connected to the OCP/TSD block. The EN pin is connected to the input of an inverter, whose output is connected to the Error AMP. The GND pin is connected to the negative input of the Error AMP and the source of the MOSFET. The Power Good Control block is connected to the FB pin and the gate of the MOSFET. The output of the Power Good Control block is connected to the gate of the MOSFET. The MOSFET's drain is also connected to the output terminal OUT. The output terminal OUT is connected to the FB pin and the PG pin. The PG pin is connected to the Power Good Control block. The Power Good Control block is also connected to the gate of the MOSFET. The MOSFET's source is connected to ground. The input voltage  $V_{IN}$  is connected to the positive input of the Error AMP. The output of the Error AMP drives the gate of the power MOSFET. The MOSFET's source is connected to ground, and its drain is connected to the output terminal OUT. The feedback signal is taken from OUT and connected to the FB pin. The FB pin is also connected to the OCP/TSD block. The EN pin is connected to the input of an inverter, whose output is connected to the Error AMP. The GND pin is connected to the negative input of the Error AMP and the source of the MOSFET. The Power Good Control block is connected to the FB pin and the gate of the MOSFET. The output of the Power Good Control block is connected to the gate of the MOSFET. The MOSFET's drain is also connected to the output terminal OUT. The output terminal OUT is connected to the FB pin and the PG pin. The PG pin is connected to the Power Good Control block. The Power Good Control block is also connected to the gate of the MOSFET. The MOSFET's source is connected to ground. The input voltage  $V_{IN}$  is connected to the positive input of the Error AMP. The output of the Error AMP drives the gate of the power MOSFET. The MOSFET's source is connected to ground, and its drain is connected to the output terminal OUT. The feedback signal is taken from OUT and connected to the FB pin. The FB pin is also connected to the OCP/TSD block. The EN pin is connected to the input of an inverter, whose output is connected to the Error AMP. The GND pin is connected to the negative input of the Error AMP and the source of the MOSFET. The Power Good Control block is connected to the FB pin and the gate of the MOSFET. The output of the Power Good Control block is connected to the gate of the MOSFET. The MOSFET's drain is also connected to the output terminal OUT. The output terminal OUT is connected to the FB pin and the PG pin. The PG pin is connected to the Power Good Control block. The Power Good Control block is also connected to the gate of the MOSFET. The MOSFET's source is connected to ground.

■ ABSOLUTE MAXIMUM RATING ( $T_A=25^{\circ}\text{C}$  unless otherwise specified)

| PARAMETER            | SYMBOL        | RATINGS             | UNIT                 |
|----------------------|---------------|---------------------|----------------------|
| Input Voltage        | $V_{IN}$      | -0.3 ~ 7            | V                    |
| Output Voltage       | OUT           | -0.3 ~ $V_{IN}+0.3$ | V                    |
| Junction to Ambient  | $\theta_{JA}$ | 50                  | $^{\circ}\text{C/W}$ |
| Junction to Case     | $\theta_{JC}$ | 10                  | $^{\circ}\text{C/W}$ |
| Junction Temperature | $T_J$         | +150                | $^{\circ}\text{C}$   |
| Storage Temperature  | $T_{STG}$     | -65 ~ +150          | $^{\circ}\text{C}$   |

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

| PARAMETER                 | SYMBOL   | RATINGS   | UNIT               |
|---------------------------|----------|-----------|--------------------|
| Input Voltage Range       | $V_{IN}$ | 2.5 ~ 6.0 | V                  |
| Ambient Temperature Range | $T_A$    | -40 ~ +85 | $^{\circ}\text{C}$ |

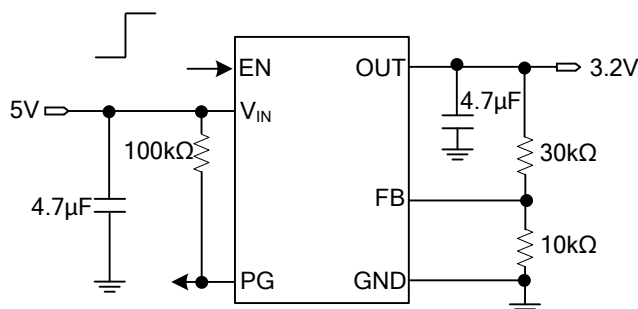
■ ELECTRICAL CHARACTERISTICS

All parameters are guaranteed over the operational supply voltage and temperature range. Operating conditions unless otherwise noted are:  $V_{IN}=5\text{V}$ ,  $\text{OUT}=2.5\text{V}$  and  $T_A=25^{\circ}\text{C}$ . Typical values are for information only.

| PARAMETER                              | SYMBOL      | TEST CONDITIONS  | MIN  | TYP   | MAX | UNIT               |
|--|-------------|--|------|-------|-----|--------------------|
| <b>Supply Voltage</b>                  |             |  |      |       |     |                    |
| Quiescent Current                      | $I_Q$       | $I_{OUT}=100\text{mA}$   |      | 300   |     | $\mu\text{A}$      |
| Shutdown Current                       | $I_{STD}$   | $V_{IN}=6\text{V}$ , $V_{EN}=\text{GND}$                                     |      | 0.2   | 2   | $\mu\text{A}$      |
| <b>Feedback (FB)</b>                   |             |  |      |       |     |                    |
| Feedback Voltage Accuracy              | $V_F$       | $I_{OUT}=10\text{mA}$ , $T_A=25^{\circ}\text{C}$                             | 784  | 800   | 816 | mV                 |
| Input Bias Current                     | $I_F$       | $V_{FB}=0.8\text{V}$ , $V_{IN}=6\text{V}$                                    |      | 0.001 | 0.1 | $\mu\text{A}$      |
| <b>Output (OUT)</b>                    |             |  |      |       |     |                    |
| Output Accuracy                        | $V_{OUT}$   |  | -2   |       | 2   | %                  |
| Load Regulation                        | $R_{LO}$    | $I_{OUT}=1\text{mA}$ to 1.5A   |      | 0.1   | 2   | %/A                |
| Line Regulation                        | $R_{LN}$    | $V_{IN}=2.2\sim 6\text{V}$ , $V_{OUT}=1.225\text{V}$ , $I_{OUT}=1\text{mA}$  | -0.2 |       | 0.2 | %/V                |
| Dropout Voltage                        | $V_{DRP}$   | $I_{OUT}=1.5\text{A}$ , $V_{FB}=768\text{mV}$                                |      | 400   |     | mV                 |
|  |             | $I_{OUT}=1\text{A}$ , $V_{FB}=768\text{mV}$                                  |      | 140   | 280 |                    |
|  |             | $I_{OUT}=0.5\text{A}$ , $V_{FB}=768\text{mV}$                                |      |       | 200 |                    |
| Current Limit                          | $I_C$       |  | 1.8  |       |     | A                  |
| Load transient (Note 1)                | $L_{OT}$    | $I_{OUT}=20\text{mA}$ to 1.5A,   |      | 3     |     | %                  |
| Line Transient (Note 1)                | $R_{NT}$    | $\Delta V_{IN}=0.5\text{V}$  |      | 3     |     | %                  |
| <b>Enable (EN)</b>                     |             |  |      |       |     |                    |
| Input Threshold                        | $V_{ENH}$   | EN rising, $V_{IN}=\text{OUT}+1\text{V}\sim 6\text{V}$                       | 1.2  |       |     | V                  |
|  | $V_{ENL}$   | EN falling, $V_{IN}=\text{OUT}+1\text{V}\sim 6\text{V}$                      |      |       | 0.4 |                    |
| Input Bias Current                     | $I_{EN}$    | EN=0 or 6V   | -1   | 0     | 1   | $\mu\text{A}$      |
| <b>Power Good (PG)</b>                 |             |  |      |       |     |                    |
| Threshold Voltage                      | $P_{V1}$    | FB high, $V_{HYS}=10\text{mV}$ , $V_{IN}=\text{OUT}+1\text{V}\sim 6\text{V}$ | 835  | 880   | 924 | mV                 |
|  | $P_{V2}$    | FB low, $V_{HYS}=10\text{mV}$ , $V_{IN}=\text{OUT}+1\text{V}\sim 6\text{V}$  | 652  | 688   | 760 | mV                 |
| Output Voltage Low                     | $P_{CL}$    | FB=0.6V or 1.0V, $I_{PG}=1\text{mA}$   |      | 25    | 200 | mV                 |
| Output Current High                    | $P_{CH}$    | $P_{WRGD}=6\text{V}$   |      | 0.001 | 0.1 | $\mu\text{A}$      |
| Rising Delay Time                      | $P_{RDT}$   | From FB*90% to PG  |      | 150   |     | $\mu\text{s}$      |
| Falling Delay Time 1                   | $P_{FDT1}$  | $V_{IN}=2.5\text{V}$ , From FB to PG   | 20   | 70    | 120 | $\mu\text{s}$      |
| Falling Delay Time 2                   | $P_{FDT2}$  | $V_{IN}=6\text{V}$ , From FB to PG   | 60   | 180   | 300 | $\mu\text{s}$      |
| <b>Thermal Shutdown (TSD) (Note 1)</b> |             |  |      |       |     |                    |
| TSD Threshold                          | $T_{SDON}$  | TSD On   |      | 165   |     | $^{\circ}\text{C}$ |
|  | $T_{SDOFF}$ | TSD Off  |      | 145   |     | $^{\circ}\text{C}$ |

Note: Guaranteed by design but not production tested.

■ TYPICAL APPLICATION CIRCUIT



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