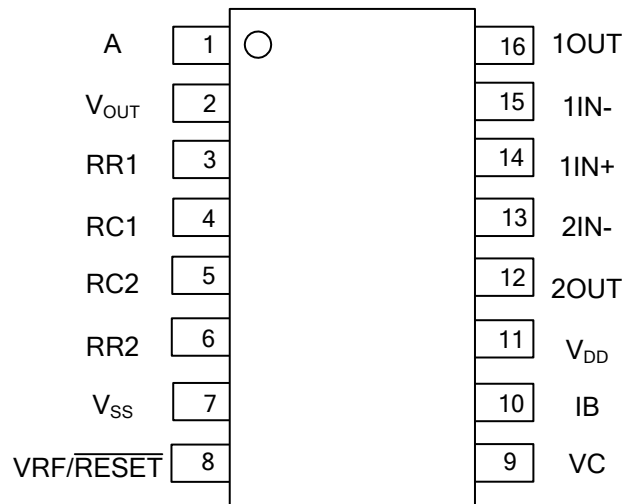


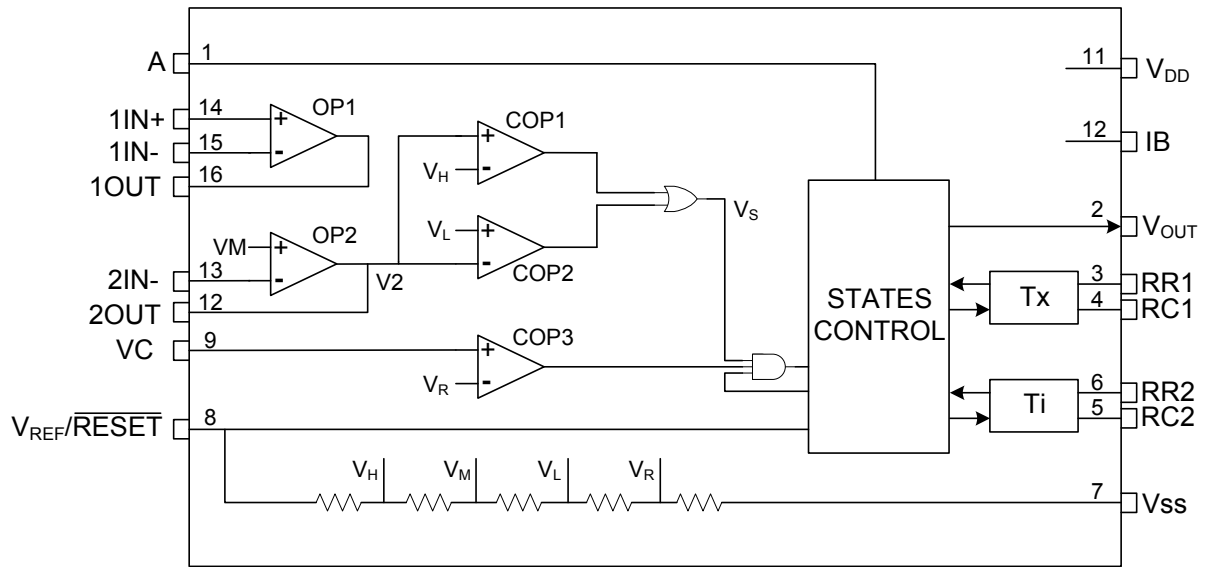
■ PIN CONFIGURATIONS



■ PIN DESCRIPTIONS

PIN NO.	PIN NAME	I/O	PIN DESCRIPTION
1	A	I	Retriggerable & non-retriggerable mode select
2	V _{OUT}	O	Detector output pin (active high)
3	RR1		Output pulse width control (Tx)
4	RC1		Output pulse width control (Tx)
5	RC2		Trigger inhibit control (Ti)
6	RR2		Trigger inhibit control (Ti)
7	V _{SS}		Ground
8	VRF	I	RESET & voltage reference input (normally high. Low=reset)
9	VC	I	Trigger disable input (VC>0.2V _{DD} =enable; VC<0.2V _{DD} =disable)
10	IB		Op-amp input bias current setting
11	V _{DD}		Supply voltage
12	2OUT	O	2 nd stage Op-amp output
13	2IN-	I	2 nd stage Op-amp inverting input
14	1IN+	I	1 st stage Op-amp non-inverting input
15	1IN-	I	1 st stage Op-amp inverting input
16	1OUT	O	1 st stage Op-amp output

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

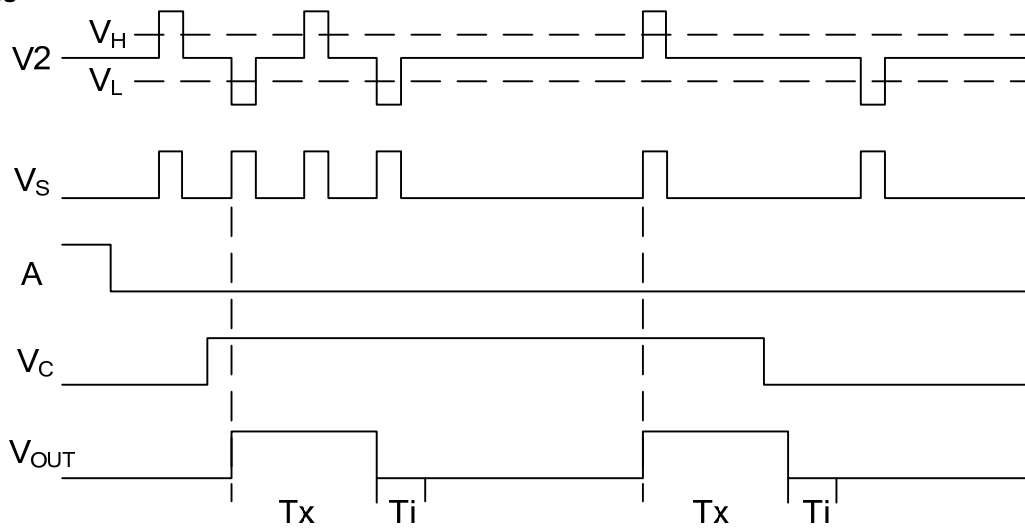
PARAMETER	SYMBOL	RATINGS	UNIT
DC Supply Voltage	V_{DD}	-0.3~6.0	V
Input/ Output Voltage	V_{IN}/V_{OUT}	$V_{SS}-0.3\sim V_{DD}+0.3$	V
Max. Output Current ($V_{DD}=5.0V$)	I_{OUT}	10	mA
Operating Temperature	T_{OPR}	-20~+70	°C
Storage Temperature	T_{STG}	-40~+125	°C

■ DC ELECTRICAL CHARACTERISTICS ($T_A = +25^{\circ}C$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC Supply Voltage	V_{DD}		3		5	V
Average Supply Current	I_{DD}	No Load			50	μA
		$V_{DD}=3V$			100	
		$V_{DD}=5V$			100	
Op-Amp Input Offset Voltage	V_{OS}	$V_{DD}=5V$			50	mV
Op-Amp Input Offset Current	I_{OS}	$V_{DD}=5V$			50	nA
Op-Amp Gain	A_{VO}	$V_{DD}=5V, R_L=1.5M\Omega$	60			dB
Op-Amp Common Mode Rejection Ration	CMRR	$V_{DD}=5V, R_L=1.5M\Omega$	60			dB
Op-Amp HIGH Level Output Voltage	V_{YH}	$V_{DD}=5V, R_L=500K\Omega$ connect to $1/2V_{DD}$	4.25			V
Op-Amp LOW Level Output Voltage	V_{YL}		0.75			V
V_C High Level Input Voltage	V_{RH}	$V_{RF}=V_{DD}=5V$	1.1			V
V_C Low Level Input Voltage	V_{RL}		0.9			V
V_{OUT} High Level Output Voltage	V_{OH}	$V_{DD}=5V, I_{OH}=0.5mA$	4			V
V_{OUT} Low Level Output Voltage	V_{OL}	$V_{DD}=5V, I_{OH}=0.1mA$			0.4	V
Pin A High Level Input Voltage	V_{AH}	$V_{DD}=5V$	3.5			V
Pin A Low Level Input Voltage	V_{AL}	$V_{DD}=5V$			1.5	V

■ FUNCTIONAL DESCRIPTIONS

1. Re-Triggerable Mode



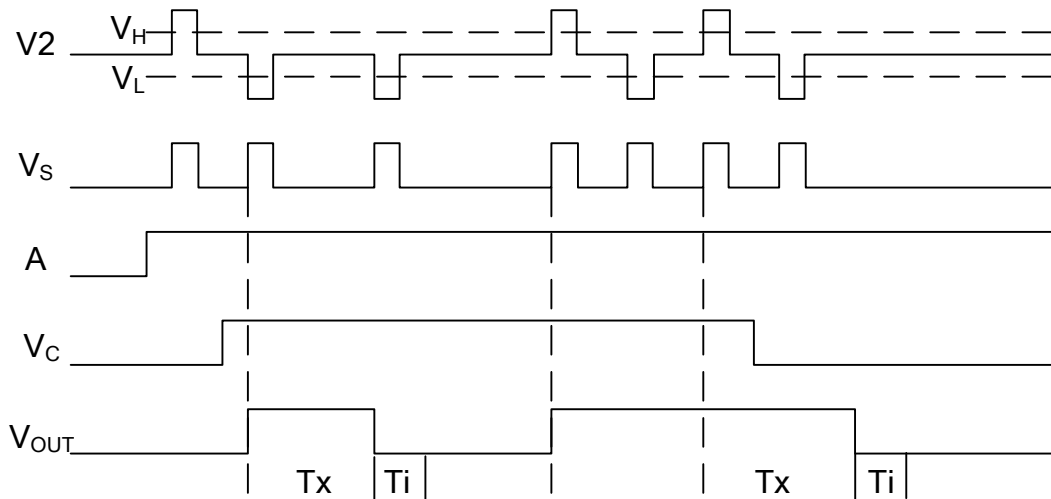
Re-Triggerable Waveform

Operational amplifier OP1 composed sensor signal pre-processing circuit. The amplified signal coupled to the operational amplifier OP2, and elevated DC level to $V_M (\approx 0.5V_{DD})$, The output signal V_2 input to Bi-directional level detector(COP1&COP2), detected the effective signal V_s . As the $V_H \approx 0.7V_{DD}$, $V_L \approx 0.3V_{DD}$, while $V_{DD} = 5V$, it is immune to the $\pm 1V$ noise interference and can improve system reliability.

COP3 is a condition comparator. When the input voltage $V_c < V_R (\approx 0.2V_{DD})$, COP3 output is low, it disabled the V_s transmission to State Control circuit; When $V_c > V_R$, COP3 output is high, chip access to extension time period.

When pin A connect to "0", any change of V_2 have been ignored until the end of T_x period, which called non-retriggerable mode. When the T_x period ended, V_o jump back to the low level, chip access to the lock period T_i . During the T_i period, any changes of V_2 can not make V_o jumping to valid state (high level), it can inhibit a variety of interference when the load changed.

2. Non-Retriggerable mode

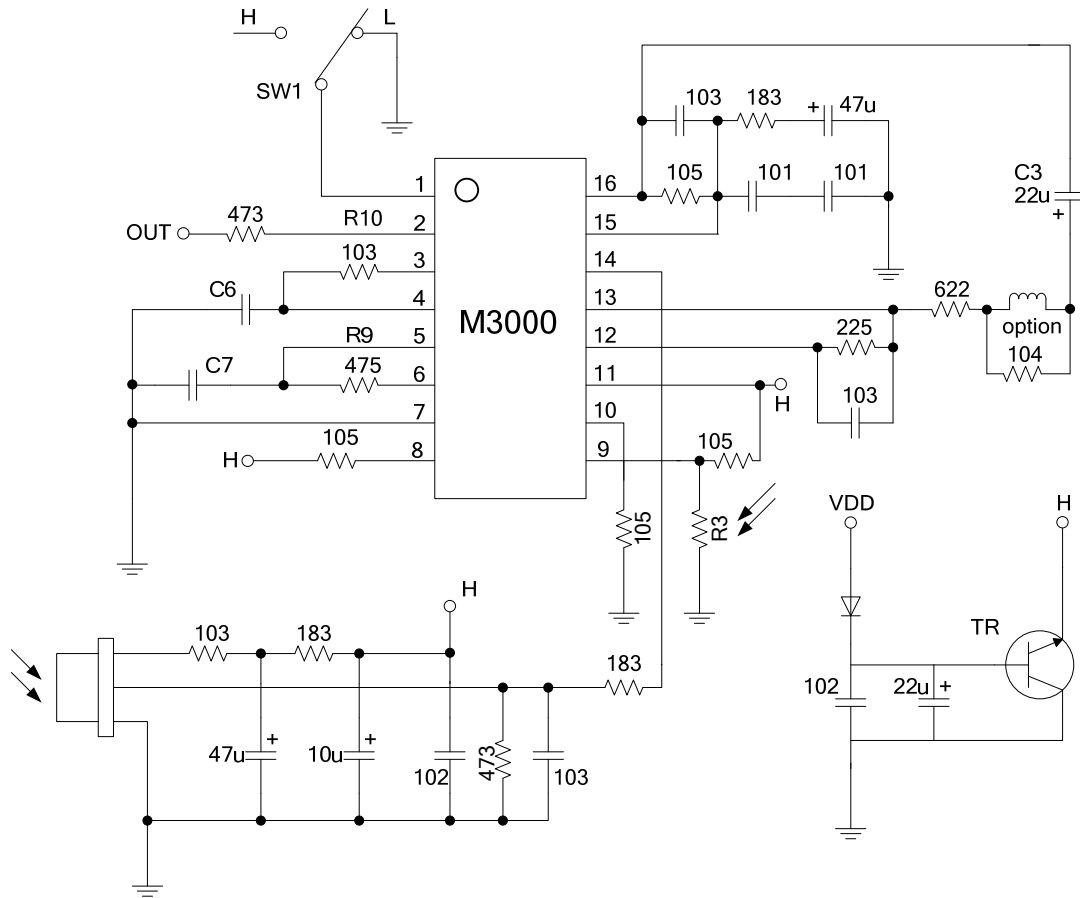


Non-Retriggerable Waveform

During the time of $V_c = "0"$, $A = "0"$, signal V_s can not trigger V_o to a valid state; When $V_c = "1"$, $A = "1"$, V_s can repeatable trigger V_o to the valid state, and keep the state in T_x period.

In the T_x period, if V_s jump to "1", then V_o extend to an another T_x ; if V_s keep "1" state, V_o maintains the valid state; if V_s keep "0" state, after the period of T_x , V_o change to invalid state, and in the T_i time, any change of V_s can not trigger V_o to a valid state.

■ TYPICAL APPLICATIONS CIRCUIT



NOTE: R3 is a light dependent resistor which has low resistance under strong ambient light. This cause the detector to be operational only when the detection area is sufficient dark.

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