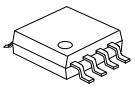
M7085

CMOS IC

PFM STEP-DOWN DC-DC CONTROLLER



MSOP-8

■ DESCRIPTION

The UTC **M7085** step-down DC-DC Controller is optimized for use with a power PMOSFET. It utilize a Pulse-Frequency Modulation (PFM) control scheme that implies high efficiency operation at light loads.

There are two user-selectable over-current protection methods one provides over-current protection by taking advantage of the $R_{DS(ON)}$ of the P- Channel. The other provides accurate over-current protection with the use of an external sense resistor. The cycle-by-cycle current limit threshold can be adjusted with a external resistor.

■ FEATURES

* High efficiency 90% and up is possible
* Low dropout operation：100% duty cycle
* Maximum operating frequency > 1MHz
* Two methods of over-current protection
* 4.5V ~ 35V wide input range
* 1.24V ~ V_{IN} adjustable output range

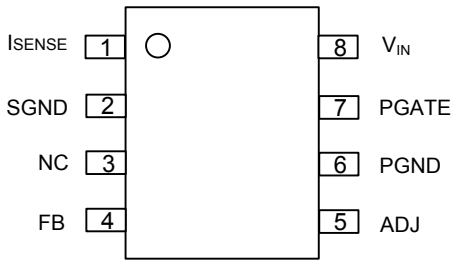
■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
M7085L-SM1-R	M7085G-SM1-R	MSOP-8	Tape Reel
M7085L-SM1-T	M7085G-SM1-T	MSOP-8	Tube

M7085L-SM1-R
(1)Packing Type
(2)Package Type
(3)Lead Free

(1) R: Tape Reel, T: Tube
(2) SM1: MSOP-8
(3) G: Halogen Free, L: Lead Free

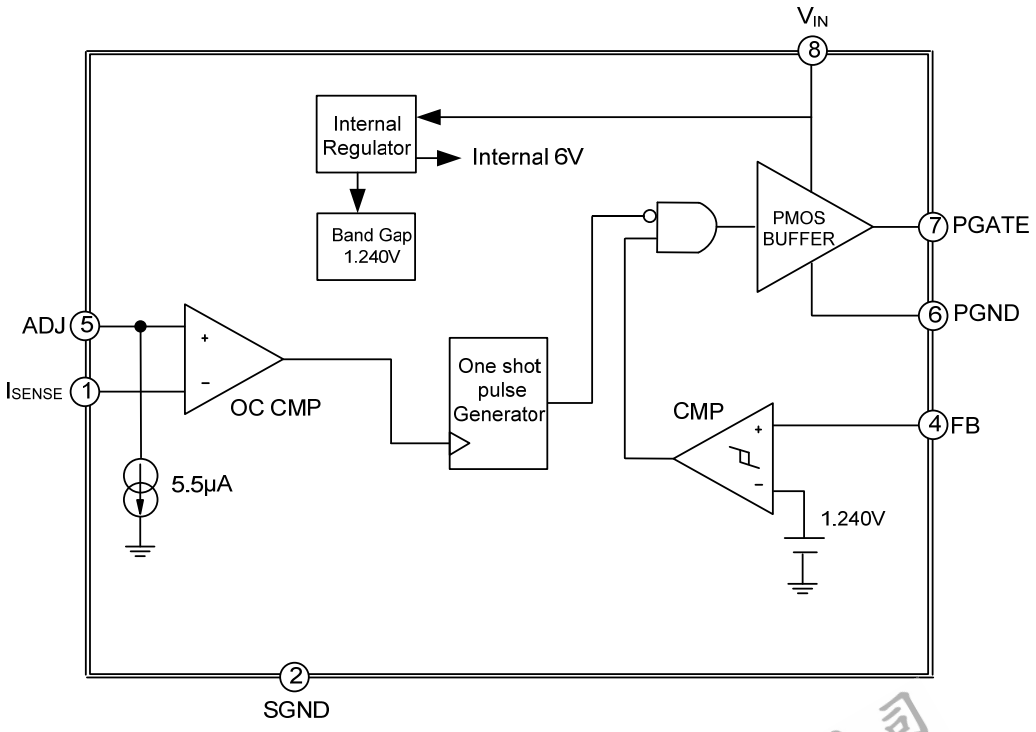
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO	PIN NAME	DESCRIPTION
1	I_{SENSE}	The over-current protection input pin that be connected to Drain node of the external P-Channel.
2	S_{GND}	Signal Ground.
3	NC	No Connection.
4	FB	The feedback voltage input.
5	ADJ	The over-current protection input pin that adjust current limit threshold.
6	P_{GND}	Power Ground.
7	GATE	Driver pin to Gate of the external P-Channel. PGATE swings between V_{IN} and V_{IN}-5V.
8	V_{IN}	Power Supply

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Input Voltage	V_{IN}	-0.3 ~ 36	V
P_{GATE} Voltage	V_{PGATE}	-0.3 ~ 36	V
FB Voltage	V_{FB}	-0.3 ~ 5	V
I_{SENSE} Voltage	V_{ISNS}	-1.0 ~ 36	V
ADJ Voltage	V_{ADJ}	-0.3 ~ 36	V
Power Dissipation (T_A =25℃)	P_D	400	mW
Junction Temperature	T_J	150	℃
Storage Temperature	T_{STG}	-65 ~ +150	℃

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ OPERATING RATINGS

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage		4.5 ~ 35	V
Operating Junction Temperature	T_{OPR}	-40 ~ +125	℃

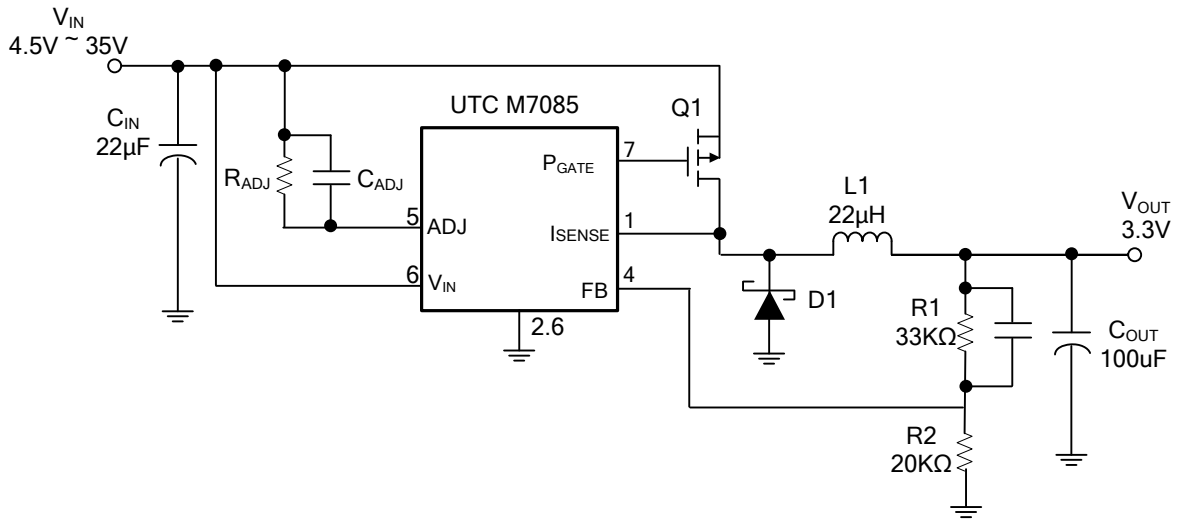
■ ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{ISNS} = V_{IN} − 1V, and V_{ADJ} = V_{IN} − 1.1V, Ta=25℃

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Feedback Voltage (Note 1)		V_{FB}		1.224	1.240	1.256	V
				1.215		1.265	
Minimum Driver Voltage		$V_{PGATE(MIN)}$	V_{IN} = 4.5V V_{FB} = 1.0V I_{GATE} = 100μA sink		1.15		V
Comparator Hysteresis		V_{HYS}			10	16	mV
					15	21	
Current Limit Comparator Trip Voltage		V_{CL} (Note2)	R_{ADJ} = 20Ω		110		mV
			R_{ADJ} = 160Ω		880		
Current Limit Comparator Offset		$V_{CL(OFF)}$	V_{FB} = 1.5V	-20	0	+20	mV
Current Limit ADJ Current Source		$I_{CL(ADJ)}$	V_{FB} = 1.5V	3.0	5	7.0	μA
FB pin Bias Current (Note 3)		I_{FB}	V_{FB} = 1.0V		320	756	nA
Driver Output Current	Source	I_{PGATE}	V_{IN} = 7V, P_{GATE} = 3.5V		0.4		A
	Sink		V_{IN} = 7V, P_{GATE} = 3.5V		0.3		
Driver Resistance	Source	R_{PGATE}	I_{SOURCE} = 100mA		5		Ω
	Sink		I_{SINK} = 100mA		8		
Current Limit One Shot off Time		T_{CL}	V_{ADJ} = 11.5V, V_{ISNS} = 11.0V, V_{FB} = 1.0V	5	8	13	μS
Minimum on Time in Normal Operation		$T_{OPR(MIN)}$	V_{ISNS} = V_{ADJ}+0.1V, C_{LOAD} on OUT = 1000pF, (Note 4)		110		ns
Minimum on Time in Current Limit		$T_{CL(MIN)}$	V_{ISNS} = V_{ADJ}+0.1V, V_{FB} = 1.0V C_{LOAD} on OUT=1000pF (Note 4)		185		ns
Feedback Voltage Line Regulation		$\%V_{FB}/\triangle V_{IN}$	4.5 ≤ V_{IN} ≤ 35V		0.010		%/V
Quiescent Current at Ground Pin		I_Q	FB = 1.5V (Not Switching)		300	500	μA

Note: 1. The V_{FB} is the trip voltage at the FB pin when PGATE switches from high to low.
2. V_{CL} = I_{CL_ADJ} * R_{ADJ}
3. Bias current flows out from the FB pin.
4. A 1000pF capacitor is connected between V_{IN} and P_{GATE}.

■ TYPICAL APPLICATION CIRCUIT



■ APPLICATION INFORMATION

Setting the output voltage

Select an output voltage between 1.24V and V_{IN} by connecting FB to a resistive voltage-divider between V_{OUT} and GND (see the Typical Operating Circuit). Choose R2 for a reasonable bias current in the resistive divider. A wide range of resistor values is acceptable.

R1, R2 is given by:

$$V_{OUT} = 1.240^* (R1 + R2) / R2$$

Setting over current protection threshold by the $R_{DS(ON)}$ of the P-Channel

The UTC **M7085** has a cycle-by-cycle current limit. Current limit is sensed across the V_{DS} of the P-Channel or across an additional sense resistor. When current limit is activated, the UTC **M7085** turns off the external P-Channel for a period of 9μs(typical). The current limit is adjusted by an external resistor, R_{ADJ}.

The current limit circuit is composed of the I_{SENSE} comparator and the one-shot pulse generator. The positive input of the I_{SENSE} comparator is the ADJ pin. An internal 5.5μA current sink creates a voltage across the external R_{ADJ} resistor. This voltage is compared to the voltage across the P-Channel or sense resistor. The ADJ voltage can be calculated as follows:

$$V_{ADJ} = V_{IN} - (R_{ADJ} * 3.0\mu A)$$

Where 3.0μA is the minimum $I_{CL(ADJ)}$ value.

The negative input of the I_{SENSE} comparator is the I_{SENSE} pin that should be connected to the drain of the external P-Channel. The inductor current is determined by sensing the V_{DS}. It can be calculated as follows.

$$V_{ISENSE} = V_{IN} - (R_{DS(ON)} * I_{IND\_PEAK}) = V_{IN} - V_{DS}$$

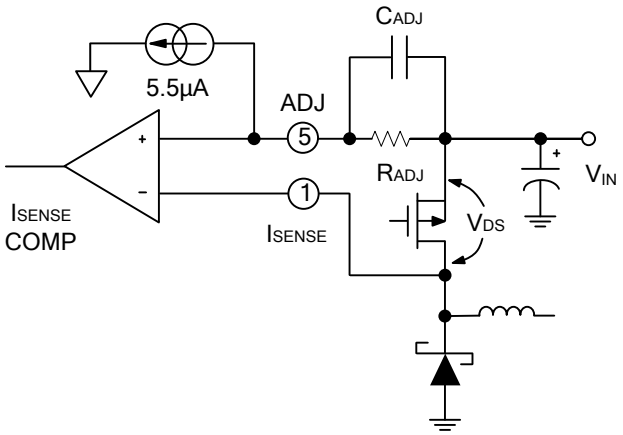


Fig. 1 Current Sensing by V_{DS}

The current limit is activated when the voltage at the ADJ pin exceeds the voltage at the I_{SENSE} pin. The I_{SENSE} comparator triggers the 9μs one shot pulse generator forcing the driver to turn the P-Channel off. The driver turns the P-Channel back on after 9μs. If the current has not reduced below the set threshold, the cycle will repeat continuously.

A filter capacitor, C_{ADJ}, should be placed as shown in Fig. 1 C_{ADJ} filters unwanted noise so that the I_{SENSE} comparator will not be accidentally triggered. A value of 100pF to 1nF is recommended in most applications. Higher values can be used to create a soft-start function. The current limit comparator has approximately 100ns of blanking time. This ensures that the P-Channel is fully on when the current is sensed. However, under extreme conditions such as cold temperature, some P-Channels may not fully turn on within the blanking time. In this case, the current limit threshold must be increased. If the current limit function is used, the on time must be greater than 100ns. Under low duty cycle operation, the maximum operating frequency will be limited by this minimum on time.

■ APPLICATION INFORMATION(Cont.)

Setting over current protection threshold by external sense resistor

The V_{DS} of a P-Channel will tend to vary significantly over temperature. This will result an equivalent variation in current limit. To improve current limit accuracy an external sense resistor can be connected from V_{IN} to the source of the P-Channel, as shown in Fig. 2.

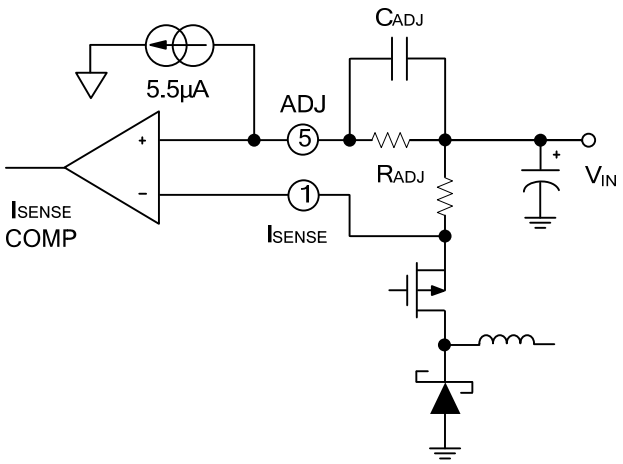


Fig. 2 Current Sensing by External Resistor

Setting start up time

The current limit circuit is active during start-up. During start-up the P-Channel will stay on until either the current limit or the feedback comparator is tripped If the current limit comparator is tripped first then the fold back characteristic should be taken into account. Start-up into full load may require a higher current limit set point or the load must be applied after start-up.

One problem with selecting a higher current limit is inrush current during start-up. Increasing the capacitance(C_{ADJ}) in parallel with R_{ADJ} results in soft-start. C_{ADJ} and R_{ADJ} create an RC time constant forcing current limit to activate at a lower current. The output voltage will ramp more slowly when using the soft-start functionality. There are example start-up plots for C_{ADJ} equal to 1nF and 10nF in the Typical Performance Characteristics. Lower values for C_{ADJ} will have little to no effect on soft-start.

Inductor selection (L1)

UTC **M7085** operates over a wide frequency range and can use a wide range of inductance values. The inductance value and the resulting ripple is one of the key parameters controlling operating frequency. The second is the ESR.

Output capacitor selection (C_{OUT})

The output capacitor, C_{OUT}, is required to keep the output voltage ripple small and to ensure regulation loop stability. C_{OUT} must have low impedance at the switching frequency. For most applications, a 200mF capacitor is sufficient.

Input capacitor selection (C_{IN})

The input capacitor, C_{IN}, reduces the current peaks drawn and reduces switching noise in the IC. a bypass capacitor is required between the input source and ground. It must be located near the source pin of the external P-Channel. The input capacitor prevents large voltage transients at the input and provides the instantaneous current when the P-Channel turns on. The capacitance value should be selected such that the ripple voltage created by the charge and discharge of the capacitance is less than 10% of the total ripple across the capacitor.

Catch diode selection (D1)

The important parameters for the catch diode are the peak current, the peak reverse voltage, and the average power dissipation. For high temperature applications, diode leakage current may become significant and require a higher reverse voltage rating to achieve acceptable performance.

■ APPLICATION INFORMATION(Cont.)

P-Channel MOSFET Selection(Q1)

An external P-Channel power MOSFET must be used the UTC **M7085** key selection criteria for the power for the P-Channel are the maximum Drain-Source voltage (V_{DS}) MOSFET are the gate threshold, V_{GS}, the “ON” resistance, $R_{DS(ON)}$ and its total gate charge.

The voltage across the PFET when it is turned off is equal to the sum of the input voltage and the diode forward voltage. The V_{DS} must be selected to provide some margin beyond the input voltage.

$R_{DS(ON)}$determines the conduction losses for each switching cycle, the lower the ON resistance, the higher the efficiency can be chivied.

A power MOSFET with lower gate charge can give lower switching losses but the fast transient can cause unwanted EMI to the system. Compromise in between is required during the design stage. Keeping the gate capacitance below 2000pF is recommended.