



# MJE13003-H

## NPN SILICON TRANSISTOR

### NPN SILICON POWER TRANSISTOR

■ DESCRIPTION

These devices are designed for high-voltage, high-speed power switching inductive circuits where fall time is critical. They are particularly suited for 115 and 220V applications in switch mode.

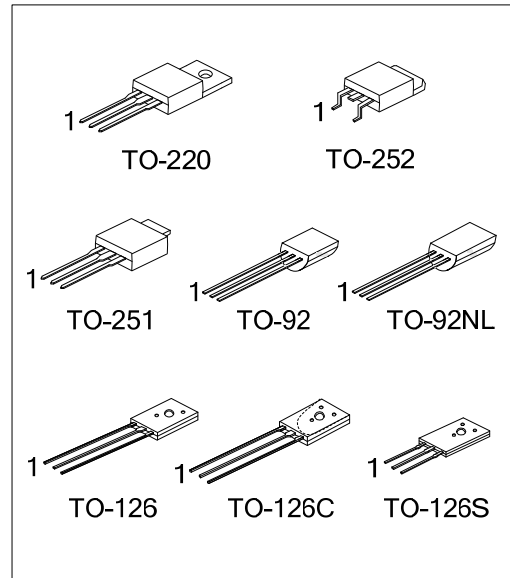
■ FEATURES

- \* Reverse biased SOA with inductive load @  $T_c=100^\circ\text{C}$
- \* Inductive switching matrix 0.5 ~ 1.5 Amp, 25 and  $100^\circ\text{C}$   
Typical  $t_c = 290\text{ns}$  @ 1A,  $100^\circ\text{C}$ .
- \* 900V blocking capability

■ APPLICATIONS

- \* Switching regulator's, inverters
- \* Motor controls
- \* Solenoid/relay drivers
- \* Deflection circuits

■ ORDERING INFORMATION



Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen-Free		1	2	3	
MJE13003L-H-x-T60-K	MJE13003G-H-x-T60-K	TO-126	B	C	E	Bulk
MJE13003L-H-x-T6C-A-K	MJE13003G-H-x-T6C-A-K	TO-126C	E	C	B	Bulk
MJE13003L-H-x-T6C-K	MJE13003G-H-x-T6C-K	TO-126C	B	C	E	Bulk
MJE13003L-H-x-T6S-K	MJE13003G-H-x-T6S-K	TO-126S	B	C	E	Bulk
MJE13003L-H-x-T92-B	MJE13003G-H-x-T92-B	TO-92	E	C	B	Tape Box
MJE13003L-H-x-T92-K	MJE13003G-H-x-T92-K	TO-92	E	C	B	Bulk
MJE13003L-H-x-T92-R	MJE13003G-H-x-T92-R	TO-92	E	C	B	Tape Reel
MJE13003L-H-x-T9N-B	MJE13003G-H-x-T9N-B	TO-92NL	E	C	B	Tape Box
MJE13003L-H-x-T9N-K	MJE13003G-H-x-T9N-K	TO-92NL	E	C	B	Bulk
MJE13003L-H-x-T9N-R	MJE13003G-H-x-T9N-R	TO-92NL	E	C	B	Tape Reel
MJE13003L-H-x-TA3-T	MJE13003G-H-x-TA3-T	TO-220	B	C	E	Tube
MJE13003L-H-x-TM3-T	MJE13003G-H-x-TM3-T	TO-251	B	C	E	Tube
MJE13003L-H-x-TN3-R	MJE13003G-H-x-TN3-R	TO-252	B	C	E	Tape Reel
MJE13003L-H-x-TN3-T	MJE13003G-H-x-TN3-T	TO-252	B	C	E	Tube

<p>MJE13003L-H-x-T6C-A-K</p>	<p>(1)Packing Type (2)Pin Assignment (3)Package Type (4)Rank (5)Lead Free</p>	<p>(1) B: Tape Box, K: Bulk, R: Tape Reel, T: Tube (2) refer to Pin Assignment (for TO-126C) (3) T60: TO-126, T6C: TO-126C, T6S: TO-126S T92: TO-92, T9N: TO-92NL, TA3: TO-220 TM3: TO-251, TN3: TO-252 (4) x: refer to Classification of <math>h_{FE1}</math> (5) L: Lead Free, G: Halogen Free</p>
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■ ABSOLUTE MAXIMUM RATINGS

PARAMETER		SYMBOL	RATINGS	UNIT	
Collector-Emitter Voltage		$V_{CEO(SUS)}$	400	V	
Collector-Base Voltage		$V_{CBO}$	900	V	
Emitter Base Voltage		$V_{EBO}$	9	V	
Collector Current	Continuous	$I_C$	1.5	A	
	Peak (1)	$I_{CM}$	3		
Base Current	Continuous	$I_B$	0.75	A	
	Peak (1)	$I_{BM}$	1.5		
Emitter Current	Continuous	$I_E$	2.25	A	
	Peak (1)	$I_{EM}$	4.5		
Power Dissipation	$T_A=25^\circ\text{C}$	TO-126 / TO-126C TO-126S	$P_D$	1.4	W
		TO-92 / TO-92NL		1.1	W
		TO-220		2	W
		TO-251 / TO-252		1.56	W
	$T_C=25^\circ\text{C}$	TO-126 / TO-126C TO-126S		20	W
		TO-92 / TO-92NL		1.5	W
		TO-220		40	W
		TO-251 / TO-252		25	W
Junction Temperature		$T_J$	+150	$^\circ\text{C}$	
Storage Temperature		$T_{STG}$	-55 ~ +150	$^\circ\text{C}$	

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.  
 Absolute maximum ratings are stress ratings only and functional device operation is not implied.

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## NPN SILICON TRANSISTOR

■ ELECTRICAL CHARACTERISTICS (T<sub>C</sub>=25°C, unless otherwise specified.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>OFF CHARACTERISTICS (Note)</b>						
Collector-Emitter Sustaining Voltage	V <sub>CEO(SUS)</sub>	I <sub>C</sub> =10mA, I <sub>B</sub> =0	400			V
Collector Cutoff Current	I <sub>CEO</sub>	V <sub>CEO</sub> =Rated Value, V <sub>BE(OFF)</sub> =1.5 V			1	mA
			T <sub>C</sub> =25°C			
Emitter Cutoff Current	I <sub>EBO</sub>	V <sub>EB</sub> =9V, I <sub>C</sub> =0			1	mA
<b>SECOND BREAKDOWN</b>						
Second Breakdown Collector Current with bass forward biased	I <sub>s/b</sub>			See Fig.5		
Clamped Inductive SOA with base reverse biased	RB <sub>SOA</sub>			See Fig.6		
<b>ON CHARACTERISTICS (Note)</b>						
DC Current Gain	h <sub>FE1</sub>	I <sub>C</sub> =0.3A, V <sub>CE</sub> =5V	14		57	
	h <sub>FE2</sub>	I <sub>C</sub> =1A, V <sub>CE</sub> =5V	5		30	
Collector-Emitter Saturation Voltage	V <sub>CE(SAT)</sub>	I <sub>C</sub> =0.5A, I <sub>B</sub> =0.1A			0.5	V
		I <sub>C</sub> =1A, I <sub>B</sub> =0.25A			1	
		I <sub>C</sub> =1.5A, I <sub>B</sub> =0.5A			3	
		I <sub>C</sub> =1A, I <sub>B</sub> =0.25A, T <sub>C</sub> =100°C			1	
Base-Emitter Saturation Voltage	V <sub>BE(SAT)</sub>	I <sub>C</sub> =0.5A, I <sub>B</sub> =0.1A			1	V
		I <sub>C</sub> =1A, I <sub>B</sub> =0.25A			1.2	
		I <sub>C</sub> =1A, I <sub>B</sub> =0.25A, T <sub>C</sub> =100°C			1.1	
<b>DYNAMIC CHARACTERISTICS</b>						
Current-Gain-Bandwidth Product	f <sub>T</sub>	I <sub>C</sub> =100mA, V <sub>CE</sub> =10V, f=1MHz	4	10		MHz
Output Capacitance	C <sub>OB</sub>	V <sub>CB</sub> =10V, I <sub>E</sub> =0, f=0.1MHz		21		pF
<b>SWITCHING CHARACTERISTICS</b>						
<b>Resistive Load (Table 1)</b>						
Delay Time	t <sub>D</sub>	V <sub>CC</sub> =125V, I <sub>C</sub> =1A, I <sub>B1</sub> =I <sub>B2</sub> =0.2A, t <sub>p</sub> =25μs, Duty Cycle≤1%		0.05	0.1	μs
Rise Time	t <sub>R</sub>			0.5	1	μs
Storage Time	t <sub>S</sub>			2	4	μs
Fall Time	t <sub>F</sub>			0.4	0.7	μs
<b>Inductive Load, Clamped (Table 1)</b>						
Storage Time	t <sub>STG</sub>	I <sub>C</sub> =1A, V <sub>CLAMP</sub> =300V, I <sub>B1</sub> =0.2A, V <sub>BE(OFF)</sub> =5V <sub>DC</sub> , T <sub>C</sub> =100°C		1.7	4	μs
Crossover Time	t <sub>C</sub>			0.29	0.75	μs
Fall Time	t <sub>F</sub>			0.15		μs

Note: Pulse Test: PW=300μs, Duty Cycle≤2%

■ CLASSIFICATION OF h<sub>FE1</sub>

RANK	A	B	C	D	E	F	G	H
RANGE	14 ~ 22	21 ~ 27	26 ~ 32	31 ~ 37	36 ~ 42	41 ~ 47	46 ~ 52	51 ~ 57

## APPLICATION INFORMATION

Table 1. Test Conditions for Dynamic Performance

Reverse Bias Safe Operating Area and Inductive Switching		Resistive Switching
Test Circuits	<p>Note: P<sub>w</sub> and V<sub>cc</sub> Adjusted for Desired I<sub>c</sub> R<sub>b</sub> Adjusted for Desired I<sub>bt</sub></p>	
Circuit Values	<p>Coil Data : V<sub>CC</sub>=20V Ferroxcube core #6656 V<sub>CLAMP</sub>=300V Full Bobbin ( ~ 200 Turns) #20</p> <p>GAP for 30 mH/2 A L<sub>COIL</sub>=50mH</p>	<p>V<sub>CC</sub>=125V R<sub>C</sub>=125Ω D1=1N5820 or Equiv. R<sub>C</sub>=47Ω</p>
Test Waveforms	<p>Output Waveforms</p> <p>Test Equipment Scope-Tektronics 475 or Equivalent</p>	<p>tr, tf &lt; 10ns Duty Cycle = 1.0% R<sub>b</sub> and R<sub>c</sub> adjusted for desired I<sub>b</sub> and I<sub>c</sub></p>

Table 2. Typical Inductive Switching Performance

I <sub>c</sub> (A)	T <sub>c</sub> (°C)	t <sub>sv</sub> (μs)	t <sub>rv</sub> (μs)	t <sub>fi</sub> (μs)	t <sub>ti</sub> (μs)	t <sub>c</sub> (μs)
0.5	25	1.3	0.23	0.30	0.35	0.30
	100	1.6	0.26	0.30	0.40	0.36
1	25	1.5	0.10	0.14	0.05	0.16
	100	1.7	0.13	0.26	0.06	0.29
1.5	25	1.8	0.07	0.10	0.05	0.16
	100	3	0.08	0.22	0.08	0.28

Note: All Data Recorded in the Inductive Switching Circuit in Table 1

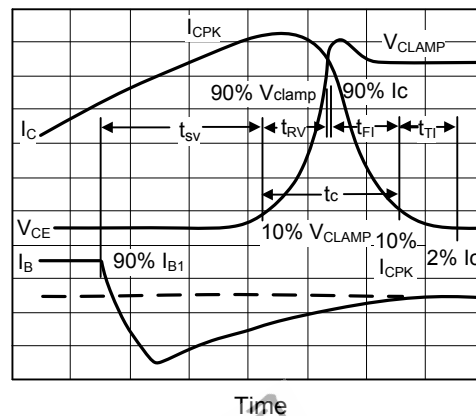


Fig.1 Inductive Switching Measurements

## SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads, which are common to switch mode power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

$t_{SV}$  = Voltage Storage Time, 90%  $I_{B1}$  to 10%  $V_{CLAMP}$

$t_{RV}$  = Voltage Rise Time, 10 ~ 90%  $V_{CLAMP}$

$t_{FI}$  = Current Fall Time, 90 ~ 10%  $I_C$

$t_{TI}$  = Current Tail, 10 ~ 2%  $I_C$

$t_C$  = Crossover Time, 10%  $V_{CLAMP}$  to 10%  $I_C$

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation:

$$P_{SWT} = 1/2 V_{CC} I_C (t_C) f$$

In general,  $t_{RV} + t_{FI} \approx t_C$ . However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this transistor are the inductive switching speeds ( $t_C$  and  $t_{SV}$ ) which are guaranteed at 100°C.

## RESISTIVE SWITCHING PERFORMANCE

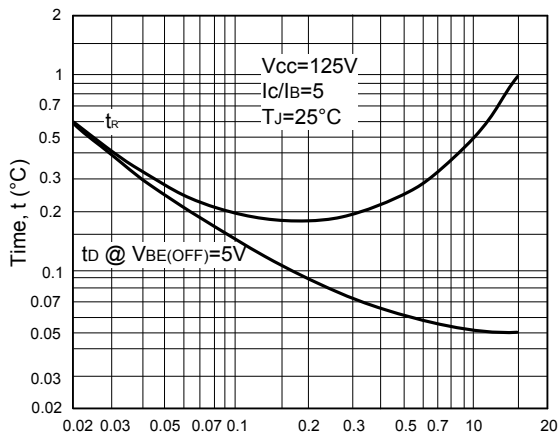


Fig.2 Turn-On Time

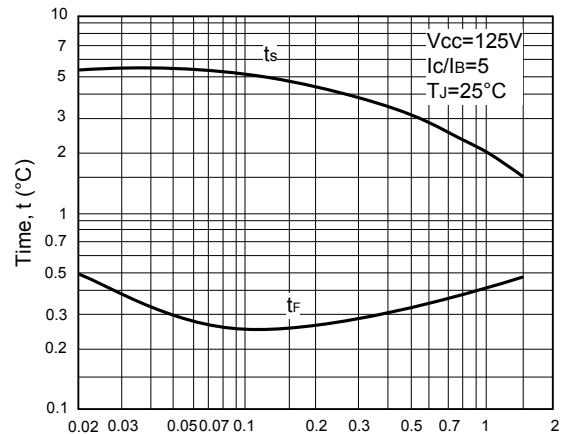


Fig.3 Turn-Off Time

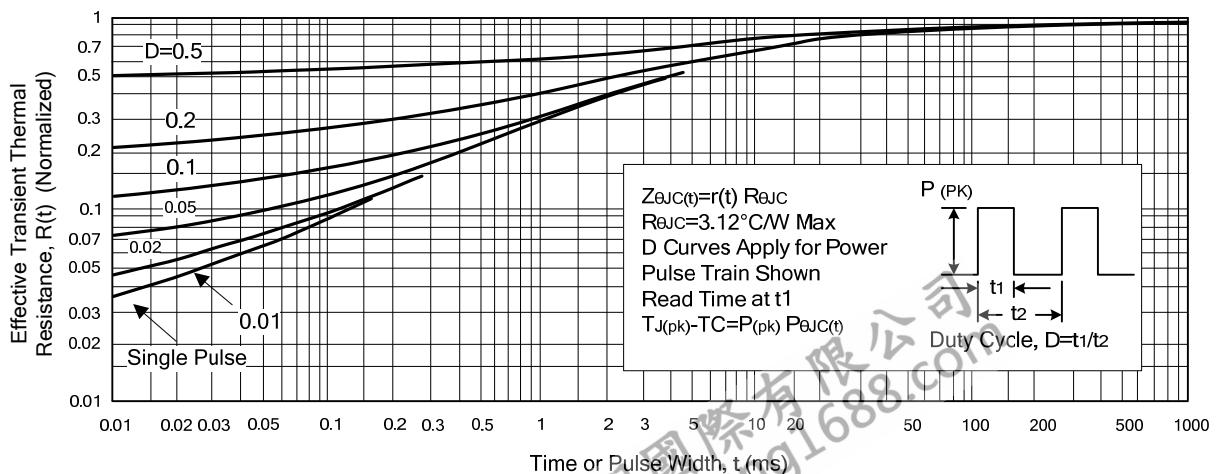


Fig.4 Thermal Response

## SAFE OPERATING AREA INFORMATION

### FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C$ - $V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Fig.5 is based on  $T_C = 25^\circ\text{C}$ ;  $T_{J(PK)}$  is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when  $T_C \geq 25^\circ\text{C}$ . Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Fig.5.

$T_{J(PK)}$  may be calculated from the data in Fig.4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

### REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as  $RB_{SOA}$  (Reverse Bias Safe Operating Area) and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Fig.6 gives  $RB_{SOA}$  characteristics.

The Safe Operating Area of Fig.5 and 6 are specified ratings (for these devices under the test conditions shown.)

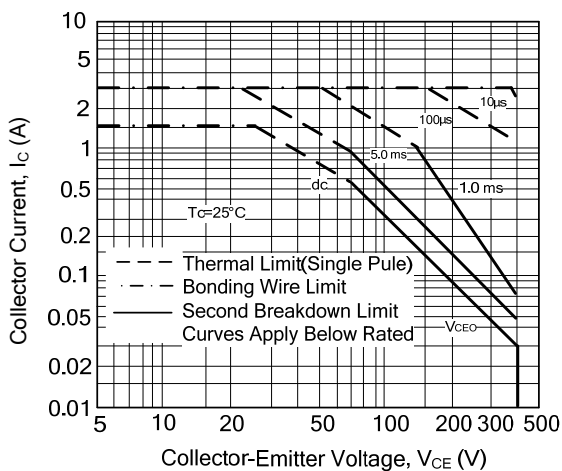


Fig.5 Active Region Safe Operating Area

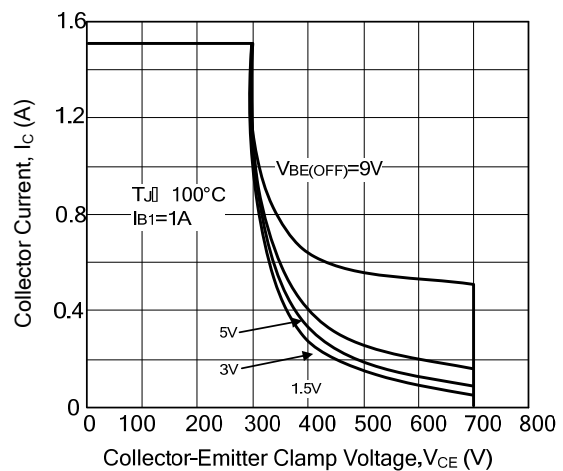
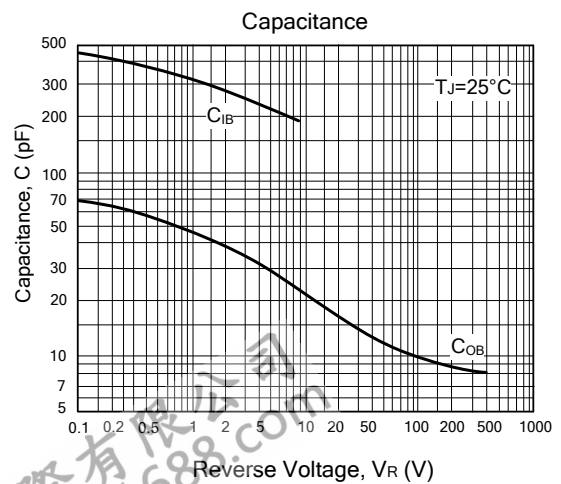
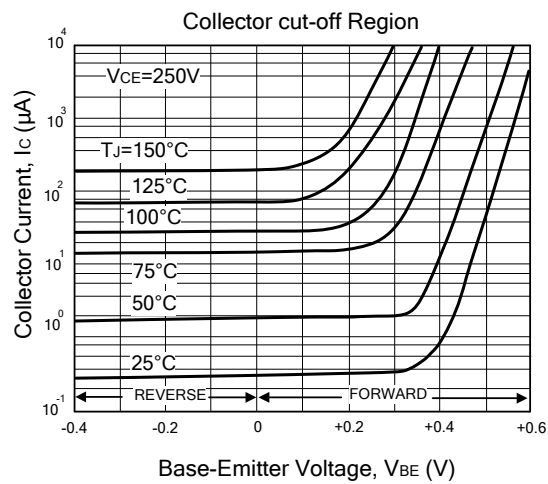
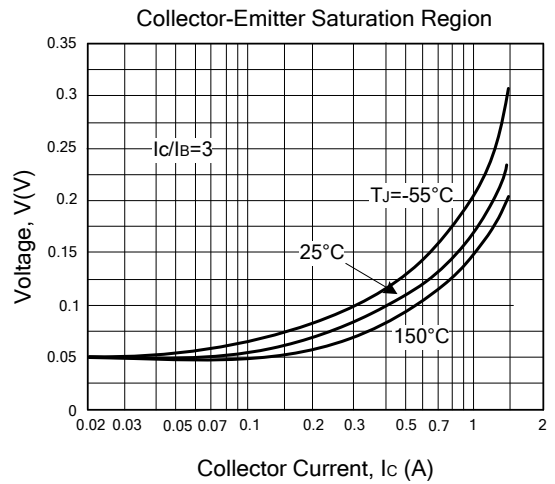
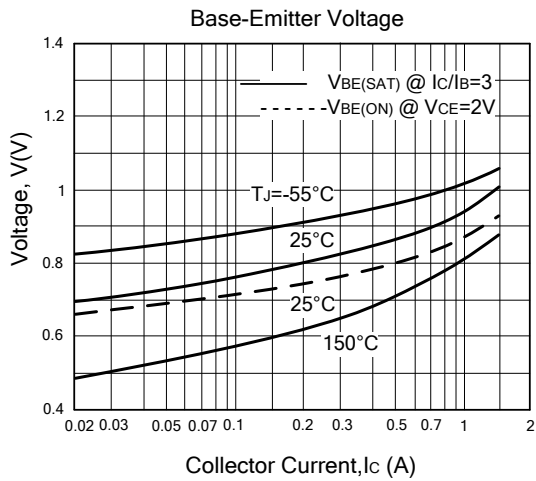
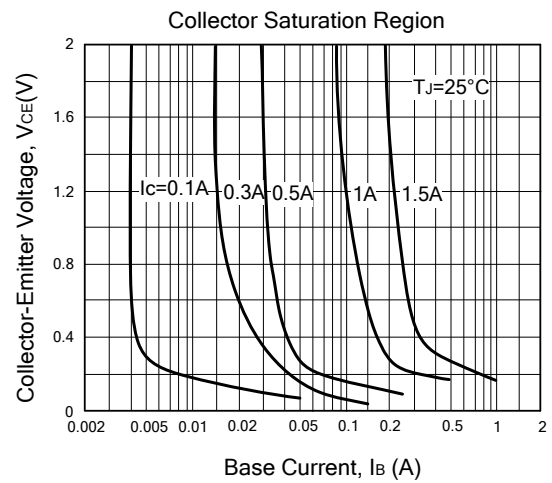
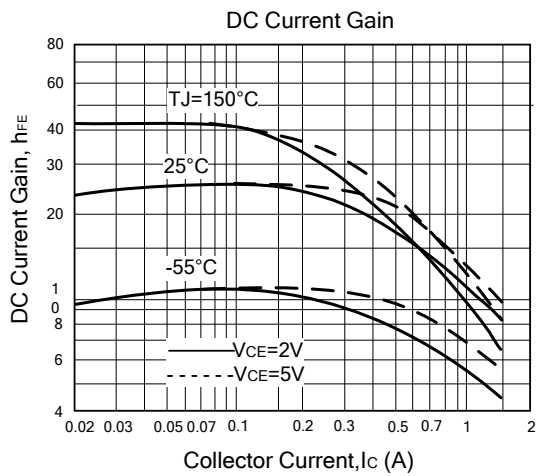
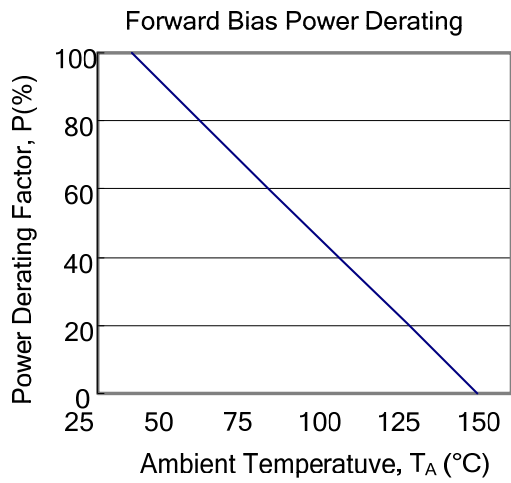


Fig.6 Reverse Bias Safe Operating Area

### TYPICAL CHARACTERISTICS



### ■ TYPICAL CHARACTERISTICS(Cont.)



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