# MJE13005-H

**_NPN SILICON TRANSISTOR_**

## NPN SILICON POWER TRANSISTORS

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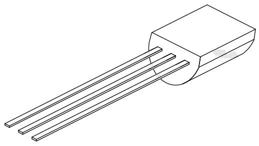


TO-92

## ■ DESCRIPTION

These devices are designed for high-voltage, high-speed power switching inductive circuits where fall time is critical. They are particularly suited for 115 and 220 V SWITCHMODE.

## ■ FEATURES

* $V_{CEO(SUS)}$= 400 V
* Reverse bias SOA with inductive loads @ $T_C$ = 100°C
* Inductive switching matrix 2 to 4 Amp, 25 and 100°C
  $t_C$ @ 3A, 100°C is 180 ns (Typ)
* 700V blocking capability
* SOA and switching applications information

## ■ APPLICATIONS

* Switching regulator's, inverters
* Motor controls
* Solenoid/Relay drivers
* Deflection circuits

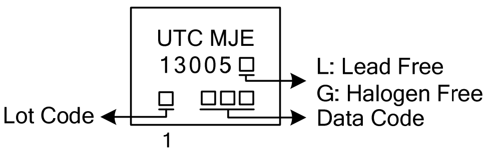
## ■ ORDERING INFORMATION

| Ordering Number | | Package | Pin Assignment | | | Packing |
|---|---|---|---|---|---|---|
| Lead Free | Halogen-Free | | 1 | 2 | 3 | |
| MJE13005L-H-x-T92-B | MJE13005G-H-x-T92-B | TO-92 | B | C | E | Tape Box |
| MJE13005-L-H-x-T92-K | MJE13005G-H-x-T92-K | TO-92 | B | C | E | Bulk |

Note: Pin assignment: E: Emitter B: Base C: Collector

| MJE13005L-H-x-T92-K | |
|---|---|
| (1)Packing Type | (1) B: Tape Box, K: Bulk |
| (2)Package Type | (2) T92: TO-92 |
| (3)Rank | (3) x: refer to Classification of $h_{FE1}$ |
| (4)Green Package | (4) L: Lead Free, G: Halogen Free and Lead Free |

## ■ MARKING



## ■ ABSOLUTE MAXIMUM RATINGS

| PARAMETER | | SYMBOL | RATINGS | UNIT |
|---|---|---|---|---|
| Collector-Emitter Voltage | | $V_{CEO(SUS)}$ | 400 | V |
| Collector-Emitter Voltage ($V_{BE}$=0) | | $V_{CES}$ | 900 | V |
| Collector-Base Voltage | | $V_{CBO}$ | 900 | V |
| Emitter Base Voltage | | $V_{EBO}$ | 9 | V |
| Collector Current | Continuous | $I_C$ | 4 | A |
| | Peak (1) | $I_{CM}$ | 8 | A |
| Base Current | Continuous | $I_B$ | 2 | A |
| | Peak (1) | $I_{BM}$ | 4 | A |
| Emitter Current | Continuous | $I_E$ | 6 | A |
| | Peak (1) | $I_{EM}$ | 12 | A |
| Power Dissipation at $T_A$=25°C | | $P_D$ | 0.8 | W |
| Derate above 25°C | | | 6.4 | mW/°C |
| Operating and Storage Junction Temperature | | $T_J$ , $T_{STG}$ | -65 ~ +150 | °C |

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.
Absolute maximum ratings are stress ratings only and functional device operation is not implied.

## ■ THERMAL DATA

| PARAMETER | SYMBOL | RATINGS | UNIT |
|---|---|---|---|
| Junction to Ambient | $\theta_{JA}$ | 150 | °C/W |
| Junction to Case | $\theta_{JC}$ | 45 | °C/W |

## ■ ELECTRICAL CHARACTERISTICS ($T_C$=25°C, unless otherwise specified)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** (Note 1) | | | | | | |
| Collector-Emitter Sustaining Voltage | $V_{CEO(SUS)}$ | $I_C$=10mA , $I_B$=0 | 400 | | | V |
| Collector Cutoff Current | $I_{CBO}$ | $V_{CBO}$=Rated Value, $V_{BE(OFF)}$=1.5V | | | 1 | mA |
| | | $V_{CBO}$=Rated Value, $V_{BE(OFF)}$=1.5V, $T_C$=100°C | | | 5 | mA |
| Emitter Cutoff Current | $I_{EBO}$ | $V_{EB}$=9V, $I_C$=0 | | | 1 | mA |
| **SECOND BREAKDOWN** | | | | | | |
| Second Breakdown Collector Current with bass forward biased | $I_{S/B}$ | | | See Fig. 11 | | |
| Clamped Inductive SOA with Base Reverse Biased | RBSOA | | | See Fig. 12 | | |
| **ON CHARACTERISTICS** (Note 1) | | | | | | |
| DC Current Gain | $h_{FE1}$ | $I_C$=0.5A, $V_{CE}$=5V | 15 | | 50 | |
| | $h_{FE2}$ | $I_C$=1A, $V_{CE}$=5V | 10 | | 60 | |
| | $h_{FE3}$ | $I_C$=2A, $V_{CE}$=5V | 8 | | 40 | |
| Collector-Emitter Saturation Voltage | $V_{CE(SAT)}$ | $I_C$=1A, $I_B$=0.2A | | | 0.5 | V |
| | | $I_C$=2A, $I_B$=0.5A | | | 0.6 | V |
| | | $I_C$=4A, $I_B$=1A | | | 1 | V |
| | | $I_C$=2A, $I_B$=0.5A, Ta=100°C | | | 1 | V |
| Base-Emitter Saturation Voltage | $V_{BE\ (SAT)}$ | $I_C$=1A, $I_B$=0.2A | | | 1.2 | V |
| | | $I_C$=2A, $I_B$=0.5A | | | 1.6 | V |
| | | $I_C$=2A, $I_B$=0.5A, $T_C$=100°C | | | 1.5 | V |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Current-Gain-Bandwidth Product | $f_T$ | $I_C$=500mA, $V_{CE}$=10V, f=1MHz | 4 | | | MHz |
| Output Capacitance | $C_{OB}$ | $V_{CB}$=10V, $I_E$=0, f=0.1MHz | | 65 | | pF |
| **SWITCHING CHARACTERISTICS** | | | | | | |
| Resistive Load (Table 1) | | | | | | |
| Delay Time | $t_D$ | $V_{CC}$=125V, $I_C$=2A, $I_{B1}$=$I_{B2}$=0.4A, $t_P$=25μs, Duty Cycle≤1% | | 0.025 | 0.1 | μs |
| Rise Time | $t_R$ | | | 0.3 | 0.7 | μs |
| Storage Time | $t_S$ | | | 1.7 | 4 | μs |
| Fall Time | $t_F$ | | | 0.4 | 0.9 | μs |

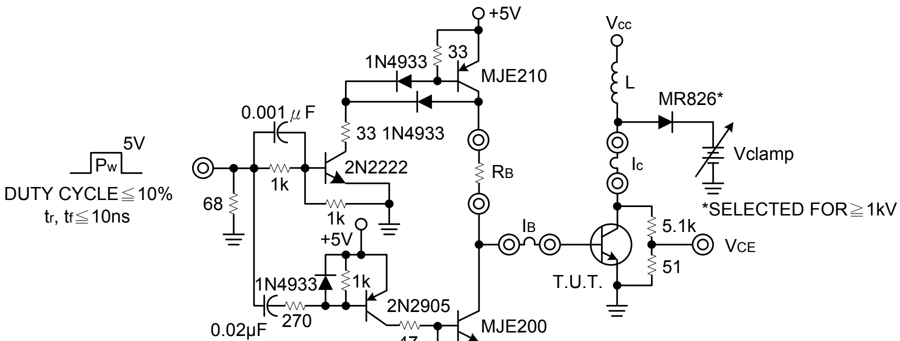
Note: 1. Pulse Test: Pulse Width=5ms, Duty Cycle≤10%
2. Pulse Test: $P_W$=300μs, Duty Cycle≤2%

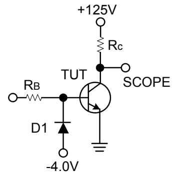
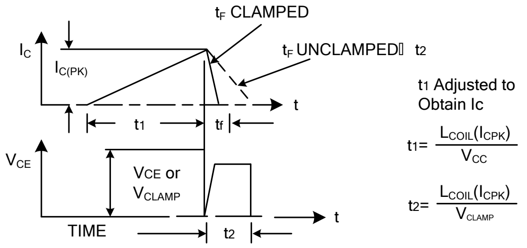
## ■ CLASSIFICATION OF $h_{FE1}$

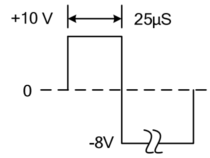
| RANK | A | B | C | D | E |
|---|---|---|---|---|---|
| RANGE | 15 ~ 20 | 20 ~ 25 | 25 ~ 30 | 30 ~ 40 | 40 ~ 50 |

## ■ APPLICATION INFORMATION

Table 1.Test Conditions for Dynamic Performance

<table>
<tr><td></td><td>Reverse Bias Safe Operating Area and Inductive Switching</td><td>Resistive Switching</td></tr>
<tr><td>Test Circuits</td><td>

<br>Note:<br>Pw and Vcc Adjusted for Desired Ic<br>RB Adjusted for Desired IB1</td><td>
</td></tr>
<tr><td>Circuit Values</td><td>Coil Data :<br>$V_{CC}$=20V<br>FERROXCUBE core #6656<br>Full Bobbin ( ~ 16 Turns) #16<br>GAP for 200μH/20 A<br>$L_{COIL}$=200μH<br>$V_{CLAMP}$=300V</td><td>$V_{CC}$=125V<br>$R_C$=62Ω<br>D1=1n5820 or Equiv.<br>RB=22Ω</td></tr>
<tr><td>Test Waveforms</td><td>OUTPUT WAVEFORMS<br>

<br>Test Equipment<br>Scope-Tektronics<br>475 or Equivalent</td><td>

<br>$t_R$, $t_F$<10ns<br>Duty Cycly=1.0%<br>$R_B$ and $R_C$ adjusted for desired $I_B$ and $I_C$</td></tr>
</table>

## ■ RESISTIVE SWITCHING PERFORMANCE

Fig. 1 Turn-On Time

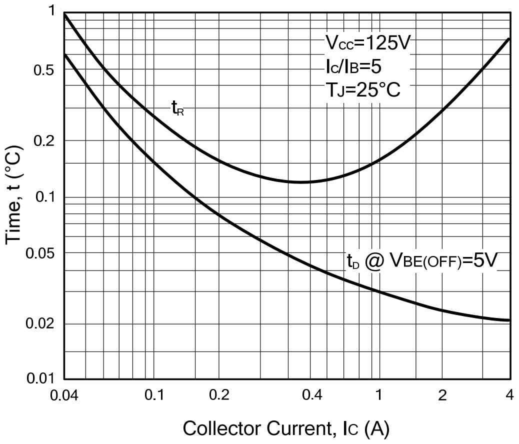



Fig. 2 Turn-Off Time

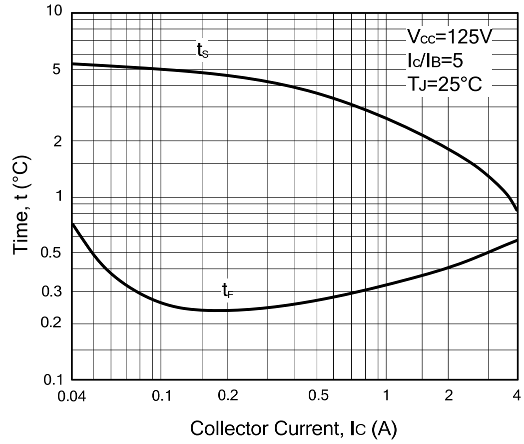



Fig. 3 Typical Thermal Response [ ZθJC(t)]

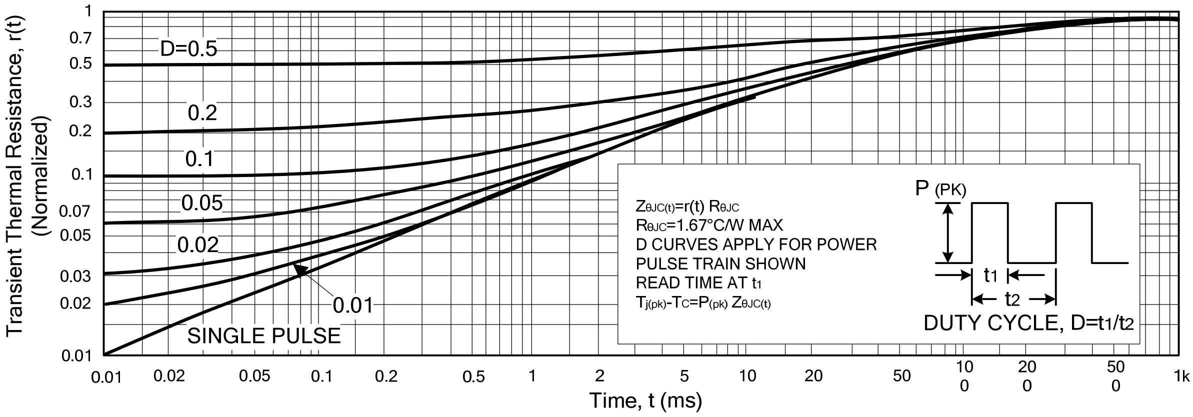
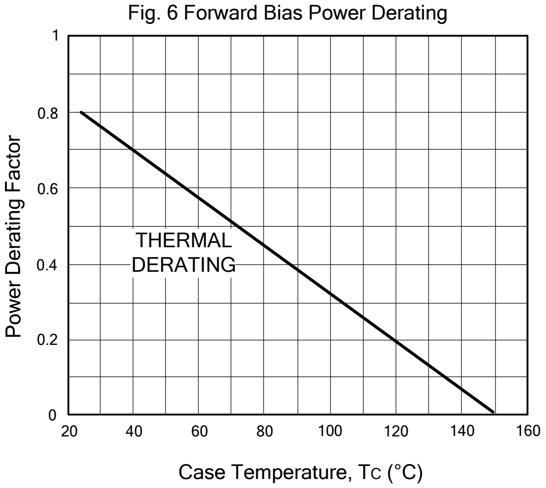



Fig. 6 Forward Bias Power Derating



## SAFE OPERATING AREA INFORMATION

**FORWARD BIAS**

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C$-$V_{CE}$ limits of the transistor that must be observed for reliable operation; e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Fig. 4 is based on $T_C$ = 25°C; $T_{J(PK)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C$≥25°C. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Fig. 4 may be found at any case temperature by using the appropriate curve on Fig. 6.

$T_{J(PK)}$ may be calculated from the data in Fig. 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

**REVERSE BIAS**

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 5 gives the complete RBSOA characteristics.

## ■ TYPICAL CHARACTERISTICS

Figure 7. DC Current Gain

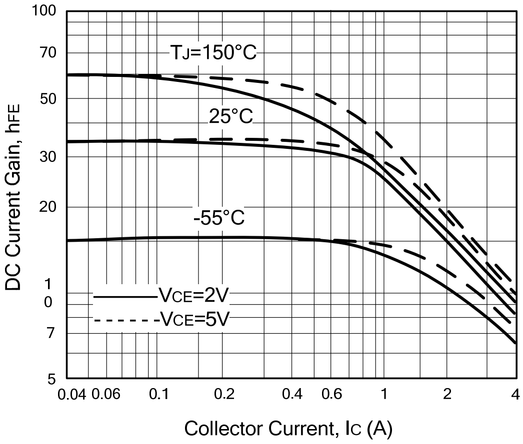



Figure 8. Collector Saturation Region

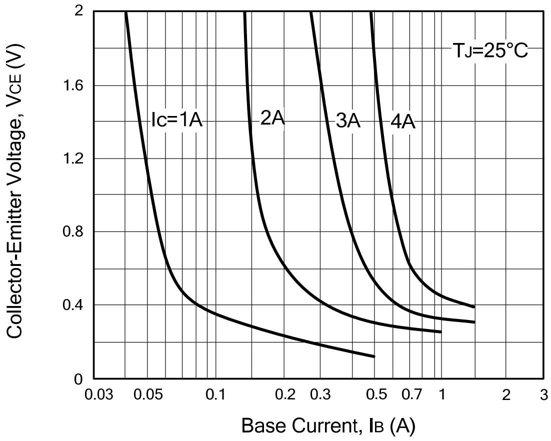



Figure 9. Base-Emitter Voltage

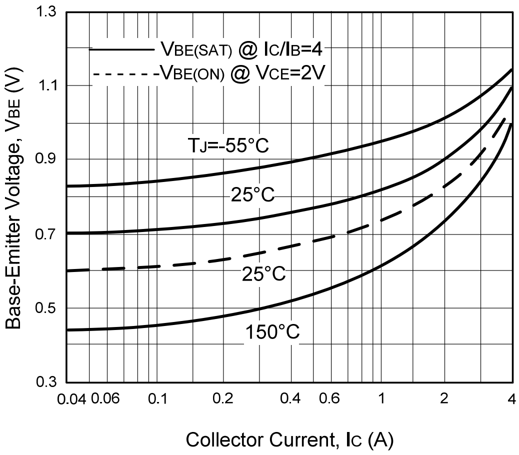



Figure 10. Collector-Emitter Saturation Voltage

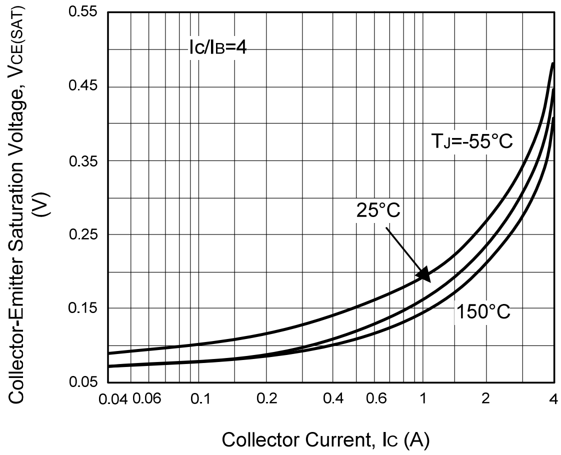



Figure 11. Collector Cutoff Region

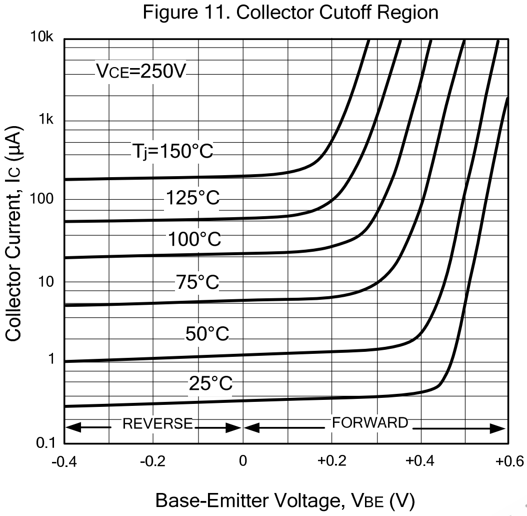



Figure 12. Capacitance