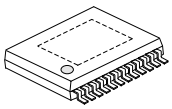
PA3212 CMOS IC

2.6W STEREO AUDIO AMPLIFIER WITH FOUR SELECTABLE GAIN SETTINGS AND MUX CONTROL



HTSSOP-24

■ DESCRIPTION

As operating on a single 5V supply, the UTC **PA3212** is capable of delivering 2.6W of output power per channel into 3Ω loads. In Bridge-Tied Load (BTL) mode the UTC **PA3212** has less than 1% THD+N, and it also has less than 0.65% THD+N across its specified frequency range when driving 1 W into 8-Ω speakers.

Way of two terminals (GAIN0 and GAIN1) can configure and control the amplifier gain. It also provides BTL gain settings of 2, 6, 12 and 24 V/V.

Other features included that the SHDN mode is provided to disable UTC **PA3212** for the low current consumption applications and the current consumption can be reduced to typically 150μA.

■ FEATURES

* Output power at 0.65% THD+N, V_{DD}=5V(TYP)
  −2.6W/CH (typical) into a 3Ω load
  −1.0W/CH (typical) into a 8Ω load
* Bridge-tied load (BTL) supported
* Gain control internally
* Differential Input fully
* Depop circuitry Inside
* Shutdown protection
* Stereo input

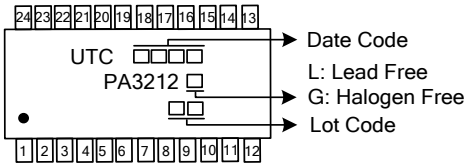
■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
PA3212L-N24-R	PA3212G-N24-R	HTSSOP-24	Tape Reel

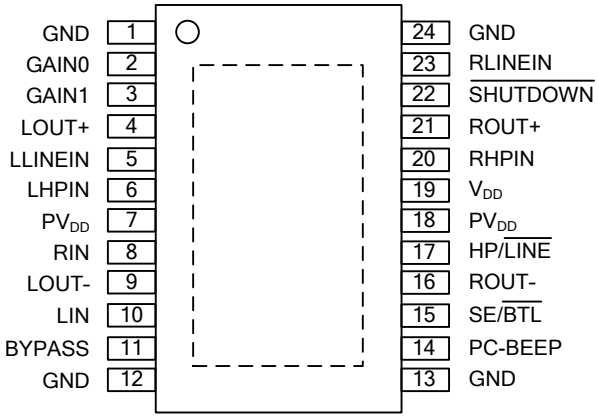
PA3212G-N24-R
(1)Packing Type
(2)Packing Type
(3)Green Package

(1) R: Tape Reel
(2) N24: HTSSOP-24
(3) G: Halogen Free and Lead Free, Lead Free

■ MARKING



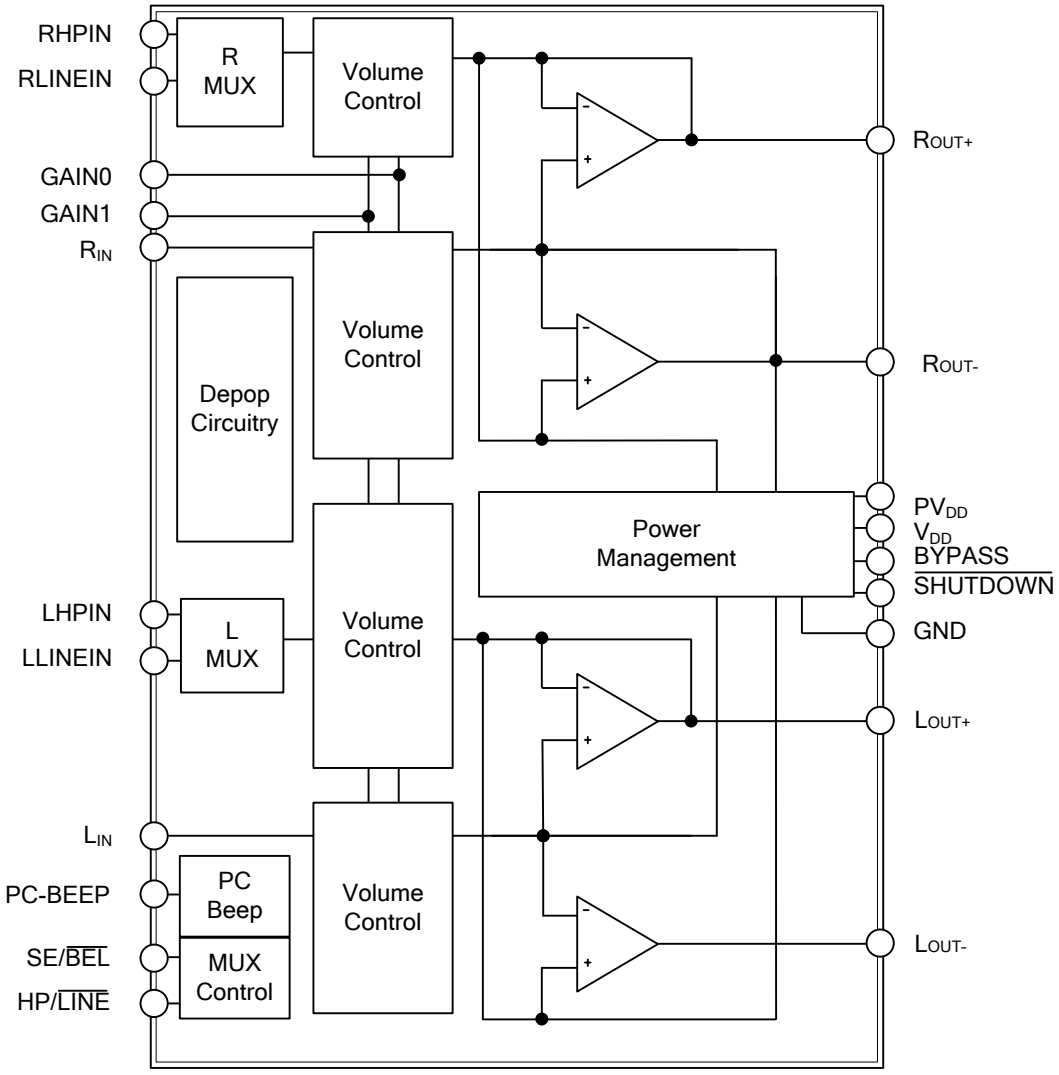
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	I/O	DESCRIPTION
1,12,13,24	GND		Ground.
11	BYPASS		Connected to voltage divider
2	GAIN0	I	For gain control: Bit 0
3	GAIN1	I	For gain control: Bit 1
5	LLINEIN	I	Line input for Left channel, available when pin15 is held low.
6	LHPIN	I	Headphone input Left channel, available when pin15 is held high.
7,18	PV_{DD}	I	Power supply voltage.
8	RIN	I	Differential input for right channel. And for single-ended inputs is also AC ground.
10	LIN	I	Differential input for Left channel. And for single-ended inputs is also AC ground.
14	PC-BEEP	I	PC-BEEP mode input. When at least eight continuous >1-V_{PP} square waves is input to this pin, PC-BEEP is enabled.
17	HP/$\overline{\text{LINE}}$	I	Input of MUX control. Being high to select the inputs of Pin6, 20, and low to select inputs of PIN 5, 23.
15	SE/$\overline{\text{BTL}}$	I	Low for BTL mode, high for SE mode.
19	V_{DD}	I	Analog V_{DD} supply voltage
20	RHPIN	I	Right channel headphone input, selected when pin17 is held high.
23	RLINEIN	I	Headphone input right channel, available when pin17 is held low.
22	$\overline{\text{SHUTDOWN}}$	I	In shutdown mode when held low, expect PC-BEEP remains active.
4	L_{OUT+}	O	In BTL mode: left channel + output; In SE mode: left channel + output
9	L_{OUT-}	O	In BTL mode: left channel - output; In SE mode: high impedance
16	R_{OUT-}	O	In BTL mode: right channel - output; In SE mode: right channel + output
21	R_{OUT+}	O	In BTL mode: right channel - output; In SE mode: high impedance

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}	6	V
Input Voltage	V_{IN}	-0.3 ~ V_{DD} ~ +0.3	V
Junction Temperature	T_J	+150	°C
Operating Temperature	T_{OPR}	-40 ~ +85	°C
Storage Temperature	T_{STG}	-55 ~ +150	°C

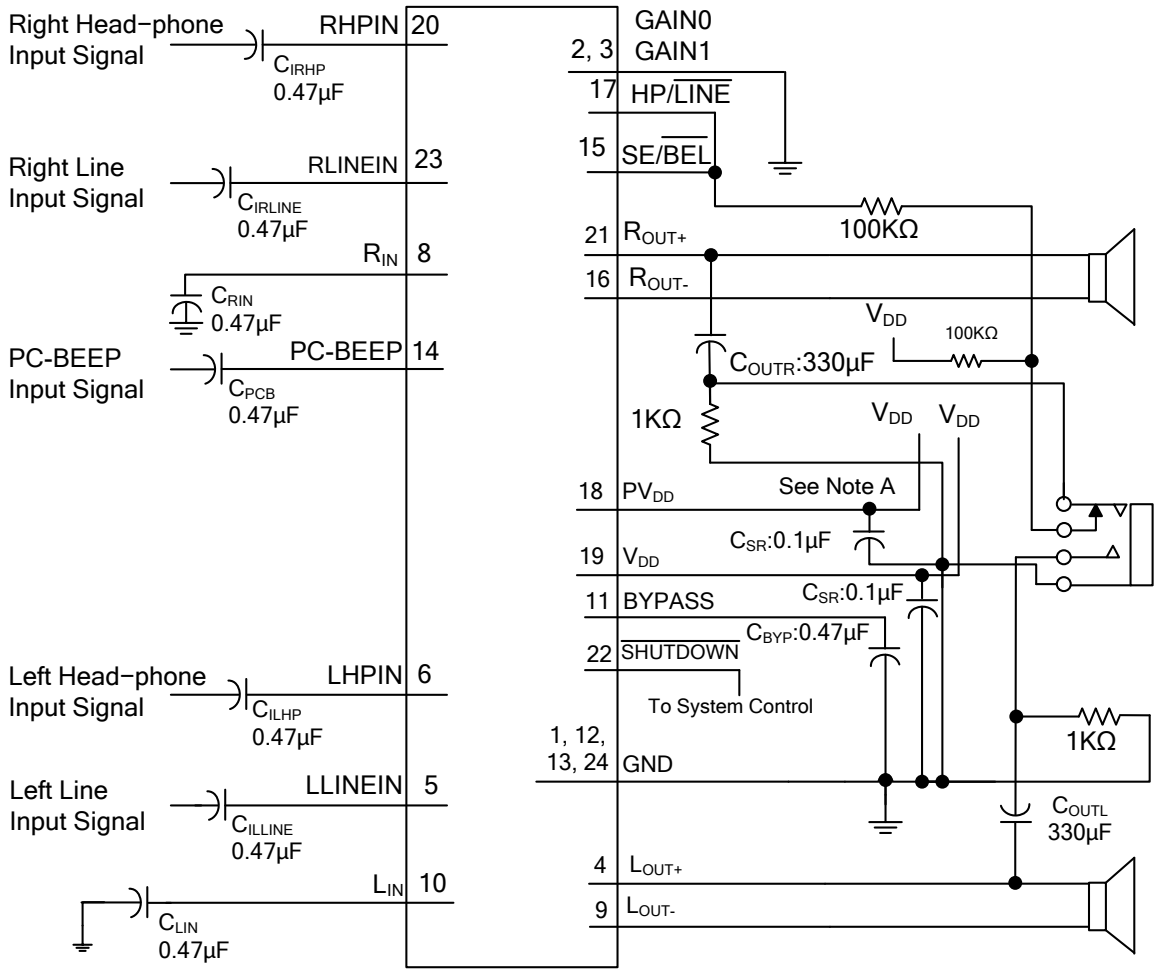
Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ ELECTRICAL CHARACTERISTICS (T_a= 25°C, unless otherwise specified.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC ELECTRICAL CHARACTERISTICS						
Supply Voltage	V_{DD}		4.5	5	5.5	V
High-Level Input voltage	V_{IH}	$\overline{SHUTDOWN}$	2			V
		SE/BTL, HP/LINE, GAIN0, GAIN1	$0.8\times V_{DD}$			V
Low-Level Input voltage	V_{IL}	$\overline{SHUTDOWN}$			0.8	V
		GAIN0, GAIN1			$0.4\times V_{DD}$	V
		SE/$\overline{BTL}$, HP/$\overline{LINE}$			$0.6\times V_{DD}$	V
DC Differential Output Voltage	$V_{OUT(DIFF)}$	V_{IN}=0V,Gain=2V/V			25	mV
Supply Current in Mute Mode	I_{DD}	BTL Mode		6	8	mA
		SE Mode		3	4	mA
Supply Current, Shutdown Mode	$I_{DD(SD)}$	V_{DD}=5V		150	300	μA
High-Level Input Current	$\|I_{IH}\|$	V_{DD}=5.5V, V_{IN}=V_{DD}			900	nA
Low-Level Input Current	$\|I_{IL}\|$	V_{DD}=5.5V, V_{IN}=0V			900	nA
Operating Free-Air Temperature	T_A		-40		+85	°C
AC ELECTRICAL CHARACTERISTICS (VDD = 5.0V, RL = 8Ω, unless otherwise noted)						
Output Power	P_{OUT}	THD=1%, BTL, R_L=3Ω, G=2V/V		2.05		W
		THD=10%, BTL, R_L=3Ω, G=2V/V		2.6		
Total Harmonic Distortion Plus Noise	THD+N	P_{OUT}=1W, BTL, R_L= 8Ω, G=2V/V		0.65		%
Max Output Power Bandwidth	B_{OM}	THD= 5%		15		kHz
Power Supply Ripple Rejection	PSRR	f=1kHz, BTL, G=2V/V, C_{BYP}=0.47μF		72		dB
Output Noise Voltage	eN	C_{BYP}=0.47μF,BTL, G=2V/V		20		μV_{RMS}
		C_{BYP}=0.47μF, SE, G=2V/V		18		μV_{RMS}
Signal-to-Noise Ratio	SNR			105		dB

Note: Output power is measured at the output terminals of the IC at 1kHz.

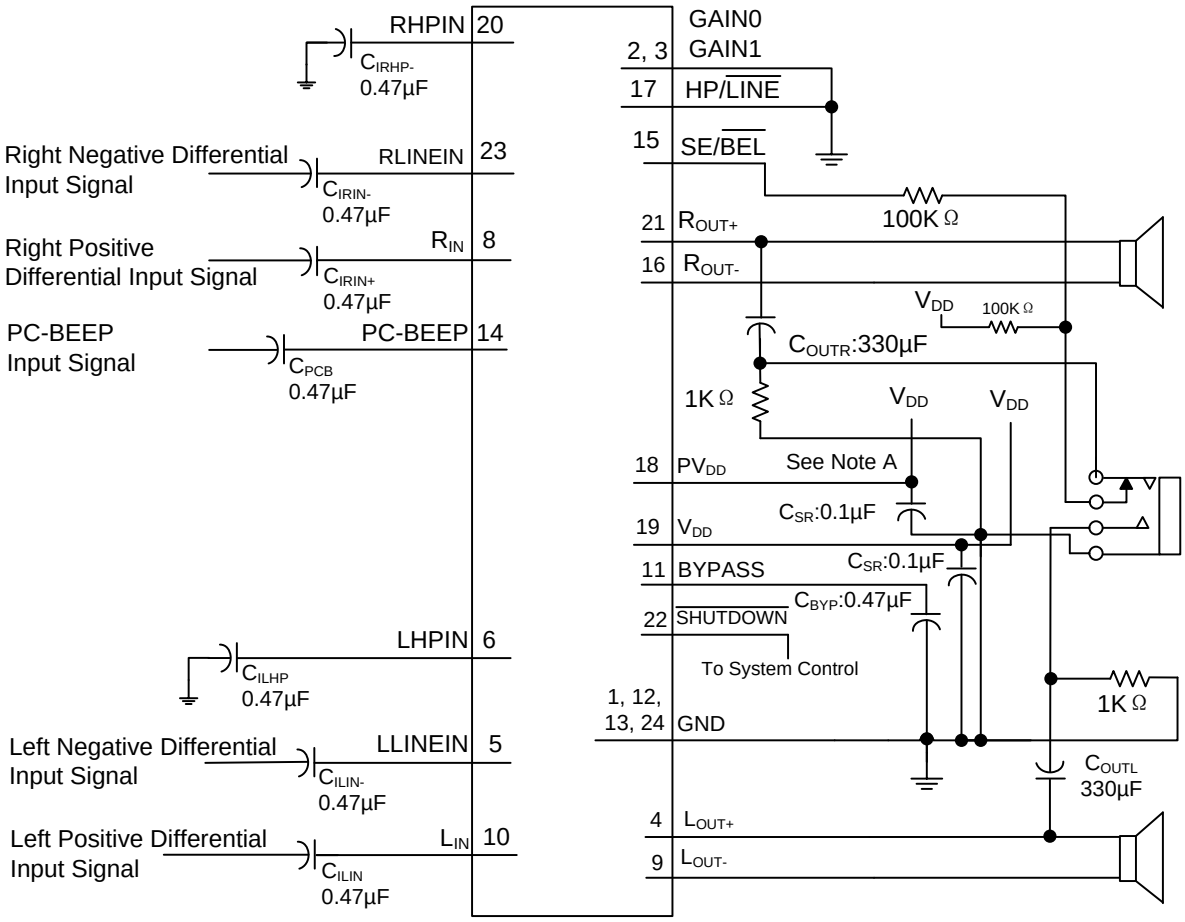
■ TYPICAL APPLICATION CIRCUITS



A 0.1-µF ceramic capacitor should be placed very close to the IC.
A larger electrolytic capacitor of 10 µF or greater should be placed near the audio power amplifier for filtering lower frequency noise signals, .

Typical PA3212 Application Circuit Using Single-Ended Inputs and Input MUX

■ TYPICAL APPLICATION CIRCUITS(Cont.)



A 0.1-µF ceramic capacitor should be placed as close as possible to the IC.
A larger electrolytic capacitor of 10 µF or greater should be placed near the audio power amplifier for filtering lower frequency noise signals.

Typical PA3212 Application Circuit Using Differential Inputs

■ APPLICATION INFORMATION

Shutdown Mode Operating

INPUT			AMPLIFIER	
HP/$\overline{\text{LINE}}$	SE/$\overline{\text{BTL}}$	$\overline{\text{SHUTDOWN}}$	INPUT	OUTPUT
X	X	L	X	MUTE
L	L	H	LINE	BTL
L	H	H	LINE	SE
H	L	H	HEADPHONE	BTL
H	H	H	HEADPHONE	SE

X: Don't care
L: Low
H: High

C_I (Input Capacitor)
The value of C_I is important to consider as it directly affects the bass performance of the application circuit. When C_I is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation, it's value can be calculate by this equation:

$C_I=1/(2\pi R_I F_C)$
R_I: Input Impedance
F_C: High-pass Filter's Frequency

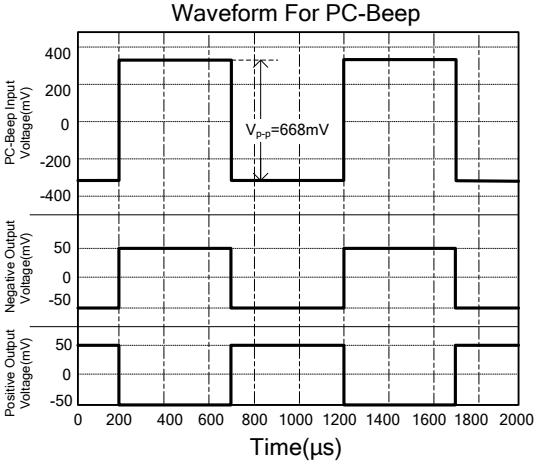
The low leakage tantalum or ceramic capacitors are suggested to be used as the input coupling capacitors, because of the small leakage current of the input capacitors will cause the dc offset voltage at the input to the amplifier that reduces the operation headroom, especially at the high gain applications. It is important to let the positive side connecting to the higher dc level of the application when using the polarized capacitors.

Gain setting (VS Gain0, Gain1 and R_I)
Gain setting is determined by GAIN0 and GAIN1. The gains listed in the next table are realized by changing the taps on the input resistors inside the amplifier which will cause the internal input impedance(R_I) to be dependent on the gain setting as we can see listed in the next table.

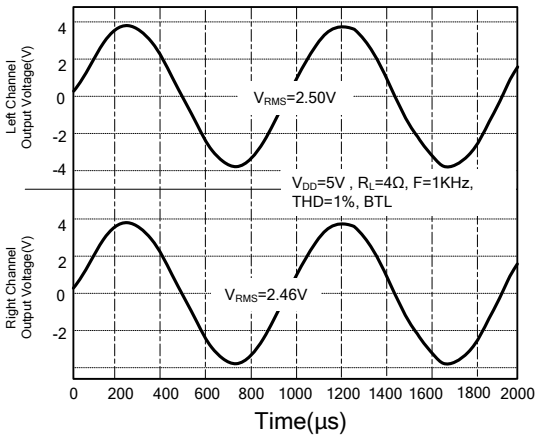
GAIN0	GAIN1	R_I(kΩ)	A_V(V/V)	SE/$\overline{\text{BTL}}$
0	0	91	2	0
0	1	45.5	6	0
1	0	26	12	0
1	1	14	24	0
X	X		1	1

■ TYPICAL CHARACTERISTICS

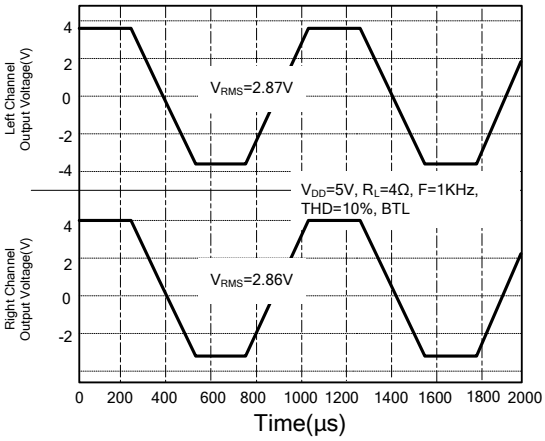
Waveform For PC-Beep



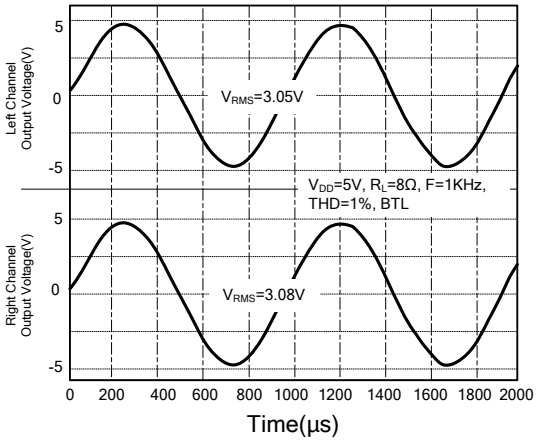
Waveform For BTL Mode



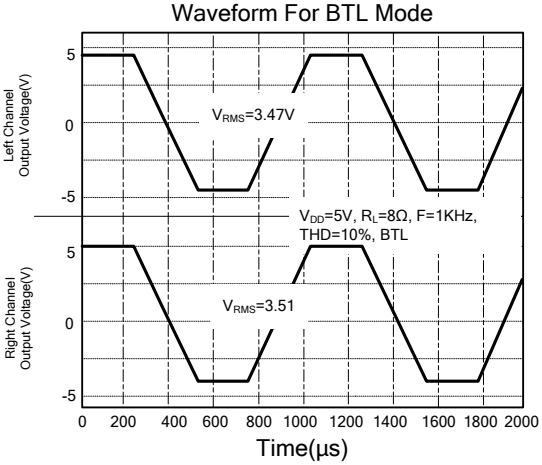
Waveform For BTL Mode



Waveform For BTL Mode



Waveform For BTL Mode



Open Loop Response