



PA4863

CMOS IC

DUAL 2.2W AUDIO AMPLIFIER PLUS STEREO HEADPHONE FUNCTION

DESCRIPTION

The UTC **PA4863** is a dual bridge-connected audio power amplifier. It combines dual bridge speaker amplifiers and stereo headphone amplifiers on one chip to simplify audio system design. In addition, the headphone input pin allows the amplifiers to operate in single-ended mode when driving stereo headphones.

The IC could deliver different power by packages as below (when connected to a 5V supply with less than 1.0% THD+N.):

- HTSSOP-20, 4Ω load: 2.2W
- HTSSOP-20, 3Ω load: 2.5W(with forced-air cooled)
- SOP/DIP, 8Ω load: 1.1W.

The UTC **PA4863** features an externally controlled, low-power consumption shutdown mode, a stereo headphone amplifier mode, and thermal shutdown protection. It also utilizes circuitry to reduce "clicks and pops" during device turn-on.

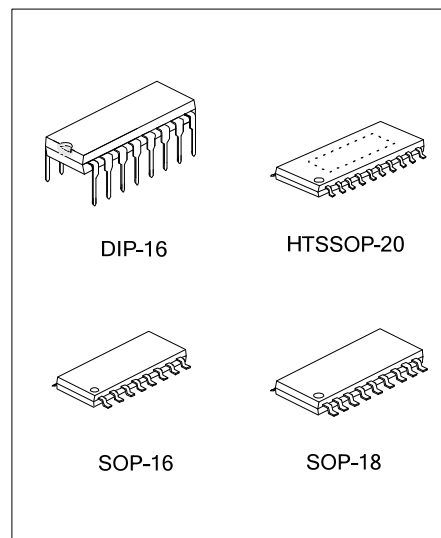
FEATURES

- * "Click and pop" suppression circuitry
- * Thermal shutdown protection circuitry
- * Unity-gain stable
- * Stereo headphone amplifier mode

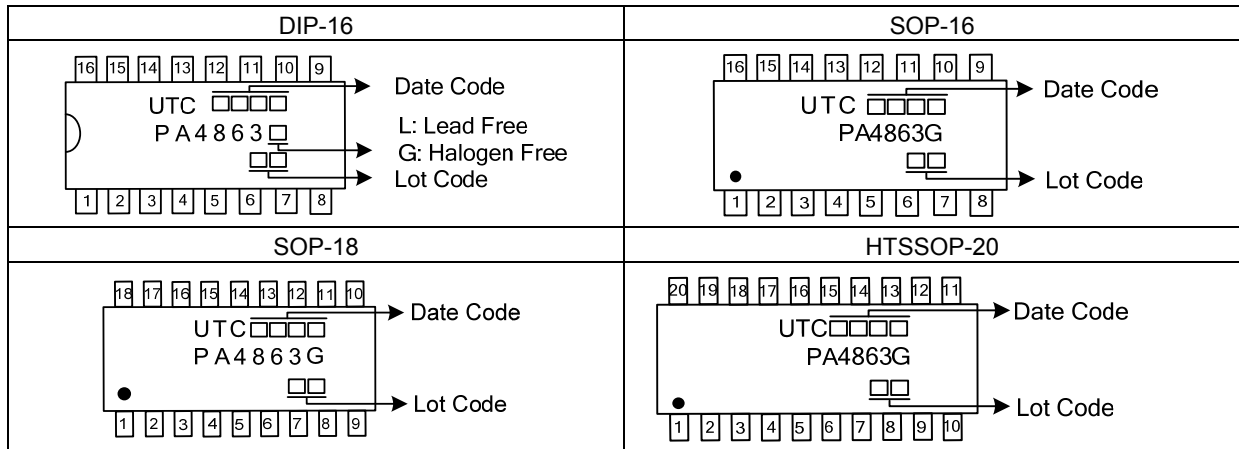
ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
PA4863L-D16-T	PA4863G-D16-T	DIP-16	Tube
-	PA4863G-S16-R	SOP-16	Tape Reel
-	PA4863G-S18-R	SOP-18	Tape Reel
-	PA4863G-N20-R	HTSSOP-20	Tape Reel

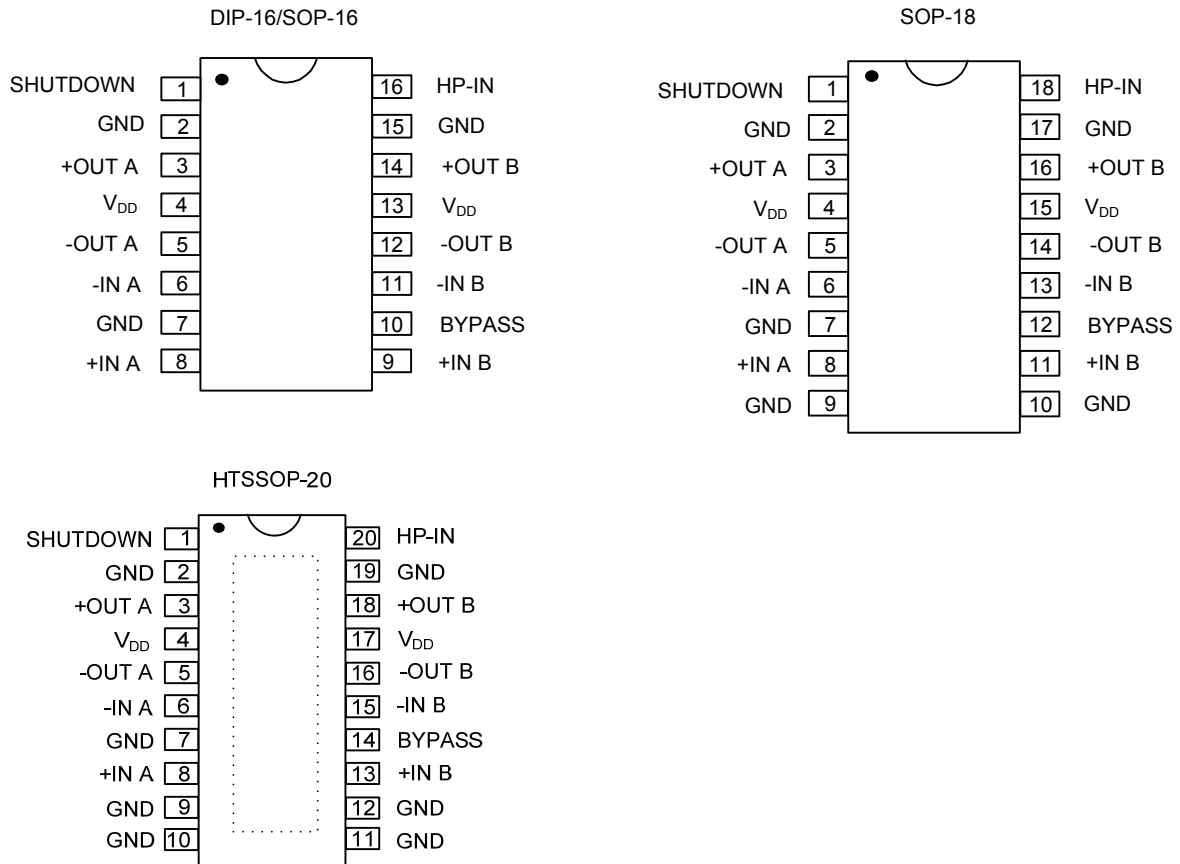
<p>PA4863L-D16-T</p> <p>(1)Packing Type (2)Package Type (3)Green Package</p>	<p>(1) T: Tube, R: Tape Reel (2) D16: DIP-16, S16: SOP-16, S18: SOP-18, N20: HTSSOP-20 (3) L: Lead Free, G: Halogen Free and Lead Free</p>
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■ MARKING



■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.		PIN NAME	I/O	PIN DESCRIPTION
DIP-16/SOP-16	SOP-18			
4,13	4,15	4,17	V _{DD}	- Supply voltage
2,7,15	2,7,9,10,17	2,7,9,10,11,12,19	GND	- Ground
10	12	14	BYPASS	- Internal mid-supply bias reference bypassing
1	1	1	SHUTDOWN	I Entire IC into the shutdown mode when this pin connected to the V _{DD}
16	18	20	HP-IN	I Output mode select, connected to the V _{DD} for SE mode or GND for BTL mode
8	8	8	+INA	I Non-inverting input of channel A, connected to BYPASS pin inside the IC
6	6	6	-INA	I Inverting input of channel A
3	3	3	+OUTA	O Channel A + output in BTL mode, high impedance in SE mode
5	5	5	-OUTA	O Channel A - output in BTL mode, + output in SE mode
9	11	13	+INB	I Non-inverting input of channel B, connected to BYPASS pin inside the IC
11	13	15	-INB	I Inverting input of channel B
14	16	18	+OUTB	O Channel B + output in BTL mode, high impedance in SE mode
12	14	16	-OUTB	O Channel B - output in BTL mode, + output in SE mode

■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}	6.0	V
Recommended Supply Voltage Range	V_{DD}	2.0 ~ 5.5	V
Input Voltage	V_{IN}	-0.3 ~ $V_{DD}+0.3$	V
Power Dissipation	P_D	Internally limited	
Junction Temperature	T_J	+125	°C
Operating Temperature	T_{OPR}	-40 ~ +85	°C
Storage Temperature	T_{STG}	-65 ~ +150	°C

Note Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	SOP-16/SOP-18	80	°C/W
	DIP-16	63	°C/W
	HTSSOP-20	90	°C/W
Junction to Case	DIP-16/SOP-16 SOP-18	20	°C/W
	HTSSOP-20	2	°C/W

■ ELECTRICAL CHARACTERISTICS (Notes 1)($V_{DD}=5V$, $T_a=25^\circ C$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIM	TYP	MAX	UNIT
FOR ENTIRE IC						
Supply Voltage	V_{DD}		2		5.5	V
Headphone Input Voltage	High	V_{IH}	4			V
		Low			0.8	V
Quiescent Power Supply Current (Note 2)	I_{DD}	$V_{IN}=0V$, $I_{OUT}=0A$, HP-IN=0V	6	11.5	20	mA
		$V_{IN}=0V$, $I_{OUT}=0A$, HP-IN=4V		5.8		
Shutdown Current	I_{SD}	V_{DD} applied to the SHUTDOWN pin	2	0.7		μA
FOR BRIDGED-MODE OPERATION						
Output Offset Voltage	$V_{O(OFF)}$	$V_{IN}=0V$		5	50	mV
Output Power (measured at the device terminals)	HTSSOP-20	P_{OUT}	THD=1%, f=1kHz	$R_L=3\Omega$	2.5	W
				$R_L=4\Omega$	2.2	
	THD+N=10%, f=1kHz		$R_L=3\Omega$	3.2		
			$R_L=4\Omega$	2.7		
	SOP/DIP	THD=1%, f=1kHz	$R_L=8\Omega$	1.0	1.1	W
THD+N=10%, f=1kHz		$R_L=8\Omega$		1.5		
THD+N=1%, f=1kHz, $R_L=32\Omega$				0.34	W	
Total Harmonic Distortion + Noise	HTSSOP-20 SOP/DIP	THD+N	20Hz $\leq f \leq$ 20kHz, $A_{VD}=2$	$R_L=4\Omega$, $P_{OUT}=2W$	0.3	%
				$R_L=8\Omega$, $P_{OUT}=1W$	0.3	
Power Supply Rejection Ratio	PSRR	$V_{DD}=5V$, $V_{RIPPLE}=200mV_{RMS}$, $R_L=8\Omega$, $C_B=1.0\mu F$		67		dB
Channel Separation	XTALK	f=1kHz, $C_B=1.0\mu F$		90		dB
Signal To Noise Ratio	SNR	$V_{DD}=5V$, $P_{OUT}=1.1W$, $R_L=8\Omega$		98		dB

■ ELECTRICAL CHARACTERISTICS(Cont.)

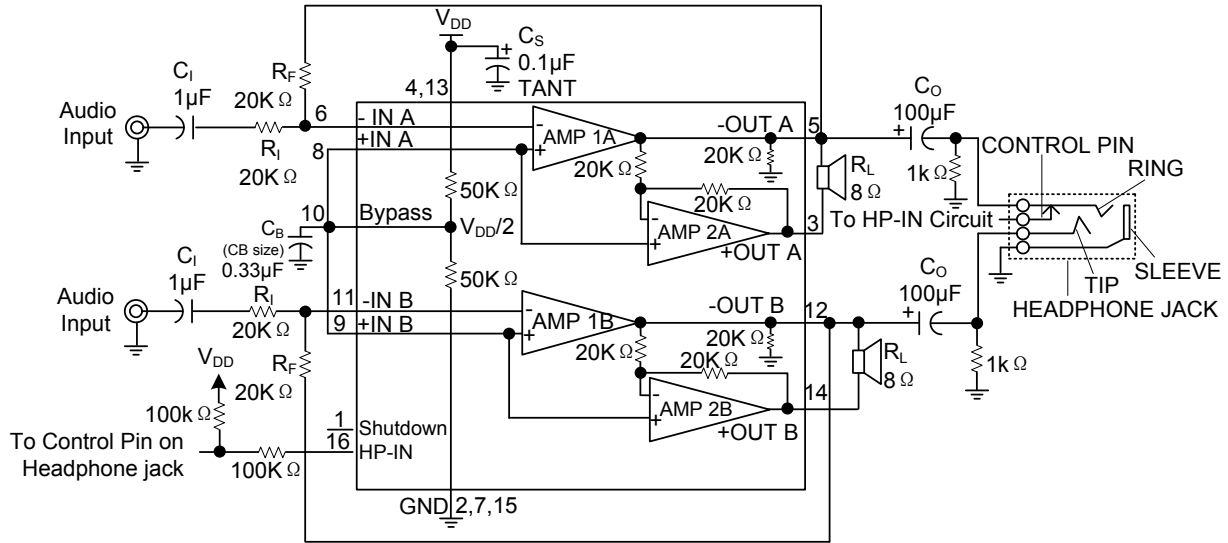
PARAMETER	SYMBOL	TEST CONDITIONS	MIM	TYP	MAX	UNIT
FOR SINGLE-ENDED OPERATION						
Output Offset Voltage	$V_{O(OFF)}$	$V_{IN}=0V$		5	50	mV
Output Power	P_{OUT}	THD=0.5%, f=1kHz, $R_L=32\Omega$	75	85		mW
		THD+N=1%, f=1kHz, $R_L=8\Omega$		340		
		THD+N=10%, f=1kHz, $R_L=8\Omega$		440		
Total Harmonic Distortion + Noise	THD+N	$A_V=-1$, $P_{OUT}=75mW$, $20Hz \leq f \leq 20kHz$, $R_L=32\Omega$		0.2		%
Power Supply Rejection Ratio	PSRR	$C_B=1.0\mu F$, $V_{RIPPLE}=200mV_{RMS}$, f=1kHz		52		dB
Channel Separation	X_{TALK}	f=1kHz, $C_B=1.0\mu F$		60		dB
Signal To Noise Ratio	SNR	$V_{DD}=5V$, $P_{OUT}=340mW$, $R_L=8\Omega$		95		dB

Note: 1. All voltages are measured with respect to the ground (GND) pins, unless otherwise specified.

2. Depends on the offset voltage when a practical load is connected to the amplifier.

3. When driving 3Ω or 4Ω and operating on a 5V supply, the HTSSOP-20 package must be mounted to the circuit board that has a minimum of 2.5 in^2 of exposed, uninterrupted copper area connected to the exposed-DAP.

■ TYPICAL APPLICATION CIRCUIT



Note: Pin out shown for DIP-16. Refer to the PIN CONFIGURATION for the pin out of other packages.

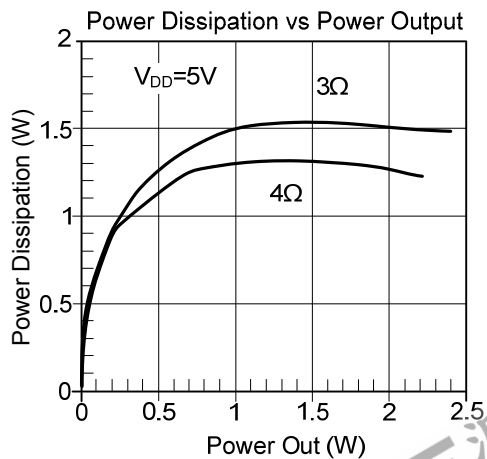
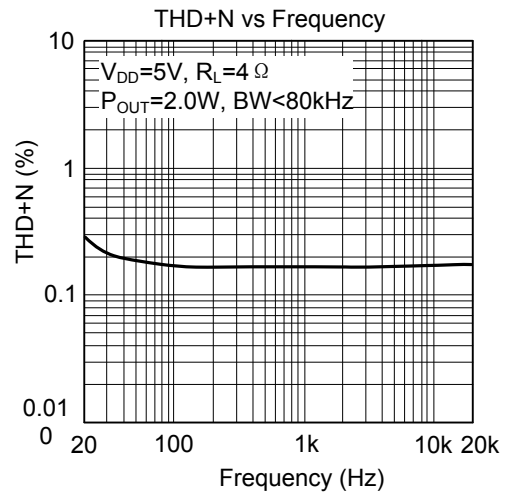
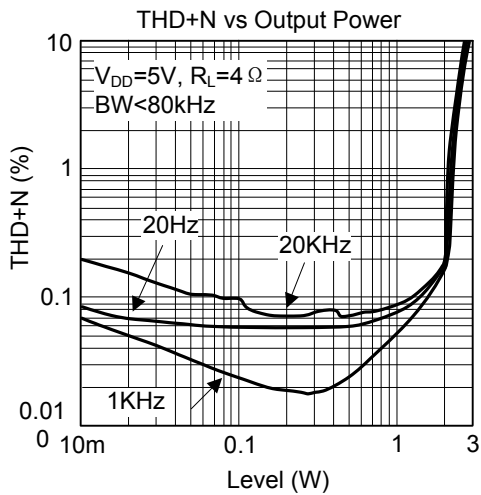
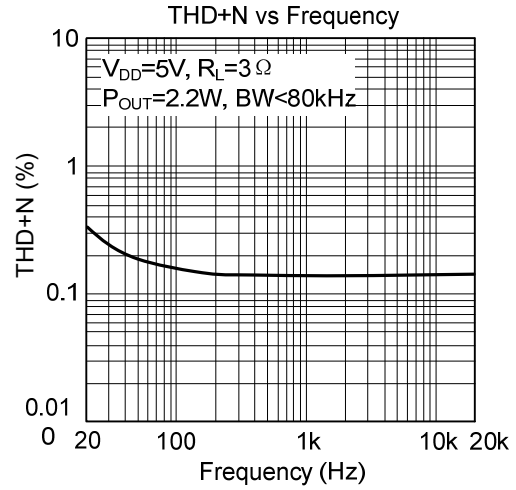
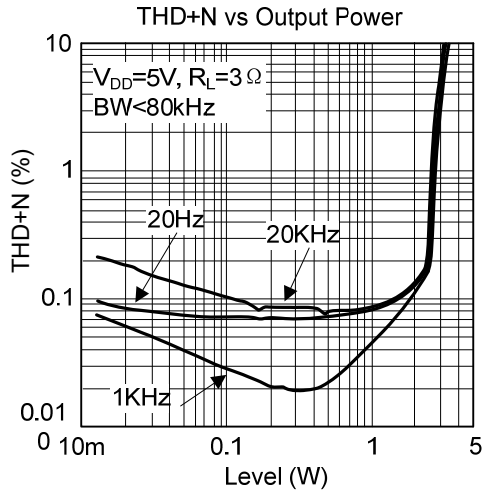
Figure 1. Typical Audio Amplifier Application Circuit

■ EXTERNAL COMPONENTS DESCRIPTION

Components	Functional Description
R_i	The inverting input resistance, along with R_F , set the closed-loop gain. R_i , along with C_i form a high pass filter with $f_c=1/(2\pi R_i C_i)$
C_i	The input coupling capacitor blocks DC voltage at the amplifier’s input terminals. C_i , along with R_i , create a high pass filter with $f_c=1/(2\pi R_i C_i)$. Refer to the section. Selecting Proper External Components, for an explanation of determine the value of C_i .
R_F	The feedback resistance, along with R_i , set the closed-loop gain.
C_s	The supply bypass capacitor. Refer to the Power Supply Bypassing section for information about properly placing and selecting the value of, this capacitor.
C_B	The capacitor, C_B , filters the half-supply voltage present on the Bypass pin. Refer to the Selecting Proper External Components section for information concerning proper placement and selecting C_B 'S value.

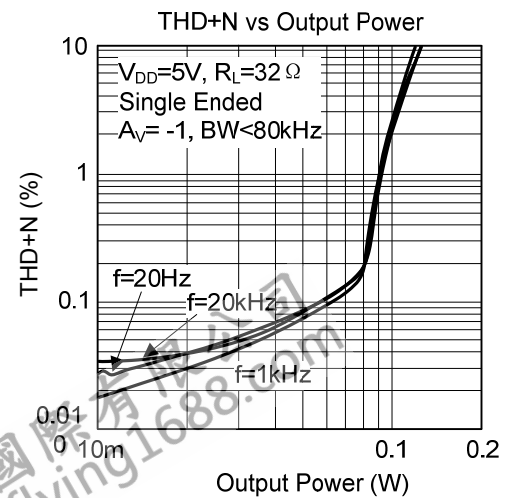
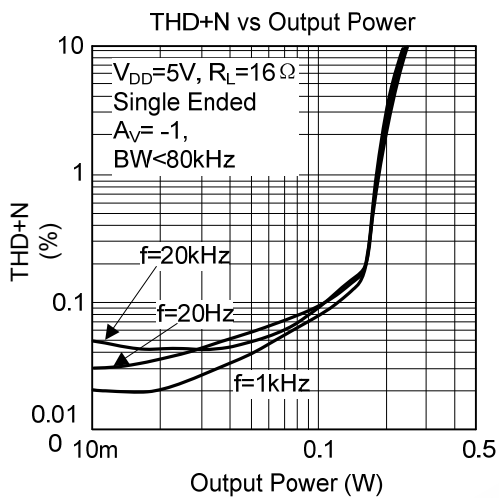
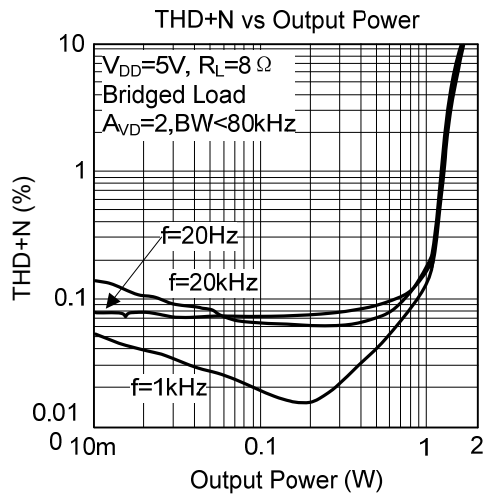
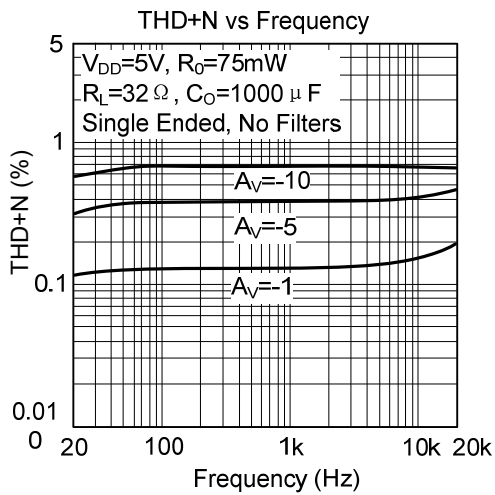
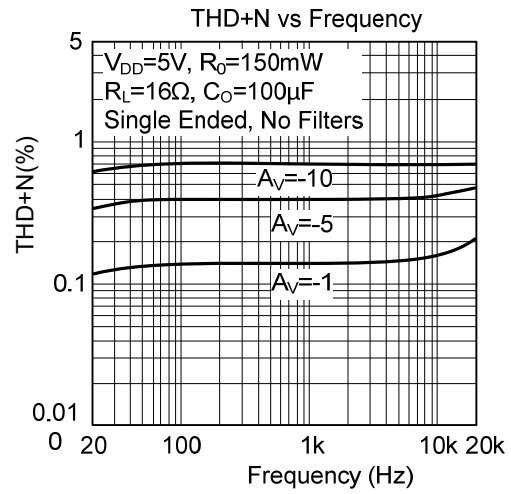
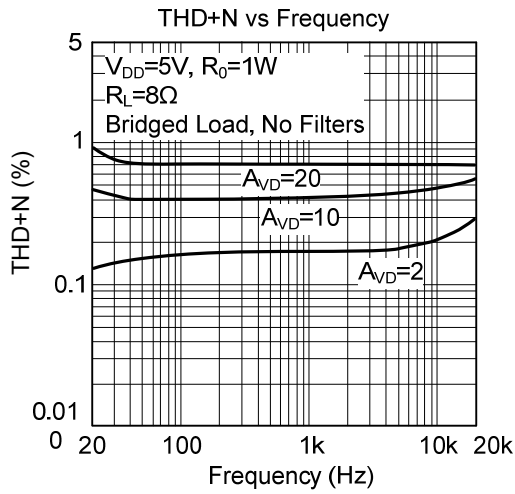
■ TYPICAL CHARACTERISTICS

(For HTSSOP-20)

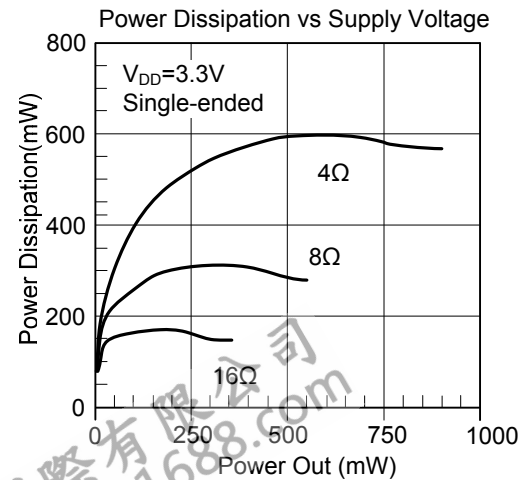
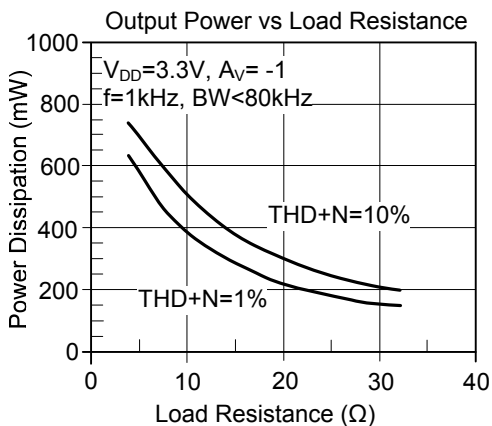
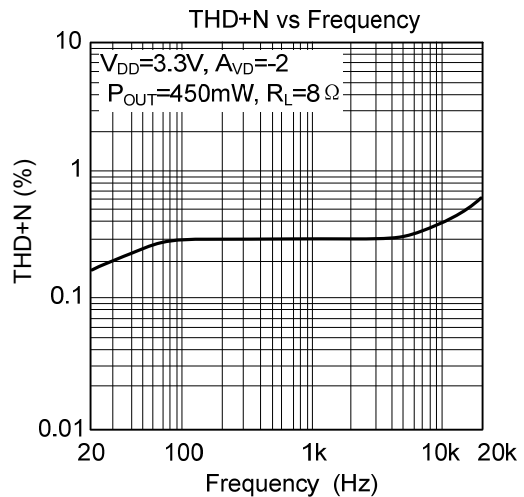
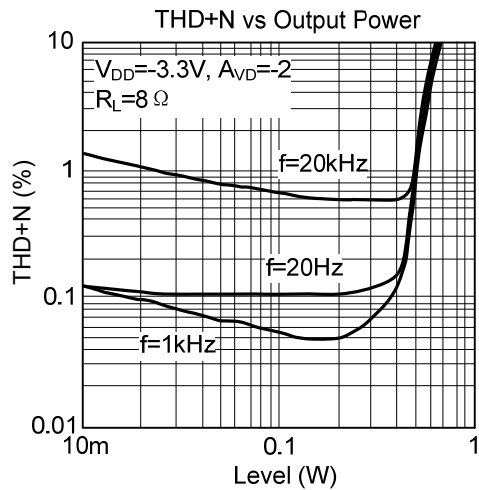
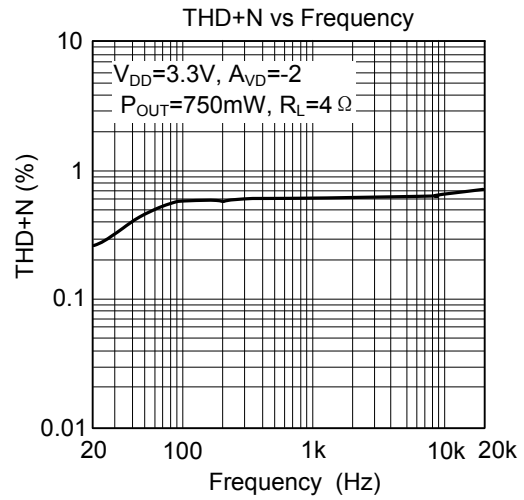
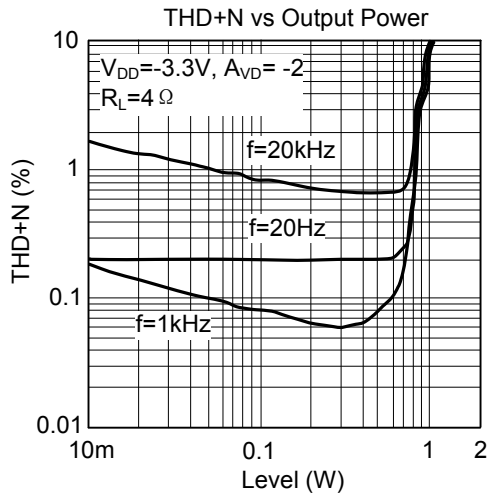


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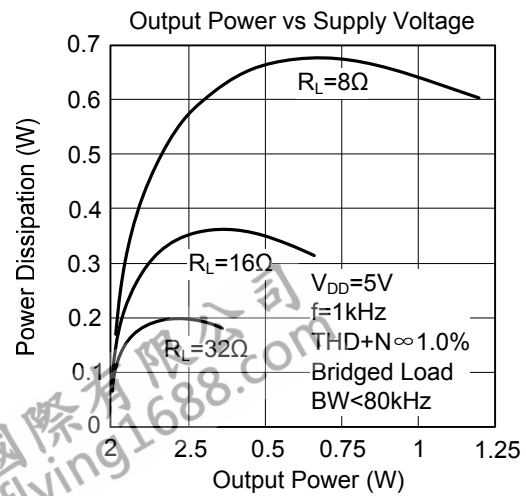
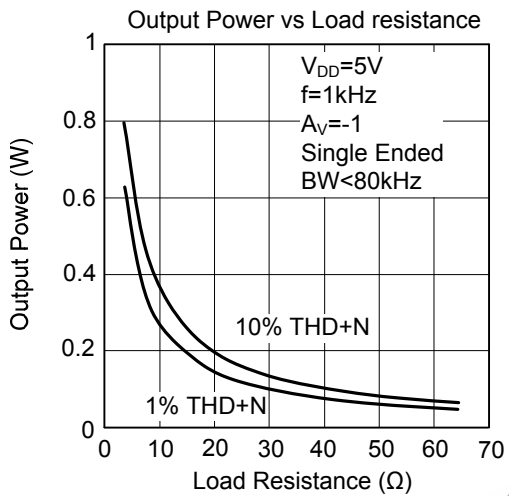
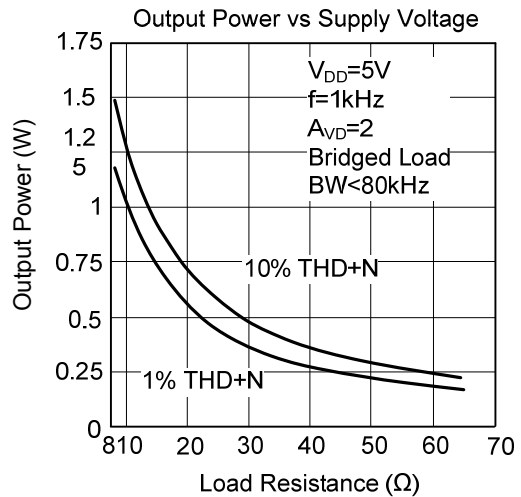
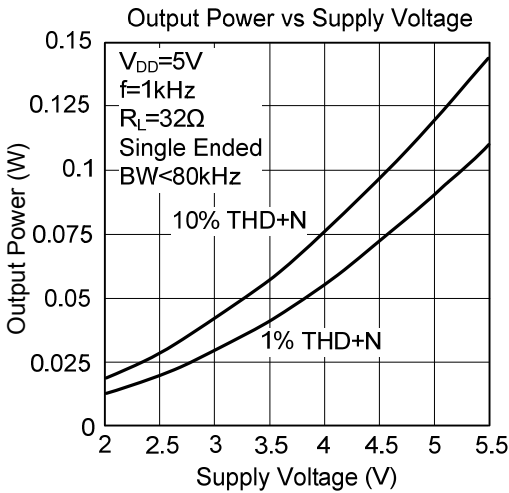
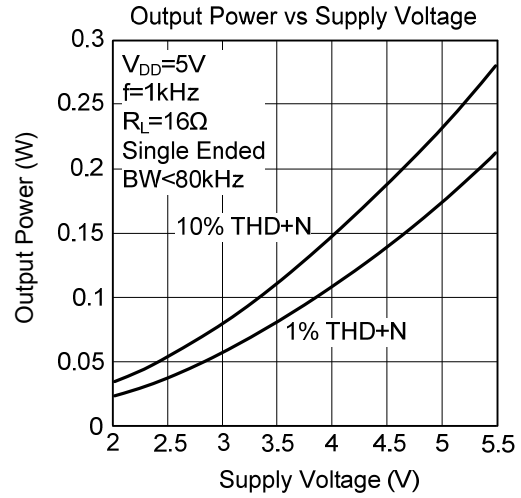
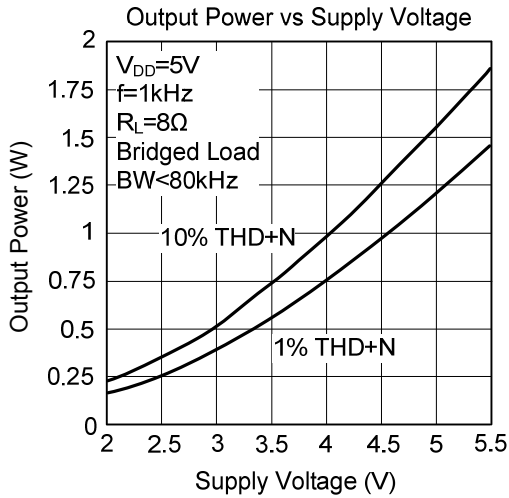
(For DIP-16, SOP-16 and SOP-18)



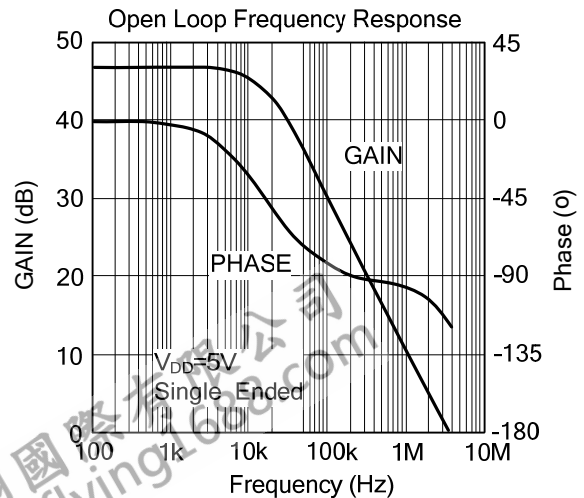
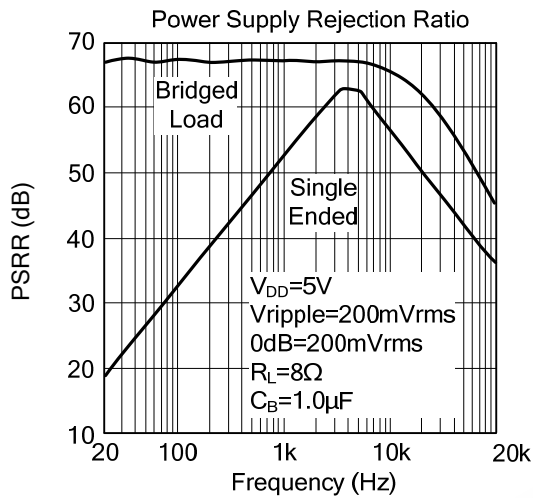
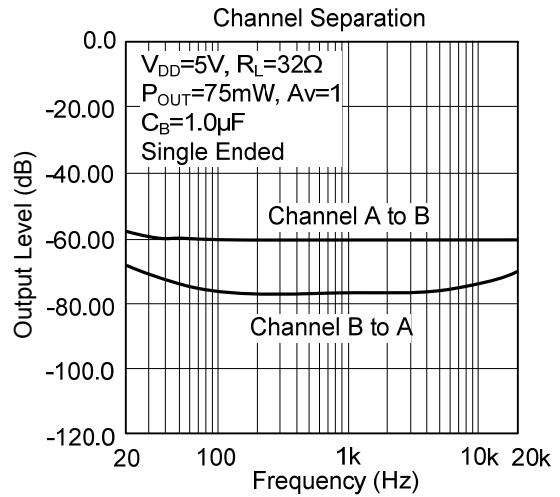
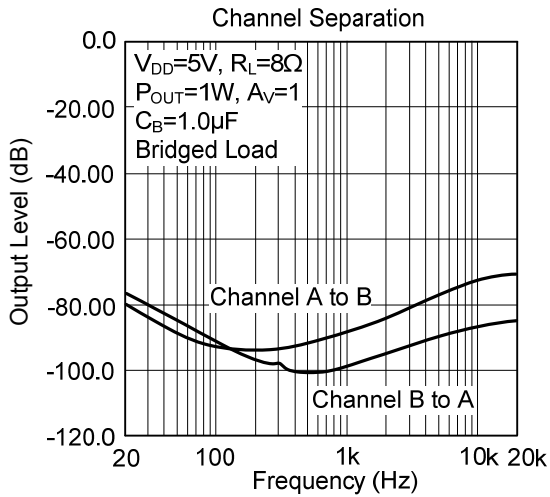
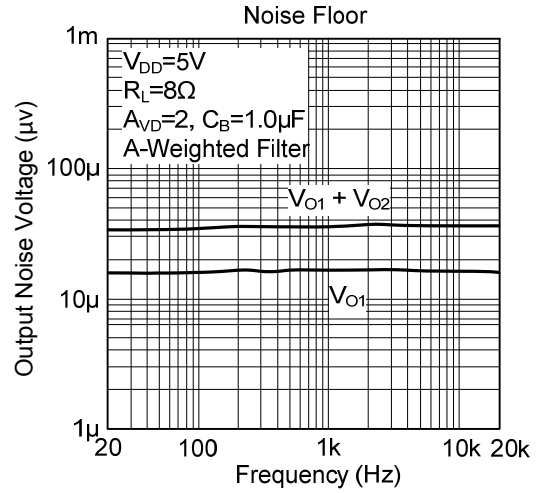
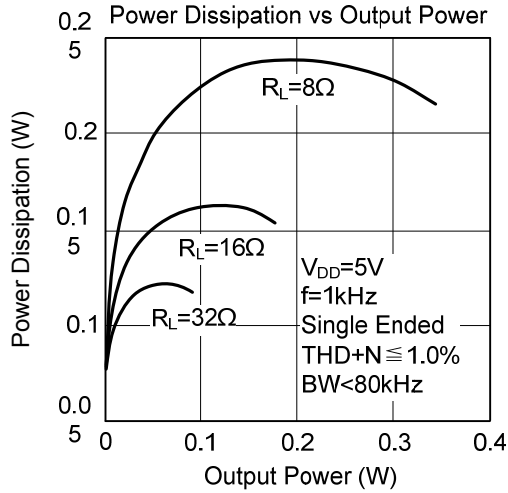
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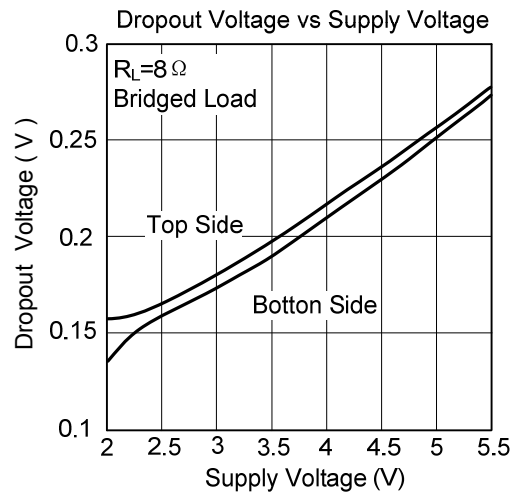
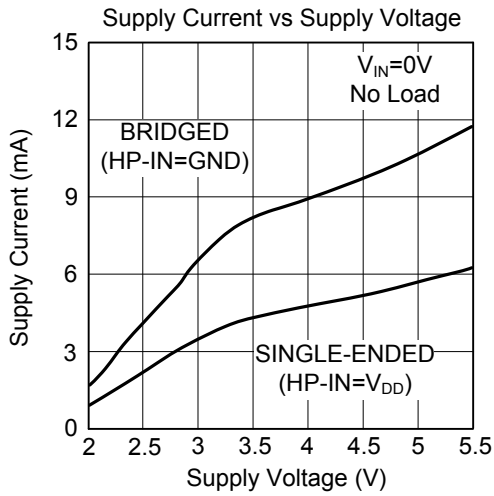
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