



## U74AHC02

CMOS IC

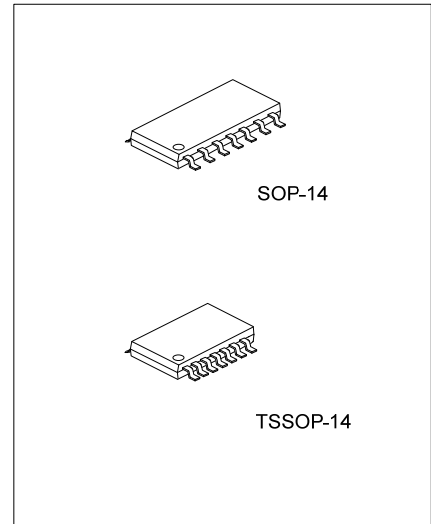
### 2-INPUT NOR GATE

#### DESCRIPTION

The UTC **U74AHC02** are independent 2-input NOR gates which provides the function  $Y = \overline{A+B}$ .

#### FEATURES

- \* Operation Voltage Range: 2.0~5.5V
- \* Low Power Dissipation
- \* High Noise Immunity
- \* Balanced Propagation Delays

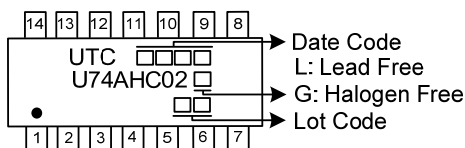


#### ORDERING INFORMATION

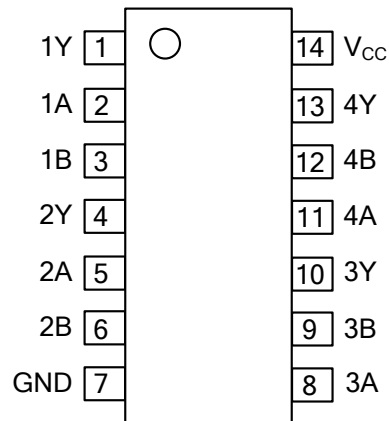
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74AHC02L-S14-R	U74AHC02G-S14-R	SOP-14	Tape Reel
U74AHC02L-P14-R	U74AHC02G-P14-R	TSSOP-14	Tape Reel

<p>U74AHC02G-S14-R</p> <p>(1) Packing Type</p> <p>(2) Package Type</p> <p>(3) Green Package</p>	<p>(1) R: Tape Reel</p> <p>(2) S14: SOP-14, P14: TSSOP-14</p> <p>(3) G: Halogen Free and Lead Free, L: Lead Free</p>
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#### MARKING



■ PIN CONFIGURATION



■ FUNCTION TABLE

INPUT		OUTPUT
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

■ LOGIC DIAGRAM (positive logic)



IEC logic symbol

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■ ABSOLUTE MAXIMUM RATINGS (unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	$V_{CC}$	-0.5~+7	V
Input Voltage	$V_{IN}$	-0.5~+7	V
Output Voltage	$V_{OUT}$	-0.5~ $V_{CC}+0.5$	V
Input Clamp Current	$I_{IK}$	-20	mA
Output Clamp Current	$I_{OK}$	$\pm 20$	mA
Continuous Output Current	$I_{OUT}$	$\pm 25$	mA
$V_{CC}$ or GND Current	$I_{CC}$	$\pm 50$	mA
Storage Temperature	$T_{STG}$	-65 ~ + 150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
Supply Voltage	$V_{CC}$		2		5.5	V	
Input Voltage	$V_{IN}$		0		5.5	V	
Output Voltage	$V_{OUT}$	High or low state	0		$V_{CC}$	V	
Input Voltage	High	$V_{IH}$	$V_{CC}=2V$	1.5		V	
			$V_{CC}=3V$	2.1		V	
			$V_{CC}=5.5V$	3.85		V	
	Low	$V_{IL}$	$V_{CC}=2V$			0.5	V
			$V_{CC}=3V$			0.9	V
			$V_{CC}=5.5V$			1.65	V
Output Current	High	$I_{OH}$	$V_{CC}=2V$			-50	$\mu A$
			$V_{CC}=3.3V \pm 0.3V$			-4	mA
			$V_{CC}=5V \pm 0.5V$			-8	mA
	Low	$I_{OL}$	$V_{CC}=2V$			50	$\mu A$
			$V_{CC}=3.3V \pm 0.3V$			4	mA
			$V_{CC}=5V \pm 0.5V$			8	mA
Input Rise or Fall Times	$\frac{\Delta t}{\Delta V}$	$V_{CC}=3.3V \pm 0.3V$			100	ns/V	
		$V_{CC}=5V \pm 0.5V$			20	ns/V	
Operating Temperature	$T_{OPR}$		-40		125	°C	

■ ELECTRICAL CHARACTERISTICS ( $T_A=25^\circ C$ , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
Output Voltage	High	$V_{OH}$	$V_{CC}=2.0V, I_{OH}=-50\mu A$	1.9	2.0		V
			$V_{CC}=3.0V, I_{OH}=-50\mu A$	2.9	3.0		V
			$V_{CC}=4.5V, I_{OH}=-50\mu A$	4.4	4.5		V
			$V_{CC}=3.0V, I_{OH}=-4mA$	2.58			V
			$V_{CC}=4.5V, I_{OH}=-8mA$	3.94			V
	Low	$V_{OL}$	$V_{CC}=2.0V, I_{OL}=50\mu A$			0.1	V
			$V_{CC}=3.0V, I_{OL}=50\mu A$			0.1	V
			$V_{CC}=4.5V, I_{OL}=50\mu A$			0.1	V
			$V_{CC}=3.0V, I_{OL}=4mA$			0.36	V
			$V_{CC}=4.5V, I_{OL}=8mA$			0.36	V
Input Leakage Current	$I_{I(LEAK)}$	$V_{CC}=0\sim 5.5V, V_{IN}=5.5V$ or GND			$\pm 0.1$	$\mu A$	
Quiescent Supply Current	$I_Q$	$V_{CC}=5.5V, V_{IN}=V_{CC}$ or GND, $I_{OUT}=0$			2	$\mu A$	
Input Capacitance	$C_{IN}$	$V_{CC}=5.0V, V_{IN}=V_{CC}$ or GND		4	10	pF	

Note: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation.

■ SWITCHING CHARACTERISTICS (see Test Circuit and Waveforms)

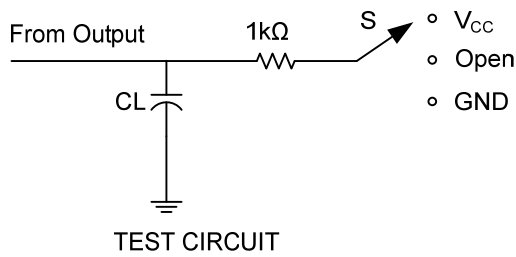
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation delay from input (A or B) to output(Y)	t <sub>PLH</sub> /t <sub>PHL</sub>	V <sub>CC</sub> =3.3V±0.3V, C <sub>L</sub> =15pF		5.6	7.9	ns
		V <sub>CC</sub> =3.3V±0.3V, C <sub>L</sub> =50pF		8.1	11.4	ns
	t <sub>PLH</sub> /t <sub>PHL</sub>	V <sub>CC</sub> =5.0V±0.5V, C <sub>L</sub> =15pF		3.6	5.5	ns
		V <sub>CC</sub> =5.0V±0.5V, C <sub>L</sub> =50pF		5.1	7.5	ns

■ OPERATING CHARACTERISTICS (V<sub>CC</sub>=5V, T<sub>a</sub>=25°C)

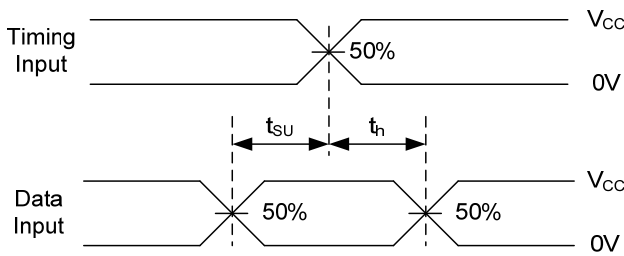
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	C <sub>PD</sub>	No load, f=1MHz		15		pF

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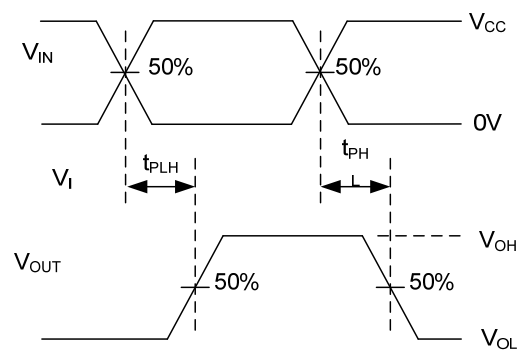
## ■ TEST CIRCUIT AND WAVEFORMS



TEST	S
t <sub>PLH</sub> /t <sub>PHL</sub>	Open
t <sub>PHZ</sub> /t <sub>PZH</sub>	GND
t <sub>PLZ</sub> /t <sub>PZL</sub>	V <sub>CC</sub>



SETUP TIME AND HOLD TIME



PROPAGATION DELAY TIMES

Note: C<sub>L</sub> includes probe and jig capacitance.

P<sub>RR</sub> ≤ 1MHz, Z<sub>O</sub> = 50Ω, t<sub>r</sub> ≤ 3ns, t<sub>f</sub> ≤ 3ns.

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