



## U74AHC373

CMOS IC

### OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

#### DESCRIPTION

The **U74AHC373** is an octal transparent D-type latch with 3-state outputs, and it has 8 channels.

When the  $\overline{OE}$  input is low and the LE input is high, the Q outputs follow the D inputs. When  $\overline{OE}$  is low and LE is low, the Q outputs are latched at the logic levels of the D inputs.

When the  $\overline{OE}$  input is high, the outputs are in the high-impedance. The  $\overline{OE}$  does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pull-up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

#### FEATURES

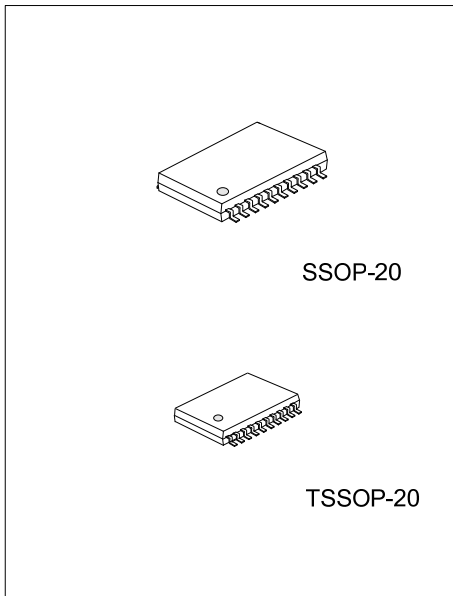
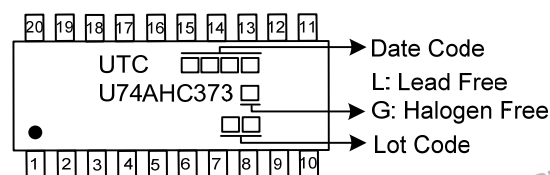
- \* Operate from 2V to 5.5V
- \* Inputs Accept Voltages to 5.5V
- \* Max  $t_{PD}$  of 13.5ns at  $V_{CC}=3.3V$ ,  $C_L=15pF$
- \* Typ  $V_{OL} < 0.36V$  at  $V_{CC}=3V$ ,  $I_{OL}=4mA$ ,  $T_A=25^\circ C$
- \* Typ  $V_{OH} > 2.58V$  at  $V_{CC}=3V$ ,  $I_{OH}=-4mA$ ,  $T_A=25^\circ C$

#### ORDERING INFORMATION

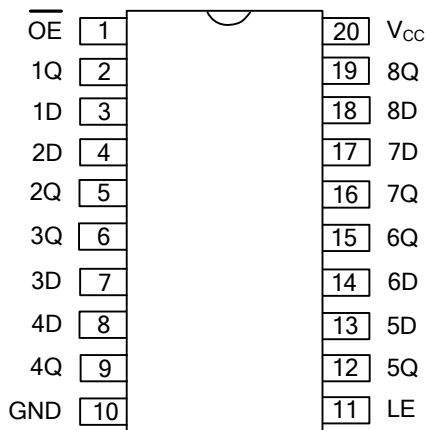
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74AHC373L-R20-T	U74AHC373G-R20-T	SSOP-20	Tube
U74AHC373L-P20-R	U74AHC373G-P20-R	TSSOP-20	Tape Reel

<p>U74AHC373G-S20-T</p> <p>(1) Packing Type (2) Package Type (3) Green Package</p>	<p>(1) R: Tape Reel (2) R20: SSOP-20, P20: TSSOP-20 (3) G: Halogen Free and Lead Free, L: Lead Free</p>
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#### MARKING



## PIN CONFIGURATION

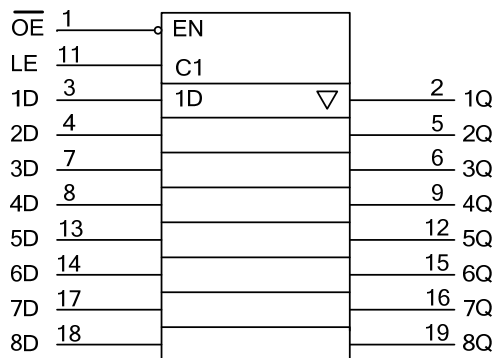


### FUNCTION TABLE

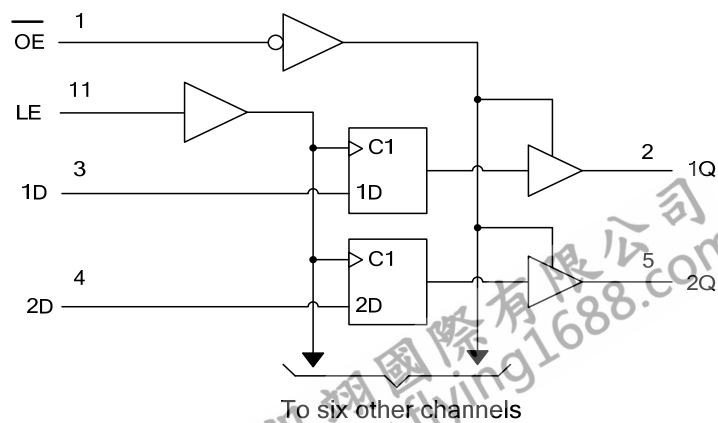
INPUTS( $\overline{OE}$ )	INPUTS(LE)	INPUTS(D)	OUTPUT(Q)
L	H	H	H
L	H	L	L
L	L	X	$Q_0$
H	X	X	Z

Note: H: HIGH voltage level; L: LOW voltage level.

### LOGIC SYMBOL



### LOGIC DIAGRAM



### ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Supply voltage	$V_{CC}$	-0.5 ~ 7	V
Input voltage (Note 2)	$V_I$	-0.5 ~ 7	V
Output voltage (Note 2)	$V_O$	-0.5 ~ $V_{CC} + 0.5$	V
Input clamp current	$I_{IK}$	-20	mA
Output clamp current	$I_{OK}$	±20	mA
Output current	$I_O$	±25	mA
$V_{CC}$ or GND current	$I_{CC}$	±75	mA
Storage temperature	$T_{STG}$	-65 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
Supply Voltage	$V_{CC}$		2		5.5	V	
High-Level Input Voltage	$V_{IH}$	$V_{CC} = 2\text{ V}$	1.5			V	
		$V_{CC} = 3\text{ V}$	2.1				
		$V_{CC} = 5.5\text{ V}$	3.85				
Low-Level Input Voltage	$V_{IL}$	$V_{CC} = 2\text{ V}$			0.5	V	
		$V_{CC} = 3\text{ V}$			0.9		
		$V_{CC} = 5.5\text{ V}$			1.65		
Input Voltage	$V_{IN}$		0		5.5	V	
Output Voltage	$V_{OUT}$		0		$V_{CC}$	V	
High-Level Output Current	$I_{OH}$	$V_{CC} = 2\text{ V}$			-50	μA	
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$			-4		mA
		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$			-8		
Low-Level Output Current	$I_{OL}$	$V_{CC} = 2\text{ V}$			50	μA	
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$			4		mA
		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$			8		
Input Rise or Fall Times	$t_R, t_F$	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$			100	ns/V	
		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$			20		

### ELECTRICAL CHARACTERISTICS ( $T_A=25^\circ\text{C}$ )

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Voltage High-Level	$V_{OH}$	$V_{CC}=2\text{V}, I_{OH}=-50\mu\text{A}$	1.9			V
		$V_{CC}=3\text{V}, I_{OH}=-50\mu\text{A}$	2.9			
		$V_{CC}=4.5\text{V}, I_{OH}=-50\mu\text{A}$	4.4			
		$V_{CC}=3\text{V}, I_{OH}=-4\text{mA}$	2.58			
		$V_{CC}=4.5\text{V}, I_{OH}=-8\text{mA}$	3.94			
Output Voltage Low-Level	$V_{OL}$	$V_{CC}=2\text{V}, I_{OL}=50\mu\text{A}$			0.1	V
		$V_{CC}=3\text{V}, I_{OL}=50\mu\text{A}$			0.1	
		$V_{CC}=4.5\text{V}, I_{OL}=50\mu\text{A}$			0.1	
		$V_{CC}=3\text{V}, I_{OL}=4\text{mA}$			0.36	
		$V_{CC}=4.5\text{V}, I_{OL}=8\text{mA}$			0.36	
Input Leakage Current	$I_{(LEAK)}$	$V_{CC}=0\text{V to } 5.5\text{V}, V_{IN}=0\text{ or } 5.5\text{V}$			±0.1	μA
Leakage Current (For output in high-impedance state)	$I_{OZ}$	$V_{CC}=5.5\text{V}, V_{IN}=V_{IH}\text{ or } V_{IL}, V_{OUT}=0\text{ or } 5.5\text{V}$			±0.25	μA
Quiescent Supply Current	$I_Q$	$V_{CC}=5.5\text{V}, V_{IN}=V_{CC}\text{ or GND}, I_{OUT}=0$			4	μA
Input Capacitance	$C_I$	$V_{CC}=5\text{V}, V_{IN}=V_{CC}\text{ or GND}$		4	10	pF
Output Capacitance	$C_O$	$V_{CC}=5\text{V}, V_{OUT}=V_{CC}\text{ or GND}$		6		pF

### SWITCHING CHARACTERISTICS

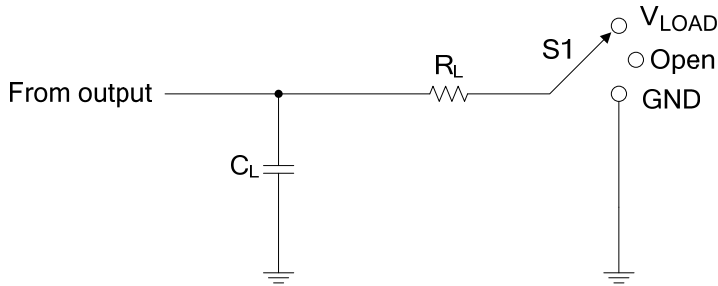
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
From D to Q	$t_{PLH}/t_{PHL}$	$V_{CC}=3.3V\pm 0.3V, C_L=15pF$		7.3	11.4	ns
		$V_{CC}=3.3V\pm 0.3V, C_L=50pF$		9.8	14.9	
		$V_{CC}=5V\pm 0.5V, C_L=15pF$		5	7.2	
		$V_{CC}=5V\pm 0.5V, C_L=50pF$		6.5	9.2	
From LE to Q		$V_{CC}=3.3V\pm 0.3V, C_L=15pF$		7	11	
		$V_{CC}=3.3V\pm 0.3V, C_L=50pF$		9.5	14.5	
		$V_{CC}=5V\pm 0.5V, C_L=15pF$		4.9	7.2	
		$V_{CC}=5V\pm 0.5V, C_L=50pF$		6.4	9.2	
From $\overline{OE}$ to Q	$t_{PZL}/t_{PZH}$	$V_{CC}=3.3V\pm 0.3V, C_L=15pF$		7.3	11.4	ns
		$V_{CC}=3.3V\pm 0.3V, C_L=50pF$		9.8	14.9	
		$V_{CC}=5V\pm 0.5V, C_L=15pF$		5.5	8.1	
		$V_{CC}=5V\pm 0.5V, C_L=50pF$		7	10.1	
From $\overline{OE}$ to Q	$t_{PLZ}/t_{PHZ}$	$V_{CC}=3.3V\pm 0.3V, C_L=15pF$		7	10	ns
		$V_{CC}=3.3V\pm 0.3V, C_L=50pF$		9.5	13.2	
		$V_{CC}=5V\pm 0.5V, C_L=15pF$		5	7.2	
		$V_{CC}=5V\pm 0.5V, C_L=50pF$		6.5	9.2	
Pulse Width, LE high	$t_w$	$V_{CC}=3.3V\pm 0.3V$	5			ns
		$V_{CC}=5V\pm 0.5V$	5			
Setup Time, data before LE $\downarrow$	$t_{SU}$	$V_{CC}=3.3V\pm 0.3V$	4			ns
		$V_{CC}=5V\pm 0.5V$	4			
Hold Time, data after LE $\downarrow$	$t_H$	$V_{CC}=3.3V\pm 0.3V$	1			ns
		$V_{CC}=5V\pm 0.5V$	1			

### OPERATING CHARACTERISTICS ( $T_A=25^\circ C$ )

PARAMETER	SYMBOL	TEST CONDITIONS	RATINGS	UNIT
Power Dissipation Capacitance	$C_{PD}$	No load, f=1MHz	18	pF

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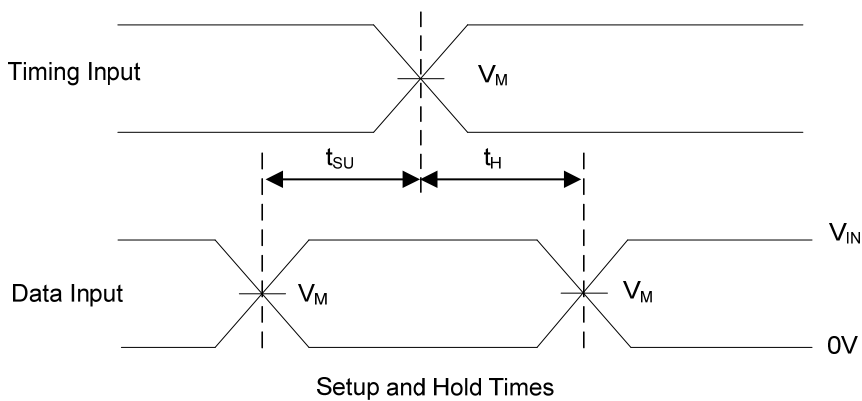
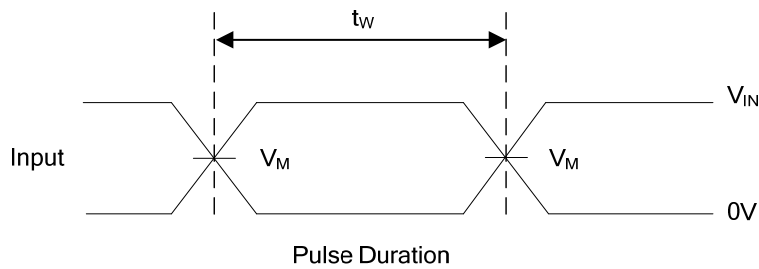
■ TEST CIRCUIT AND WAVEFORMS



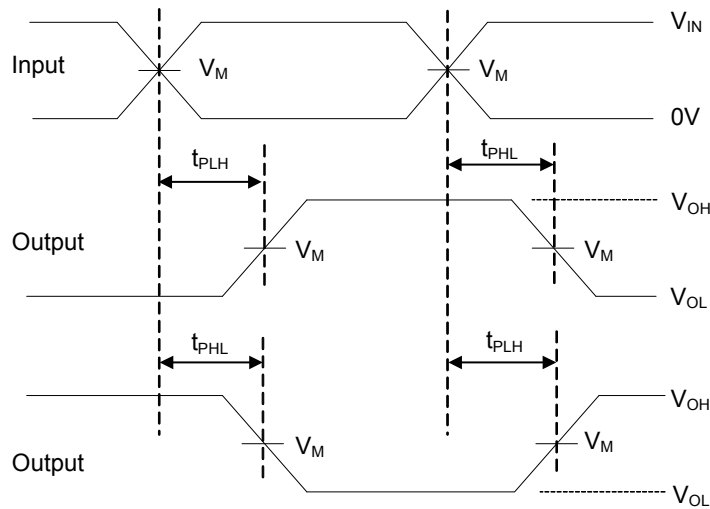
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	V <sub>LOAD</sub>
$t_{PHZ}/t_{PZH}$	GND

Test Circuit

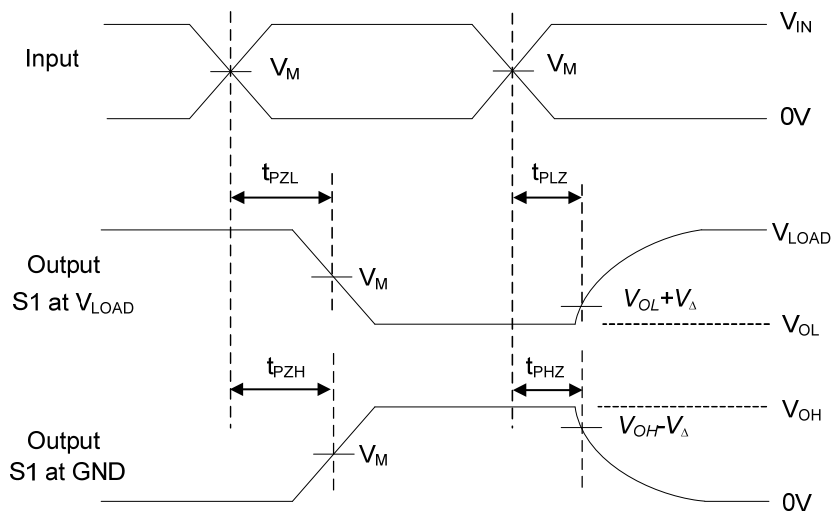
V <sub>CC</sub>	Input		V <sub>M</sub>	V <sub>LOAD</sub>	C <sub>L</sub>	R <sub>L</sub>	V <sub>Δ</sub>
	V <sub>IN</sub>	t <sub>R</sub> , t <sub>F</sub>					
3.3V±0.3V	V <sub>CC</sub>	≤3ns	V <sub>CC</sub> /2	V <sub>CC</sub>	15pF	1kΩ	0.3V
					50pF		
5V±0.5V	V <sub>CC</sub>	≤3ns	V <sub>CC</sub> /2	V <sub>CC</sub>	15pF	1kΩ	0.5V
					50pF		



## ■ TEST CIRCUIT AND WAVEFORMS(Cont.)



Voltage Waveforms Propagation Delay Times



Voltage Waveforms Enable and Disable Times

- Notes: 1.  $C_L$  includes probe and jig capacitance.  
 2.  $P_{RR} \leq 1\text{MHz}$ ,  $Z_0 = 50\Omega$ ,  $t_R \leq 3\text{ns}$ ,  $t_F \leq 3\text{ns}$ .

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