



U74AHCT00

CMOS IC

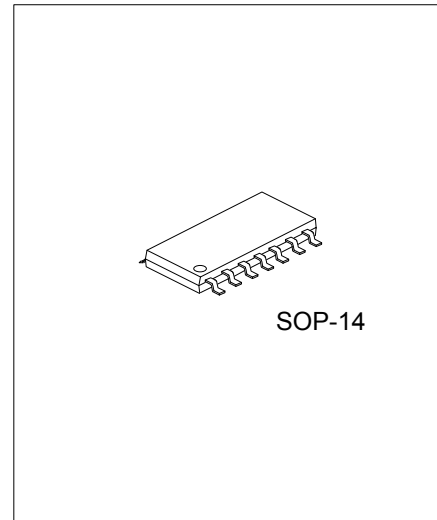
QUADRUPLE 2-INPUT POSITIVE-NAND GATE

DESCRIPTION

The **U74AHCT00** is a quadruple 2-input NAND gate which performs the function $Y=A \cdot B$ or $Y=A + B$.

FEATURES

- * Low Power Dissipation: $I_{CC} = 2.0 \mu A$ (Max.)
- * High Speed: $t_{PD} = 5ns$ (Typ.)
- * High Noise Immunity

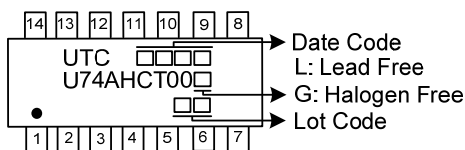


ORDERING INFORMATION

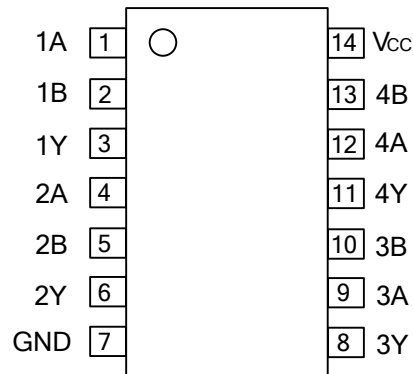
| Ordering Number | | Package | Packing |
|------------------|------------------|---------|-----------|
| Lead Free | Halogen Free | | |
| U74AHCT00L-S14-R | U74AHCT00G-S14-R | SOP-14 | Tape Reel |

| | |
|---|--|
| <p>U74AHCT00G-S14-R</p> <ul style="list-style-type: none"> (1) Packing Type (2) Package Type (3) Green Package | <ul style="list-style-type: none"> (1) R: Tape Reel (2) S14: SOP-14 (3) G: Halogen Free and Lead Free, L: Lead Free |
|---|--|

MARKING



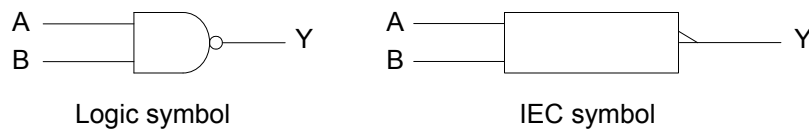
■ PIN CONFIGURATION



■ FUNCTION TABLE (Each Gate)

| INPUTS | | OUTPUT |
|--------|---|--------|
| A | B | Y |
| L | L | H |
| L | H | H |
| H | L | H |
| H | H | L |

■ LOGIC DIAGRAM (Positive Logic)



■ ABSOLUTE MAXIMUM RATING (Note)

| PARAMETER | SYMBOL | RATINGS | UNIT |
|-------------------------|-----------|--------------------|------|
| Supply Voltage | V_{CC} | -0.5~7 | V |
| Input Voltage | V_{IN} | -0.5~7 | V |
| Output Voltage | V_{OUT} | -0.5~ $V_{CC}+0.5$ | V |
| Input Clamp Current | I_{IK} | -20 | mA |
| Output Clamp Current | I_{OK} | ±20 | mA |
| Output Current | I_{OUT} | ±25 | mA |
| V_{CC} or GND Current | I_{CC} | ±50 | mA |
| Storage Temperature | T_{STG} | -65 ~ +150 | °C |

Note: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------------------|-------------|-------------------|-----|-----|----------|------|
| Supply Voltage | V_{CC} | | 4.5 | | 5.5 | V |
| Input Voltage | V_{IN} | | 0 | | 5.5 | V |
| Output Voltage | V_{OUT} | | 0 | | V_{CC} | V |
| Input Transition Rise or Fall Rate | t_R / t_F | $V_{CC}=5.0+0.5V$ | | | 20 | ns/V |
| Operating Temperature | T_A | | -40 | | 85 | °C |

■ STATIC CHARACTERISTICS

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------------------|---------------|--|------|-----|------|------|
| High-Level Input Voltage | V_{IH} | $V_{CC} = 4.5\sim 5.5 V$ | 2.0 | | | V |
| Low-Level Input Voltage | V_{IL} | $V_{CC} = 4.5\sim 5.5 V$ | | | 0.8 | V |
| High-Level Output Voltage | V_{OH} | $V_{CC} = 4.5V, I_{OH} = -50 \mu A$ | 4.4 | 4.5 | | V |
| | | $V_{CC} = 4.5V, I_{OH} = -8 mA$ | 3.94 | | | |
| Low-Level Output Voltage | V_{OL} | $V_{CC} = 4.5V, I_{OL} = 50\mu A$ | | | 0.1 | V |
| | | $V_{CC} = 4.5V, I_{OL} = 8 mA$ | | | 0.36 | |
| Input Leakage Current | $I_{I(LEAK)}$ | $V_{CC} = 0\sim 5.5V, V_{IN} = V_{CC}$ or GND | | | ±0.1 | μA |
| Quiescent Supply Current | I_Q | $V_{CC} = 5.5V, V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0$ | | | 2 | μA |
| Additional quiescent Supply Current | ΔI_Q | $V_{CC} = 5.5V, V_{IN} = 3.4V$; other input at V_{CC} or GND; $I_{OUT}=0$ | | | 1.35 | mA |
| Input Capacitance | C_{IN} | $V_{CC} = 5V, V_{IN} = V_{CC}$ or GND | | 2 | 10 | pF |

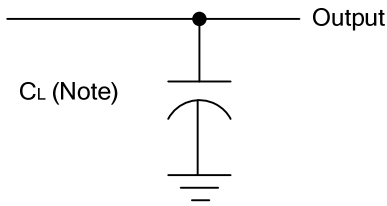
■ DYNAMIC CHARACTERISTICS ($t_R, t_F \leq 3 ns$)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|-----------|------------------------------------|-----|-----|-----|------|
| Propagation delay from input (A and B) to output (Y) | t_{PLH} | $V_{CC} = 5\pm 0.5 V, C_L = 15 pF$ | | 5 | 6.9 | ns |
| | t_{PHL} | | | 5 | 6.9 | |
| | t_{PLH} | $V_{CC} = 5\pm 0.5 V, C_L = 50 pF$ | | 5.5 | 7.9 | |
| | t_{PHL} | | | 5.5 | 7.9 | |

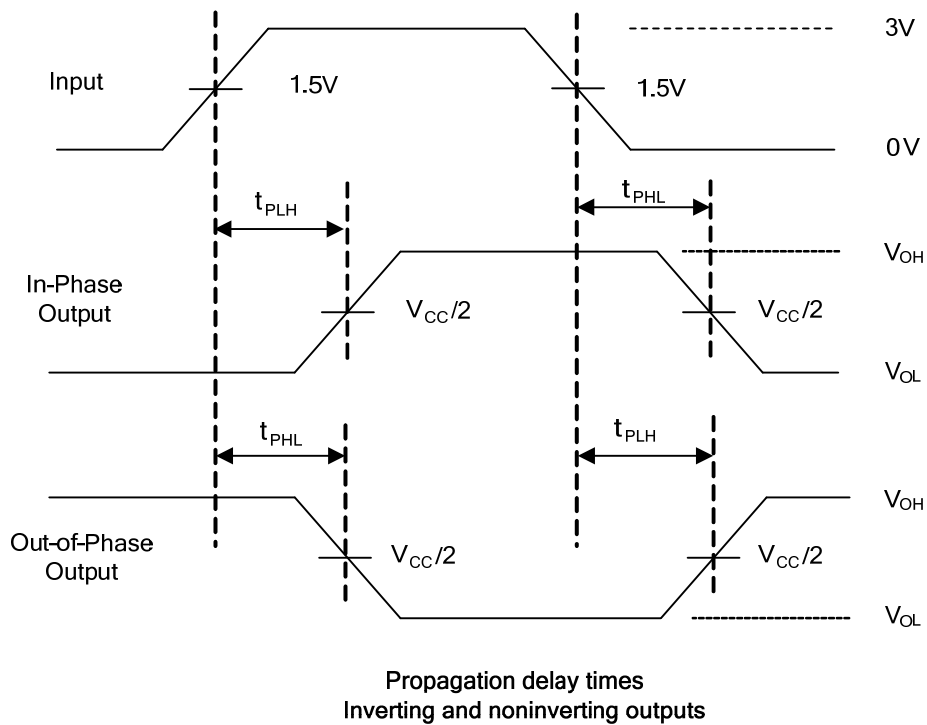
■ OPERATING CHARACTERISTICS ($V_{CC} = 5V; T_A = 25^\circ C$)

| PARAMETER | SYMBOL | TEST CONDITIONS | TYP | UNIT |
|-------------------------------|----------|-------------------|------|------|
| Power Dissipation Capacitance | C_{PD} | No load, $f=1MHz$ | 10.5 | pF |

■ TEST CIRCUIT AND WAVEFORM



Note: C_L includes probe and jig capacitance.



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